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Tunable Microwave Phase Locked Oscillator

Phase Locked Loop Implementation

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The demand for high data rates and low power consumption has had a major impact on the design of RF frequency synthesis systems. The need for highly stable oscillators is one of the main driving force in most communication systems that utilise the super heterodyne architecture. Not only the communication systems, but a variety of measurement equipment require a low noise local oscillator such the spectrum analyser.

The goal of this thesis work was to design and analyse frequency synthesis in the microwave range for laboratory use. The design utilises the Analog Devices ADF4155 Phase Locked Loop synthesizer integrated circuit. The chip incorporates the control circuitry required to implement a phase locked oscillator.

The Phase Locked Oscillator system compromises the ADF4155 PLL, Zcomm V940ME03 Voltage Controlled Oscillator and a fourth order Loop Filter. The thesis concentrates mainly on the design and analysis of the loop filter and the characterisation of the phase noise of the generated signal.

Finally, an L-Band signal of 1.45 GHz is generated and phase noise measurement is done. The measured value of the phase noise is compared with the simulated value. Further work may involve doing measurements on frequency settling time and phase jitter of the generated signal.

Keywords	Phase Locked Oscillator, Loop Filter, Phase Noise, Frequency Synthesis, L-Band, Fractional-N.

Contents

Acronyms

VCO	Voltage Controlled Oscillator
LO	Local Oscillator
PLL	Phase Locked Loop
TCXO	Temperature Compensated Crystal Oscillator
PFD	Phase Frequency Detector
CP	Charge Pump
DPLL	Digital Phase Locked Loop
RF	Radio Frequency
PLO	Phase Locked Oscillator
ECL	Emitter Coupled Logic
CMOS	Complementary Metal Oxide Semiconductor
PM	Phase Modulated
AM	Amplitude Modulated
DUT	Device under Test
SSB	Single Sideband
RMS	Root Mean Square
SRD	Step Recovery Diode
OCXO	Oven Compensated Crystal Oscillator
ASIC	Application Specific Integrated Circuit

1 Introduction

Today's communication systems demand higher frequency, higher data rates, and more channels of operation. The need for low power, portable equipment is also pushing the limits of modern electronic design. Since most of the modern communication systems use the super heterodyne architecture, there is a need for designing highly stable, low noise local oscillator. For simple design a free running Voltage Controlled Oscillator (VCO) will suffice but when low phase noise and high stability is required the design needs to be reconsidered.

Typical local oscillator (LO) synthesizers combine a Voltage Controlled Oscillator (VCO) with a Phase-Locked Loop (PLL) IC, high stable frequency reference (e.g. Crystal/TCXO) and a loop filter. The VCO is used to generate the RF output frequency, typically in the Gigahertz (GHz) range, and the PLL is used to stabilize and control the frequency. The loop filter design must integrate all of the components to establish a trade-off between noise and transient response. These all interacting components make up the Phase-Locked Oscillator circuit which acts as local oscillator in many super heterodyne architectures.

2 Theoretical Background

In this chapter the theory behind frequency synthesis will be examined. The purpose of the synthesizer as a part of the transceiver architecture is also introduced. The phase-locked loop method is studied and the technique used to control the slave oscillator (VCO) with the master oscillator temperature compensated crystal oscillator (TCXO) is presented.

2.1 Purpose

While there are several forms for receiving and processing signals, the most widely used one is the super heterodyne. The super heterodyne (RX, TX) makes use of the heterodyne principle of mixing an incoming signal with the local oscillator (LO) signal in a non-linear element. The super heterodyne receiver RX uses LO frequency offset by a fixed intermediate frequency (IF) from the desired signal. This can be expressed as

$$IF = |f_r \pm f_{LO}| \tag{1}$$

Where

IF is the output or intermediate frequency

f_{rf} is the frequency of received signal of bandwidth B_w

f_{LO} is the local oscillator frequency

The mixer is a nonlinear element that produces frequencies at the sum and difference of the input frequencies (and a variety of other undesired signals).

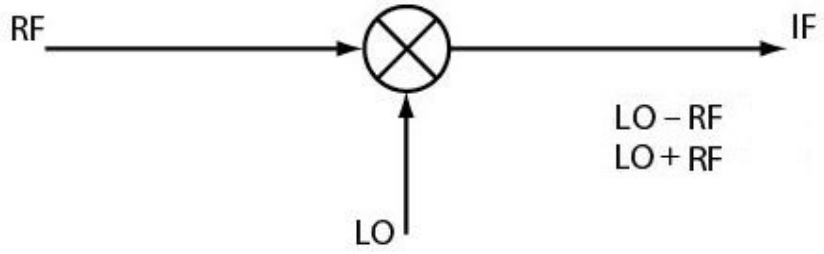

Figure 1 Mixing of RF with LO signal to produce Intermediate Frequency (IF)

Figure 1 illustrates the mixing produces two different signals the unwanted one will be filtered and the other is further processed.

2.2 PLL Basics

A phase-locked loop is a feedback system that is combining a voltage controlled oscillator (VCO), a reference oscillator and a phase frequency detector (PFD), allowing the phase control given specific accuracy. The first phase-locked loops were implemented in the early 1930s by a French engineer, de Bellescize. However the PLL found broad acceptance in the marketplace when the integrated circuit PLLs became available at lower cost components in the mid-1960s. [1.]

The PLL allows the generation of a variety of output frequencies as multiples or fractions of a single reference frequency. The PLL can be used to accomplish many tasks such as carrier recovery, clock recovery, tracking filters, frequency and phase demodulation, frequency synthesis, and clock synchronization. The main application of the PLL in this thesis work is to generate a local oscillator (LO) that can be used in a microwave systems.

The phase-locked loop can be analysed in general as a negative feedback system with a forward gain term and a feedback term. A simple block diagram of a voltage-based negative-feedback system is shown in Figure 2.

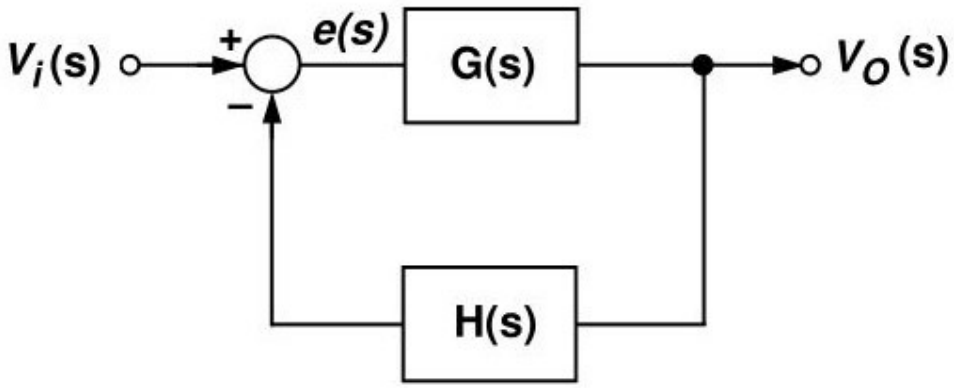

*Figure 2 Standard negative-feedback control system model (*Modified from Curtin et al (1999) [1]).

In a PLL, the error signal *e(s)* from the phase frequency detect (PFD) is the difference between the input frequency or the phase and that of the signal fed back to the system. The system will push the frequency or phase error signal to zero in the steady state. The standard equation for a negative-feedback system apply. [1; 2.]

$$Forward\ = G(s) \tag{2}$$

$$Open\_Loop\ Gain = G(s) \times H(s) \tag{3}$$

$$\begin{aligned} V_o(s) &= G(s)[V_i(s) - H(s) \times V_o(s)] \\ V_o(s)[1 + H(s) \times G(s)] &= G(s) \times V_i(s) \\ Closed\_Loop\ Gain &= \frac{G(s)}{1 + G(s) \times H(s)} \end{aligned} \tag{4}$$

Because of the integration in the loop the steady state gain, G(s), is high and

$$\frac{V_o}{V_I}, Closed\_Loop\ Gain = \frac{1}{H(s)} \tag{5}$$

The different components of a phase-locked loop that contribute to the loop gain include:

1. The *phase frequency detector* (PFD) and *charge pump* (CP), sensitivity K_d.
2. The *loop filter,* with transfer function of Z(s)
3. The *voltage-controlled oscillator* (VCO), with a sensitivity of K_V
4. The *feedback divider,* 1/N

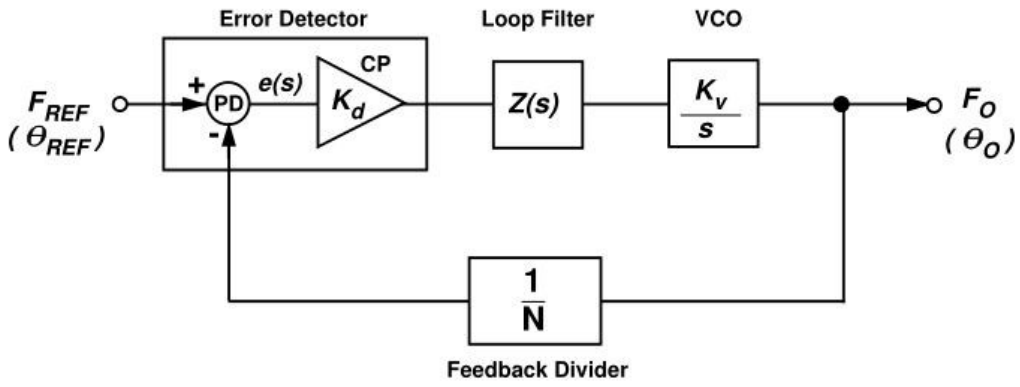

*Figure 3 Basic phase-locked loop model (*Copied from Curtin et al (1999) [1]).

If a multiplier is employed as the PFD, the loop filter and VCO are also analog elements, this is called an analog, or linear PLL (LPLL). Instead of the multiplier if Exclusive OR (EXOR) gate or J-K flip flop is used as the PFD and everything else stays the same, then it is a digital PLL (DPLL). Further if the PLL is built exclusively from digital blocks, without any passive components or linear elements, it becomes all-digital PLL (ADPLL). [1.]

As shown in Figure 3, a PLL is used to generate a signal output that has the stability of the reference source. The VCO oscillates at an angular frequency ω_o. The frequency/phase signal is fed back to the PFD, via a frequency divider with a ratio of 1/N for integer-N PLL.

When the two signals in to the PFD are almost equal in phase the error tends to be zero, the loop will be in a locked condition. The input, output frequency and error signal are related as

$$e(s) = F_{REF} - \frac{F_O}{N} \tag{6}$$

When

$$e(s) = 0, \frac{F_O}{N} = F_{REF} \tag{7}$$

Hence

$$F_O = N\, F_{REF} \tag{8}$$

In commercial PLL chips, the phase frequency detector and charge pump form the error detector block. When the two input signals are not equivalent the error detector will output source/sink current pulses to the low-pass loop filter. The loop filter smooths the current pulses into a voltage that controls the VCO frequency. The voltage is applied to the VCO to adjust its output frequency by $K_V \Delta V$, where K_V is the VCO sensitivity in

MHz/Volt, and ΔV is the change in the tune voltage of the VCO input. The relationship between the output frequency and VCO tune voltage is shown in Figure 4. [1; 2.]

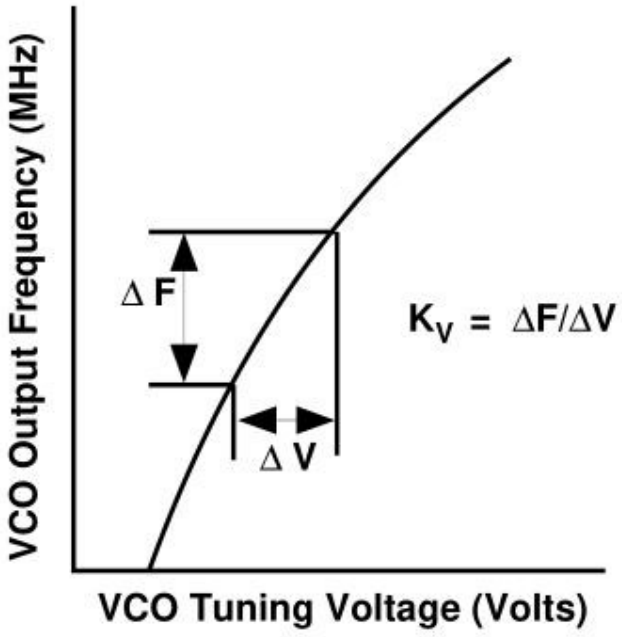

*Figure 4 VCO transfer characteristics (*Reprinted from Curtin et al (1999) [1]).

$$K_v = \left.\frac{\partial f}{\partial v}\right|_{v=v_0} \tag{9}$$

The closed-loop gain of the PLL can then be expressed by applying the concept of the negative-feedback system presented earlier. [1.]

$$\frac{F_O}{F_{REF}} = \frac{Forward\ Gain}{1 + Loop\ Gain} \tag{10}$$

$$Forward\ Gain, G(s) = \frac{K_D K_V Z(s)}{s} \tag{11}$$

$$Loop\ Gain, G(s)H(s) = \frac{K_D K_V Z(s)}{Ns} \tag{12}$$

When the Loop Gain is >>1, the closed-loop transfer function for the PLL system becomes N and hence

$$F_{OUT} = N \times F_{REF} \tag{13}$$

2.3 Linear Analysis of Classical PLL Circuits

The model shown in Figure 3 is a closed-loop feedback system. The transfer function from reference phase input to VCO phase output, T(s), can be obtained as

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d F(s) K_v / s}{1 + K_d F(s) K_v / s} \quad (14)$$

$$= \frac{K_d F(s) K_v}{s + K_d F(s) K_v} \quad (15)$$

Similarly, the sensitivity transfer function from the reference phase input to the phase error, $S(s)$, is

$$S(s) = \frac{\theta_d(s)}{\theta_i(s)} = \frac{1}{1 + K_d F(s) K_v / s} \quad (16)$$

The basic properties of interest in this transfer function are the loop stability, order, and the system type. The stability of the system can be determined by a variety of methods, such as root locus, Bode plots, Nyquist plots, and Nichols charts. [3; 5.]

2.3.1 Type and Order of the PLL

The type of the PLL refers to the number of poles at DC of the loop transfer function G(s)H(s) located at the origin. The pole usually refers to the denominator in the transfer function.

For example:

$$G(s)H(s) = \frac{3}{s(s+3)} \quad (17)$$

This system is type I as there is only one pole at the origin.

The order of the PLL refers to the total number of poles or to the highest degree of *s* in the denominator.

$$1 + G(s)H(s) = 0 \Delta\, C.E. \quad (18)$$

Where C.E. is the Characteristic Equation. The roots of the C.E. become the closed loop poles of the transfer function:

$$1 + G(s)H(s) = 1 + \frac{3}{s(s+3)} = 0 \quad (19)$$

Then

$$C.E. = s(s+3) + 3 \quad (20)$$

$$C.E. = s^2 + 3s + 3 \quad (21)$$

Which is a 2nd order polynomial. Thus, for the given G(s)H(s), is the type 1 second order system.

2.3.2 The Steady-State Error

Steady state errors of the PLL can be obtained by applying the Final Value Theorem

$$\lim_{t\to\infty} \theta_d(t) = \lim_{s\to 0} s\theta_d(s) \tag{22}$$

$$= \lim_{s\to 0} s\theta_i(s)S(s). \tag{23}$$

From equation 16, the presence of a voltage controlled oscillator (VCO) makes every PLL at least a Type 1 system, achieving zero steady state error to a phase step at θ_i. For a ramp or a frequency step, there must be another integrator in the forward path, and the natural place for this is the loop filter, $Z(s)$. [3; 5.]

A third order PLL, which can be Type 3 and have a zero steady state error to a frequency ramp, is relatively rare. There two reasons for this. First, the applications that require that type of performance are found only in very high frequency communications where the Doppler shift of the signal produces a frequency ramp. The second reason is to do with the stability of the third order loop versus that of the second order loop. [1; 3; 5.]

2.4 Nonlinear analysis of Classical PLL Circuits

For simplicity, in most cases, when a phase-locked loop is analysed, it is assumed, or approximated, that the components behave linearly. This can help with faster analysis as seen in section 2.3 but when the PLL is implemented there will be discrepancies between measured and simulated values. The reason for this is because the components are behaving differently when implemented in circuit then simulated. There are many nonlinear analysis of PLL devised during the years but only three will be discussed here. [3; 5.]

2.4.1 Phase Plane

One of the earliest methods of nonlinear system analysis is the graphical method of phase plane design. This method of analysis dates back to the early days of PLL before the widespread use of computers for such calculations. The use of phase plane portraits is made more practical by the fact that most PLLs are first or second order which does not go beyond the restrictions on phase plane techniques.

2.4.2 Lyapunov redesign

Starting with sinusoidal phase detector, mixer, shown in Figure 15, it is possible to apply the technique of Lyapunov Redesign to phase-locked loops. More recently, this method has been extended to classical digital PLLs.

2.4.3 Circle/Popov Criteria

The difficulty of applying Lyapunov methods to higher order loops has led to the exploration of nonlinear analysis methods suitable for numerical techniques. In particular, the Circle Criterion and the Popov Criterion have been used to check the stability of higher order PLLs.

2.5 Phase Noise (Spectral Purity)

Phase noise is a measure of the short-time stability of oscillators. Phase noise is caused by variations of phase or frequency and amplitude of an oscillator output signal, although the amplitude effect is negligible in most cases. These variations have a modulating effect on the oscillator signal. [14.]

The phase noise is specified as single-sideband phase noise referenced to the carrier power and as a function of the carrier offset.

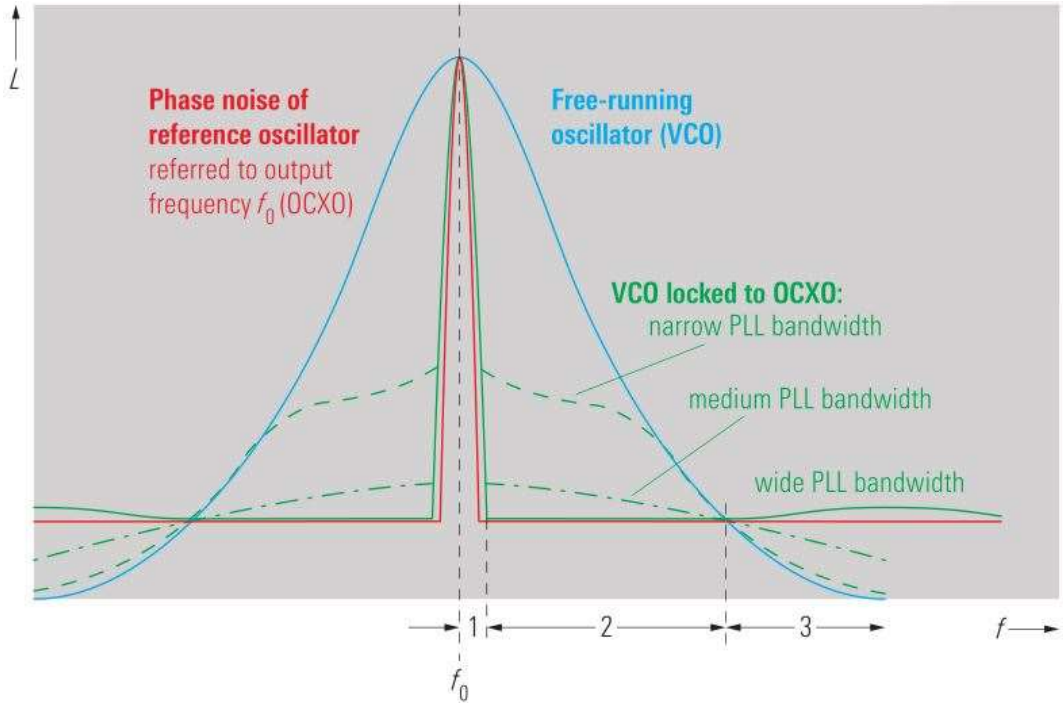

Figure 5 Phase noise contributions of reference OCXO and VCO

The effects of phase noise are illustrated in Figure 5. With high resolution it is expected a single spectral line for a purely sinusoidal signal in the frequency domain but due to noise this is not the case. Phase noise analysis of the VCO is covered in detail in Chapter 4.

3 Phase-Locked Oscillator Components

3.1 Introduction

Phase-locked oscillator (PLO) are the most used systems to synthesize microwave local oscillator frequencies of high spectral purity which are very important in communications and radar application. It combines the far-out phase noise of fundamental oscillators, especially in the microwave frequency range, an excellent long-term stability, and the close-in phase noise of a crystal oscillator (from carrier frequency to 100 kHz away).

A voltage-controlled oscillator can be phase locked by two methods [8]:

1. Digital phase lock: This is usually achieved by using a frequency divider to divide the higher frequency of the VCO to the same frequency of the crystal reference. A digital phase detector is then used to acquire the phase lock. The advantage of this method is that it is self-acquiring and can operate at very low frequencies. It is widely used at low frequencies from 1 MHz to 3 GHz. However, this method has two disadvantages. First, the noise floor of the divider will limit its close in phase noise; and second, at microwave frequencies it will not be economical.
2. Analog phase lock: This is achieved by using Step Recovery Diode (SRD) as a comb generator to create a comb of reference frequencies to the frequency of the VCO. The phase detecting is accomplished by using a multiplier (mixer) to detect the phase difference between the reference and the VCO.

Phase-locked oscillator consists of various elements which form the complete system. Most of the components that form the phase-locked oscillator can be obtained as a ready-made integrated circuit chips. Figure 6 shows a basic block diagram of a phase-locked oscillator. The design of the passive loop filter will be the focus of this thesis since the other parts are available in IC form.

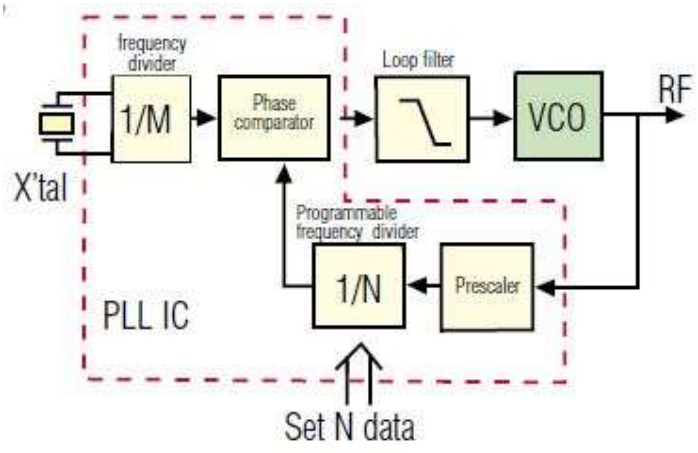

Figure 6 Basic Diagram of Phase-locked Oscillator

For the implementation of the PLO the digital phase lock technique is used by employing the Analog Devices ADF4511 PLL synthesizer chip.

3.2 Reference oscillator

A reference oscillator is one of the most important components that define the stability and phase noise characteristics of frequency synthesizer. In a frequency synthesis system the reference oscillator is the master clock and VCO is the slave clock. Various reference oscillator schemes are possible as shown in Figure 7. A 10 MHz temperature-compensated crystal oscillator (TCXO) provides a small size and cost benefits for low- to moderate-performance applications. [9.]

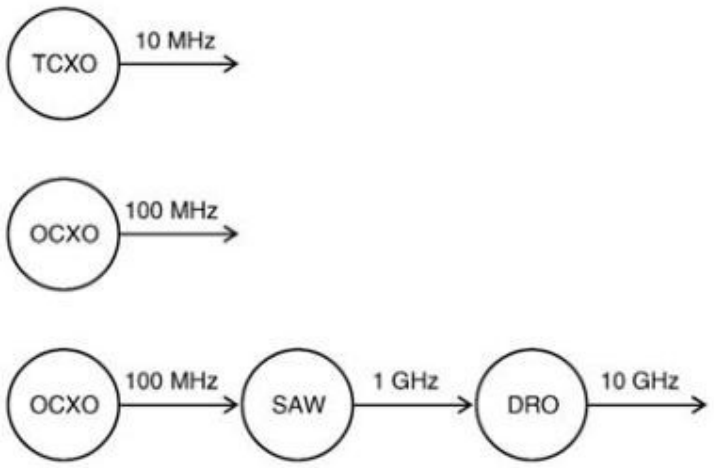

*Figure 7 Reference frequency generation schemes (*Adapted from Chenakin (2008) [9]).

Better stability and noise characteristics can be achieved by using an oven-compensated crystal oscillator (OCXO), but this is a more expensive and bulky part with higher power consumption. It is worth mentioning, that using higher frequency OCXO (e.g., 100 MHz instead of 10 MHz) can potentially result in a better synthesizer noise. There is a comparable noise floor for both parts, but the high frequency reference requires a significantly lower overall multiplication factor.

Though better phase noise performance at higher frequency offsets (100 kHz and above) can be obtained with additional low-noise oscillators (e.g., SAW, CRO, or DRO) locked to the main OCXO. The chain of oscillators provides the lowest phase noise profile at any frequency offset and can be used in high-end synthesizer designs [9].

3.3 Phase Detectors

Phase detectors employed in phase locked oscillator (PLO) are *multiplier* circuits and *sequential* circuits. Multipliers output average DC value which is the product of input-

signal waveform and VCO waveform. Well-designed multipliers are very capable on operating at an input signal buried deeply in noise and that is one reason they are mostly employed at frequencies above 10 GHz. [5,114; 9.]

Sequential phase detectors contain memory and can recall past events. They are mostly more flexible compared to the multiplier but they have poor noise-handling capability. Sequential phase detectors are usually built up from digital circuits (flip-flops, gates) and operate mostly with binary, rectangular input waveforms. Although they are mostly referred to as “digital” phase detectors this is basically incorrect since the output of a sequential phase detector is an analog quantity and the loops are analog. [4; 5.]

The phase detector generates the error signal required in the feedback loop of the synthesizer. The majority of PLL application specific integrated circuits (ASICs) use a sequential circuit called a Phase Frequency Detector (PFD) similar to the one shown in Figure 8. Compared with mixers or XOR gates, which can only resolve the phase differences in +/- π range, the PFD can resolve phase differences in the +/- 2π range or more typically “frequency difference” is used to describe a phase difference of more than 2π, hence the term “phase frequency detector”. This circuit shortens the transient switching times and performs the function in a simple and elegant digital circuit.

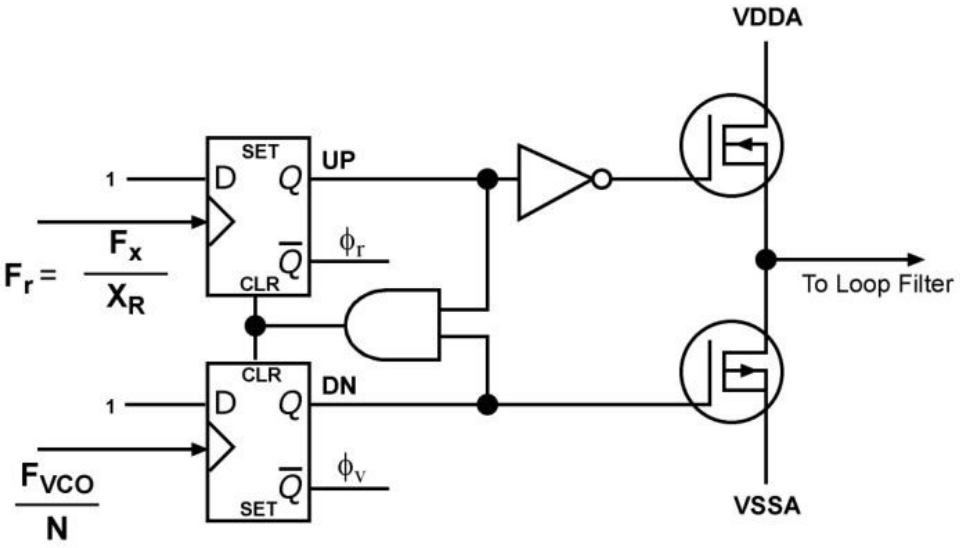

*Figure 8 Phase Frequency Detector Schematic (*Copied from Barrett (1999) [6]).

The PFD compares the F_r with that of (F_{VCO}/N) and activates the charge pumps based on the difference in phase between these two signals. The operational characteristics of the phase detector circuitry can be broken down into three modes: frequency detect,

phase detect, and phase locked mode. When the phase difference is greater than ±2π, the device is considered to be in frequency detect mode.

In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency.) The loop filter integrates this current and the result is continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2π.

Once the phase difference between the two signals is less than 2π, the PFD begins to operate in the phase detect mode. In this mode of operation the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals as shown in Figure 9. Once the phase difference between the two signals reaches zero, the device enters the phase locked state.

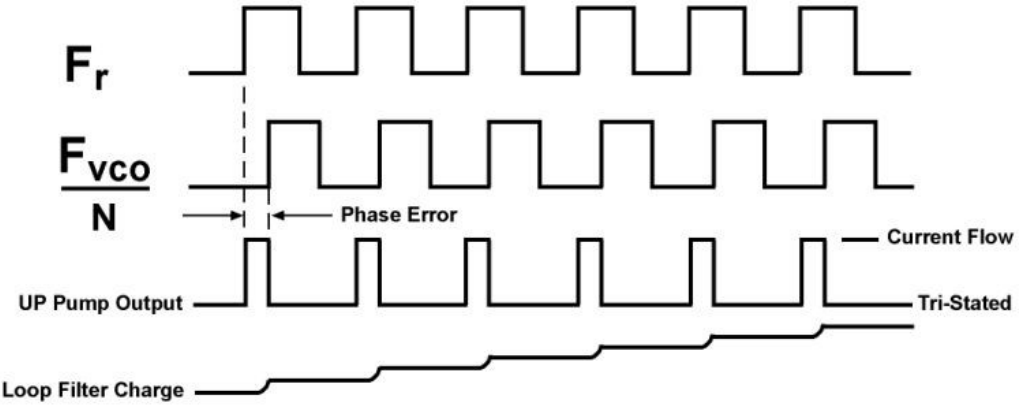

*Figure 9 Phase Detector Output (Voltage, Current) Waveforms, for Fv/N<Fr (*Copied from Barrett (1999) [6]).

In phase locked state, the PFD output will be narrow “spikes” that occur at a frequency equal to F_r. These current spikes are due to the finite speed of the logic circuits (see Figure 10, D_{OA} blow-up) and will have to be filtered so they do not modulate the VCO and generate spurious signals.

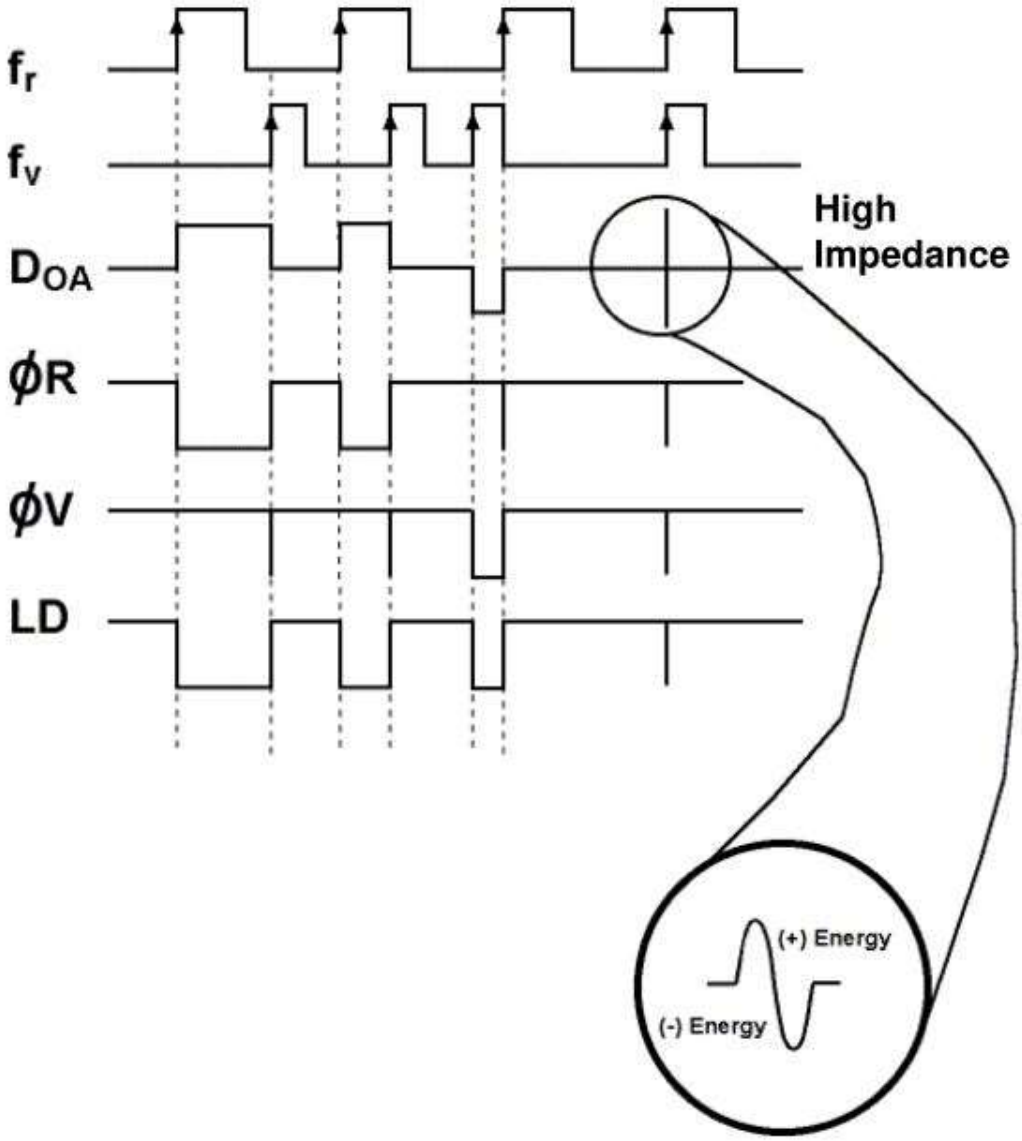

*Figure 10 Phase Detector Timing Waveforms (*Copied from Barrett (1999) [6]).

The PFD suffers from a zero phase error dead-zone. Because of the logic circuits inside the PFD have non-zero propagation delays and rise time, therefore, the PFD is never capable of generating short pulses for resolving small phase error between the two input signals.

The minimum time difference that the phase-frequency detector can sense is called the backlash time. The dead-zone results in undesired behavior of the phase-frequency detector and may lead to unexpected behavior of the phase-locked loop operation.
One way to tackle this phenomenon is the charge pump output approach, also another solution is defining the minimum on time for both source and sink charge pumps in locked

state. This undesired behavior of the phase-frequency detector will be the reference spurs to be generated. These spurs are mostly the result of mismatches and leakages in the charge pump circuit.

Phase frequency detectors (PFD) operate in a frequency discriminator mode for large initial frequency errors and to perform as a coherent phase detector once the system transient response is within the pull-in range of the phase-locked loop as shown in Figure 11.

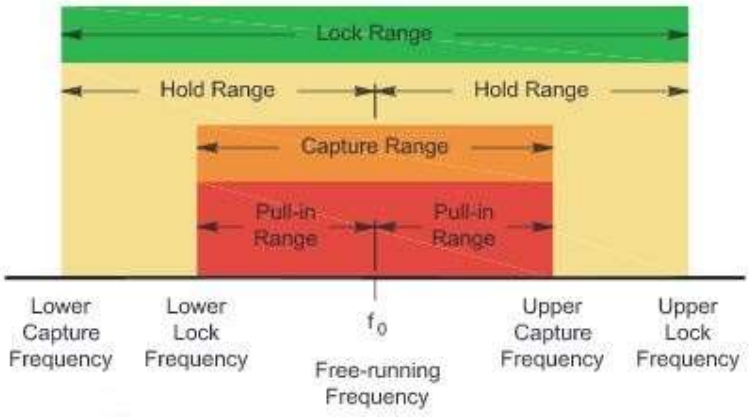

Figure 11 Operating ranges of PLL (Modified from Karhu [4]).

The PLL should have a good tracking capability. The hold range, $\Delta\omega_H$, is the frequency range that the PLL is able to maintain phase tracking. It can be determined by the calculation of the frequency offset at the reference input that causes the phase error to be beyond the range of linear analysis. For a multiplier or XOR phase detector the phase error is 90˚. For sequential detectors, such as the phase frequency detector (PFD) it will be larger. The phase detector and the hold range is related by the following equation. [3; 5.]

$$\Delta\omega_H = K_O K_d Z(0). \tag{24}$$

The lock range, $\Delta\omega_L$, is defined as the frequency range within which the PLL locks within one single-beat note between the reference frequency and output frequency. The lock range is calculated from nonlinear equation, but there are useful approximations that are made. In particular, if the relative order of numerator and denominator of the PLL is 1, then the loop can be said to behave like a first order loop at higher frequencies, and thus the lock range can be estimated as. [3; 5.]

$$\Delta\omega_L \approx \pm K_O K_d Z(\infty)\,. \tag{25}$$

The pull-in range, $\Delta\omega_p$, is defined as the frequency range in which the PLL will always become locked. [3.]

3.4 Loop Filter

Phase-frequency detectors with the current source charge pump seem to be the most used in commercial low cost synthesizer chips. The charge pump PLL offers many advantages over the traditional ones such as an infinite pull-in range and zero steady state error. The design of the loop filter involves a trade-off between reference sidebands and switching speed. The loop filter should be designed for the correct balance between reference spurs and the lock time that the system requires. [2; 3.]

There are two types of loop filters employed in PLL design, active and passive. Active loops use op-amps, are usually differential, and allow the synthesizer to generate tuning voltage levels higher than PLL IC can generate on-chip. The op-amp itself provides the DC amplification necessary to develop a control voltage that is higher than the on-chip supply of the phase detector. Active loops are mostly used in wideband applications. Most PLL ASICs use a current source for the output to generate the control voltage. This output is proportional to the phase error. This current source loop filter configuration is the most popular for wireless, narrow-band applications. [3.]

There are many types of passive loop filter. The most employed one, in simple designs, is the third-order shown in Figure 12. As a rule of thumb, the loop filter bandwidth should be 1/10 of the PFD frequency (channel spacing). Increasing the loop bandwidth will reduce lock time, but the filter bandwidth should never be more than PFD/5, to avoid significantly increasing the risk of instability.

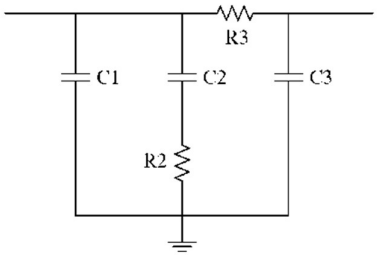

Figure 12 A third-order loop filter.

The bandwidth of the loop filter can be doubled by either doubling the PFD frequency or the charge-pump current. If the actual K_v of the VCO is significantly higher than the nominal K_v used to design the loop filter, the loop bandwidth will be significantly wider than expected. The variation of the loop bandwidth with K_v presents a major design challenge

in wideband PLL designs, where K_v can vary by more than 300%. Adjusting the programmable charge-pump current of the chip is the easiest way to compensate for changes in the loop bandwidth caused by variation in K_v.

3.4.1 Stability of the control system

Determining the stability of the phase-locked loop is very important part of the design of a frequency synthesizer. Stability analysis not only determines whether the loop will oscillate, but determines the overall performance of the loop. Bode-plot is one of the useful tools for analysing the stability of a control system. It displays the open-loop transfer function magnitude and phase. If G(s) = -1 then <G(s) = -180° then in these conditions the denominator of the transfer function

$$\frac{F_O}{F_{REF}} = \frac{Forward\ Gain}{1 + Loop\ Gain} \tag{26}$$

Becomes zero and the transfer response becomes infinite making the loop unstable. [4.]

This is the reason why the difference of the phase of the open-loop gain from 180° at the frequency when the gain equals unity is the common measure of the stability, called phase margin. A second order loop is unconditionally stable because the maximum phase shift of the two poles is -180° and this occurs at very high frequencies when the gain is less than unity. As a rule of thumb, in order for a system to be stable, phase margin should be somewhere between 45° to 50°. [4.]

The loop filter shown in Figure 13 is a low-pass type. The transient response of the loop depends on:

1. the magnitude of the pole/zero,
2. the charge pump sensitivity K_d,
3. the VCO sensitivity K_v,
4. the feedback factor, N in case of integer-N PLL

The above four parameters should be taken into account when designing the loop filter. Also the filter should be designed so the system (PLL) is stable (around 45˚ phase margin). The 3-dB cutoff frequency is the loop bandwidth, B_W. Larger loop bandwidths have the advantage of fast settling time but with the cost of increased noise in the PLL which is mostly avoided. [1; 2.]

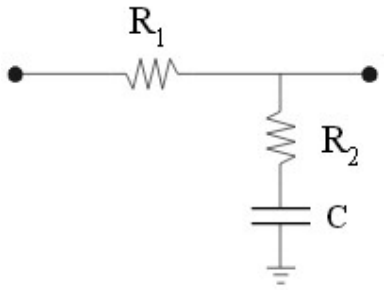

Figure 13 Second Order Passive Lag Filter

For a 2nd loop with natural frequency (loop bandwidth) $\omega_n$and damping factorδ, the switching speed (T_{SW}) is proportional to the inverse of their product.

$$T_{SW} \propto \frac{1}{\omega_n \delta} \tag{27}$$

Further the second order PLL system can be described as follows:

$$H(s) = N\frac{s\left(2\delta\omega_n - \frac{N{\omega_n}^2}{K_d K_V}\right) + {\omega_n}^2}{s^2 + 2\delta\omega_n s + {\omega_n}^2} \tag{28}$$

Where

$$\delta = \frac{1}{2}\sqrt{\frac{K_d K_V}{NC(R_1 + R_2)}}\left(CR_2 + \frac{N}{K_d K_V}\right) \tag{29}$$

And

$$\omega_n = \sqrt{\frac{K_d K_V}{NC(R_1 + R_2)}} \tag{30}$$

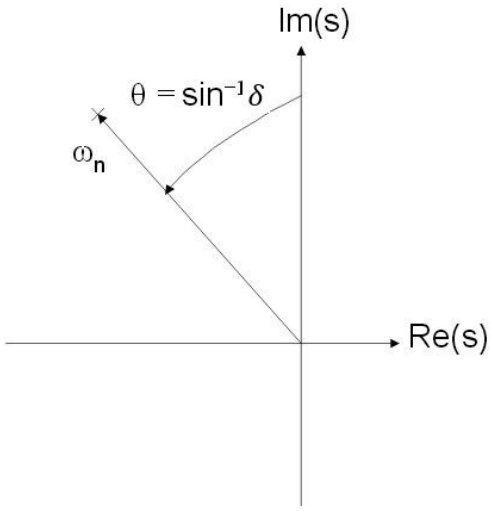

Figure 14 Complex Poles S-Plane Plot

From Figure 14 the poles are located at distance ω_n from the origin and at an angle $\theta = sin^{-1}\delta$. The damping factor, δ, is a measure of stability.

3.4.2 PLL Control Theory

Phase-locked Loops have many unique characteristics when viewed from the control theory perspective. The first part is that their correct operation depends on the fact that they are nonlinear devices contrary to one presented in Section 2.2 for simplifying the analysis. The loop does not work as expected without the presence of nonlinear devices, namely the phase-detector, when the phase detector is employed as a mixer, and VCO. These devices take the problem from signal response to phase response and back again. This is further accompanied by the time scale shift involved since the PLLs operate on signal whose centre frequency is much higher than the loop bandwidth. Most of the time the order of the PLL is either first or second order. The complete feedback loop design replaces control law design, and the design is governed only by the required characteristics of the input reference signal and the required output signal. [3.]

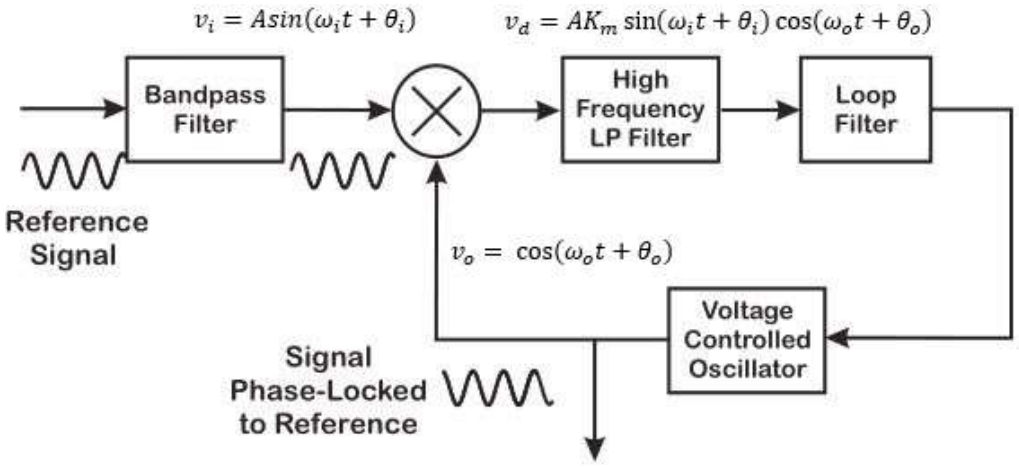

*Figure 15 Classical PLL using mixer as phase detector (*Modified from Abramovitch (2003) [3]).

The idea is that if a sinusoidal signal is injected into the reference, the internal oscillator will lock to the reference such that the frequency and phase differences between them will be driven to some constant value or 0 (depending on the system type). The internal sinusoid then represents a smoothed version of the reference. [2; 3.]

Practical PLLs mostly resemble the diagram shown in Figure 15, in which a high frequency low-pass filter is used to attenuate the double frequency term of the mixer and bandpass filter is mostly used to limit the bandwidth of input signal to the loop.

A general sinusoidal signal at the reference input of a PLL as shown in Figure 15 can be written as [3]:

$$v_i = Asin(\omega_i t + \theta_i). \tag{31}$$

For simplicity it is assumed that the output signal from the Voltage Controlled Oscillator (VCO) into the mixer is given by

$$v_o = VCO_{out} = \cos(\omega_o t + \theta_o). \tag{32}$$

The output of the mixer is then given by

$$v_d = Mixer_{out}(t) = AK_m \sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) \tag{33}$$

Where K_m is the conversion gain of the mixer.

The analysis is done by taking several steps. One that is mostly used is the trigonometric identity in terms of the PLL:

$$\begin{aligned} &2\sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) \\ &\qquad = \sin\big((\omega_i + \omega_o)t + \theta_i + \theta_o\big) + \sin((\omega_i - \omega_o)t + \theta_i - \theta_o) \end{aligned} \tag{34}$$

Taking two fundamental assumptions leads to the most commonly used model of the analog PLL.

Let

$$\theta_d = \theta_i - \theta_o \tag{35}$$

Then the assumptions are:

1. The first part in Equation 34 is attenuated by the loop filter and by the low pass nature of the PLL itself.
2. $\omega_i \approx \omega_o$, so the difference can be incorporated into θ_d.

Making these assumptions leads to the PLL model shown in Figure 3.

The problem is that the system is still nonlinear and as such in general difficult to analyze. The typical methods of analysis include [3]:

1. Linearization: For θ_d small and slowly varying

   $$\sin\theta_d \approx \theta_d, cos\theta_d \approx 1, and\ {\theta_d}^2 \approx 0. \tag{36}$$

   This is useful for studying loops that are near lock and it does not help in the analysis of the loop when θ_d is large.
2. Phase plane portraits is the graphical method of analyzing the behavior of low order, usually up to 2, nonlinear systems about a singular point.
3. Simulation is another type of analysis but it is not easy so most of the time the response of the components of the PLL (phase detector, filter, VCO) are simulated in signal space and then the entire loop is simulated only in phase space.

The linearized model shown in Figure 3 is what is used mostly for the analysis and measurements of phase-locked loops. It is possible to learn a few things about the behavior of the PLL from linear analysis. However, this model does not accurately represent the system and some issues come up when constructing the PLL.

3.5 Voltage Controlled Oscillator

Voltage Controlled Oscillator is a fundamental building block in the frequency synthesizer architecture. The VCO has a variety of applications e.g. in communication, PLL, medical field etc. In the above mentioned applications, high frequency with low power is required.

There are many requirements placed on VCOs in different applications. These requirements are usually in conflict with one another, and therefore a compromise is needed. Some of the more important requirements include [12]:

1. Phase noise(dBc/Hz)
2. Tuning sensitivity (Hz/V)
3. RF power (dBm)
4. Harmonic/Spurious (dBc)
5. Frequency pushing (Hz/V) and frequency pulling (Hz p-p)

To achieve optimal circuit performance, many VCO characteristics should be evaluated under varying conditions. For example, a very fundamental parameter is the VCO output frequency versus tuning voltage (F-V). One extension of this parameter is tuning sensitivity (Hz/V), which is the differential of the F-V curve. Ideally this is a constant, but it is not in most cases. The slope change, as a function of frequency, is also very important to know since this is a critical design parameter for the loop filter. [5; 12.]

3.6 Digital PLL Synthesis

Among the many different frequency synthesis techniques, the dominant method used in the wireless communications industry is the digital PLL circuit. While there are some benefits to using other synthesis technique, they are outside the scope of this thesis and will not be discussed.

3.6.1 Integer-N PLL

Compared to the analog techniques used in the frequency synthesis, the modern PLL is now a mostly digital circuit. Figure 16 shows a typical block diagram of PLL implemented with a TCXO reference [6].

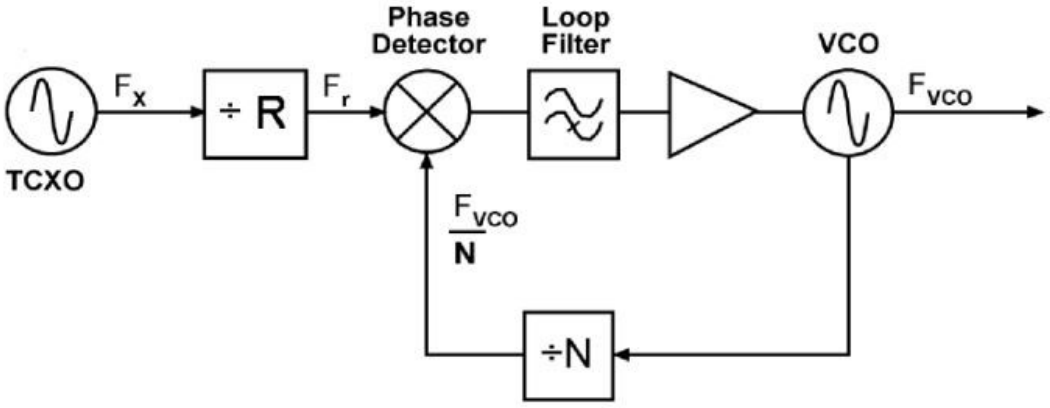

*Figure 16 Integer-N PLL Block Diagram (*Copied from Barrett (1999) [6]).

The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency, F_{VCO}, in terms of the phase detector comparison frequency, F_r [6].

$$F_{VCO} = N \times F_r \tag{37}$$

To achieve this, a reference frequency must be provided to the phase detector. Typically, the TCXO frequency (F_x), is divided down (by R) "on-board" the PLL IC. The phase detector utilizes this signal as a reference to tune the VCO and, in a "locked state," it must be equal to the desired output frequency, F_{vco}, divided by N. [1; 6.]

$$\frac{F_{VCO}}{N} = \frac{F_X}{R} = F_r \tag{38}$$

Therefore, the output frequency that the synthesizer generates, F_{VCO}, can be changed by reprogramming the divider N to a new value. By changing the value N, the VCO can be tuned across the frequency band of interest. The only constraint to the frequency output of the system is that the minimum frequency resolution, or channel spacing, is equal to F_r.

$$Channel\ spacing = \frac{F_{VCO}}{N} = \frac{F_X}{R} \tag{39}$$

When the phase-locked loop is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the difference of the phase value between the two input signals. The error voltage will tune the VCO frequency until the system is in lock state. If the crystal (TCXO) has an accuracy of 1 part-per-million (ppm), the output frequency of the synthesizer has high frequency stability and accuracy to 1 ppm. [6.]

As an example, when F_r = 30 kHz and N = 32000, the only way for this circuit to be in a stable state locked is when F_{VCO} = 960 MHz If N were changed to 32001, a frequency and phase error will develop at the input of the phase detector that will, in turn, retune the VCO frequency until a locked state has been reached. The locked state will be reached when F_{VCO} = 960 MHz and, if the TCXO has an accuracy of 1ppm, the output of the VCO will be accurate to ~ +/- 960 Hz.

3.6.2 Fractional-N PLL

In digital phase-locked loop frequency synthesis an unavoidable situation that almost always arises is that frequency multiplication (by N), raises the signal phase noise by 20Log (N) dB The main source of this noise is the noise characteristics of the phase frequency detector (PFD) active circuitry. Because the PFD are typically the dominant source of close-in phase noise, N becomes a limiting factor when determining the lowest possible phase noise performance of the output signal. A multiplication factor of N = 30,000 will add about 90 dB to the phase detector noise floor. 30,000 is a typical N value used by an integer-N PLL synthesizer for a cellular transceiver with 30 kHz channel spacing. Theoretically the phase noise of the system could be reduced by reducing the value of N but the channel spacing of an integer-N synthesizer is dependent on the value of N. Due to this situation, the phase detectors typically operate at a frequency equal to the channel spacing of the communication system.[6; 7.]

A phase frequency detector (PFD) is a digital circuit that generates high levels of transient noise at its frequency of operation, F_r. This noise is superimposed on the control voltage to the VCO and modulates the VCO RF output accordingly. This interference can be seen as spurious signals at offsets of +/- F_r (and its harmonics) around F_{VCO}. To prevent this unwanted spurious noise, a filter at the output of the charge pumps (called the loop filter) must be present and appropriately narrow in bandwidth. Unfortunately, as the loop filter bandwidth decreases, the time required for the synthesizer to switch between channels increases. [1; 5; 6; 7.]

If N could be made much smaller, F_r would increase and the loop filter bandwidth required to attenuate the reference spurs could be made large enough so that it does not impact the required switching speed of the system. However, the upper limit of F_r is bound by channel spacing requirement. This illustrates how the desire to optimize both switching speed and spur suppression directly conflict with each other. [6.]

Fractional-N PLL technology made it possible to alter the relationship between N, F_r, and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of the phase detector frequency. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and N+1 in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, K/F. This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing. [6.]

$$F_{VCO} = F_r(N + \frac{K}{F}) \tag{40}$$

Where

F = the fractional modulus of the circuit (i.e. 8 would indicate 1/8th fractional resolution.)

K= the fractional channel operation.

3.7 Analog Devices ADF4155 PLL Synthesizer

The ADF4155 PLL synthesizer allows the implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with external loop filter, external voltage controlled oscillator (VCO), and external reference frequency (TCXO). As shown in Figure 17 the ADF4155 have a built-in phase comparator and charge pump logic and many peripheral logic circuits that make it highly reconfigurable device for different applications. [11.]

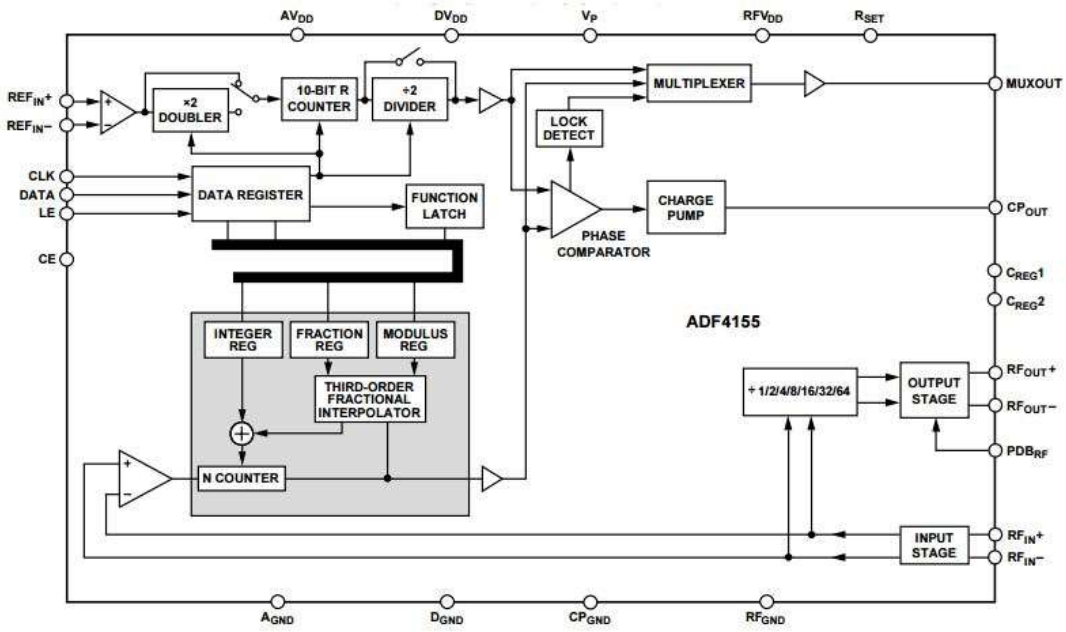

*Figure 17 ADF4155 PLL Functional Block Diagram (*Copied from ADF4155 Datasheet [11]).

The ADF4155 is for use with external voltage controlled oscillator (VCO) parts up to an 8 GHz operating frequency. The high resolution programmable modulus allows synthesis of exact frequencies with 0 Hz error.

The VCO frequency can be divided up to 64 to allow the designer to generate RF output frequencies as low as 7.8125 MHz frequency.

All the on-chip registers are through simple 3-wire interface. The device operates with power supply of 3.3 V and can be powered down when not in use.

3.7.1 Reference Input

The reference input can accept both single-ended and differential signals, and the choice is controlled by the reference input mode bit (Bit DB30, Register 6). When differential signal is used as the input, this bit must be programmed high. When a single-ended signal is used as the reference, Bit DB30 in Register 6 must be programmed to 0.

3.7.2 RF N Counter

The RF N counter allows a division ratio in the PLL which is determined by the INT, FRAC1, MOD1, FRAC2, and MOD2 values. These build up the divider as can be seen in Figure 18.

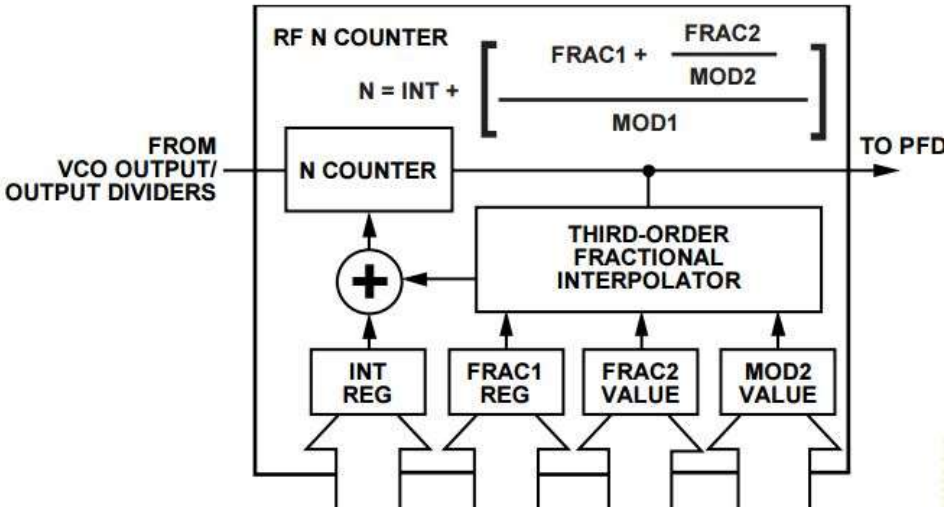

*Figure 18 RF N Counter (*Copied from ADF4155 Datasheet [11]).

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD) frequency [11].

The relation with N can be seen from the equation:

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \tag{41}$$

Where:

INT is the 16-bit integer value (23 to 32,767 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler).

FRAC1 is the numerator of the primary modulus (1-16,777,215).

FRAC2 is the numerator of the 14-bit auxiliary modulus (1-16383).

MOD2 is the programmable, 14-bit auxiliary fractional modulus (2-16,383).

MOD1 is a 24-bit primary modulus with a fixed value of 2^{24} (16,777,216).

If FRAC1 and FRAC2 are zero, then the synthesizer is operating in integer-N mode.

Once the value of N is obtained the RF_{OUT} can be calculated as follows [11]:

$$RF_{OUT} = f_{PFD} \times N \tag{42}$$

$$f_{PFD} = REF_{IN} \times \left[\frac{(1+D)}{R \times (1+T)}\right] \tag{43}$$

Where

REF_{IN} is the reference (TCXO) frequency.

D is the REF_{IN} doubler bit.

R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

T is the REF_{IN} divide by 2 bit (0 or 1).

This results in a very fine frequency resolution with no residual frequency error.

3.7.3 Phase Frequency Detector and Charge Pump

The phase frequency detector takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 19 is a simplified schematic of the Phase Frequency Detector. [3; 11.]

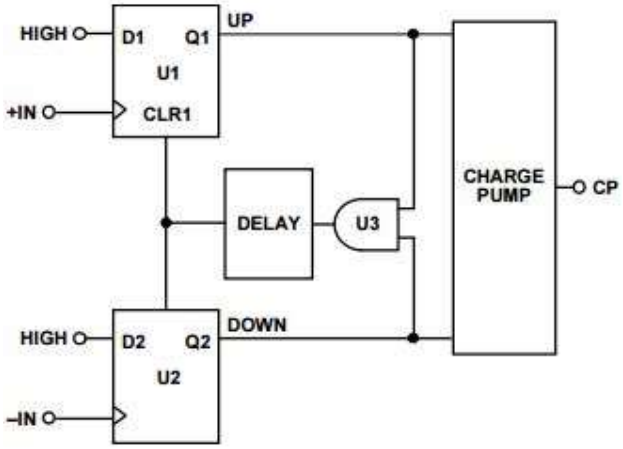

*Figure 19 Simplified PFD Schematic (*Copied from ADF4155 Datasheet [11]).

The PFD includes a fixed delay element that sets the width of the ant backlash pulse (ABP), which is around 2.6 ns. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level.

3.7.4 Output Stage

For optimal spur performance, the ADF4155 datasheet, recommends the use of the VCO output and disable of the RF output -- although the choice is optional. The RF output stage is used where lower frequency operation is required by enabling one of the output dividers.

The RF_{OUT+} and RF_{OUT-} pins of the ADF4155 are connected to the collectors of an NPN differential pair driven by a signal from the RF divider block, as shown in Figure 20.

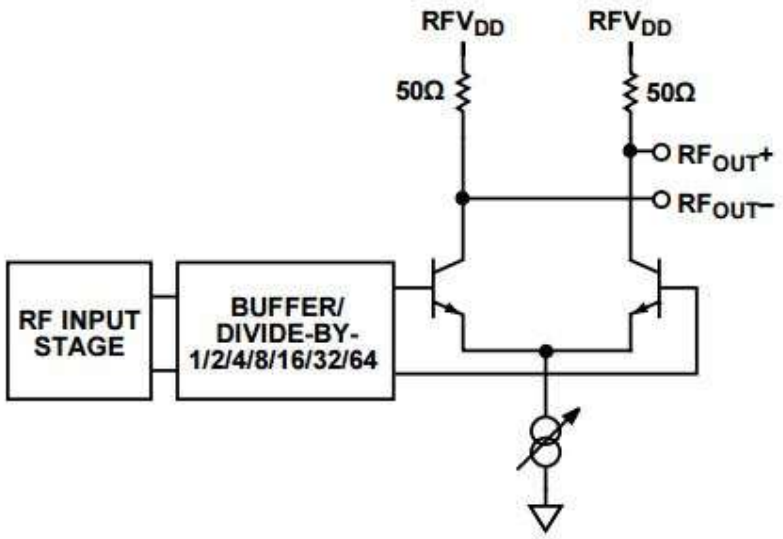

*Figure 20 ADF4155 Output Stage (*Copied from ADF4155 Datasheet [11]).

For optimal output power the tail current of the differential pair is programmable using Bits [DB5:DB4] in Register 6 (R6). Four current levels can be set. These levels give output power levels of -4 dBm, -1 dBm, +2 dBm, and +5 dBm.

The output stage uses an internal 50Ω resistor to RFV_{DD}. An external pull-up inductor to RFV_{DD} is necessary prior to ac coupling into 50Ω load. The output can be combined in a 1 + 1:1 transformer or an 180° microstrip coupler.

Another feature of the ADF4155 is that the supply current to the RF output stage can be shut down until the device achieves lock as measured by the digital lock detect circuitry. This shutdown is enabled by using the mute till lock (MTLD) bit (DB11) in Register 6 (R6).

4 Noise Parameters

In this chapter the focus is basically on one critical specification associated with the designed phase-locked oscillator: *Phase Noise*. The emphasis is placed on what causes them and how they can be minimized in a phase-locked oscillator system.

The instantaneous output of an oscillator may be represented by

$$V(t) = V_o\{1 + A(t)\}\sin\{2\pi ft + \theta(t)\} \quad (44)$$

Where

V_o is the nominal amplitude of the signal

f is the nominal frequency

A(t) represents the amplitude noise of the signal

θ(t) represents the phase noise fluctuation.

4.1 Noise in Voltage Controlled Oscillator

In phase-locked oscillator, frequency stability, both short and long term, is of critical importance Long term frequency stability is concerned with how the output signal varies over a long period of time. It is usually specified as the ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in a dB.

Short term stability is concerned with variations that occur over a period of seconds or less. The term phase noise is used to describe this phenomenon. These variations can be random or periodic. A spectrum analyser is used to examine the short-term stability of a signal. Figure 21 shows a typical spectrum with random and discrete frequency components causing peaks. [1.]

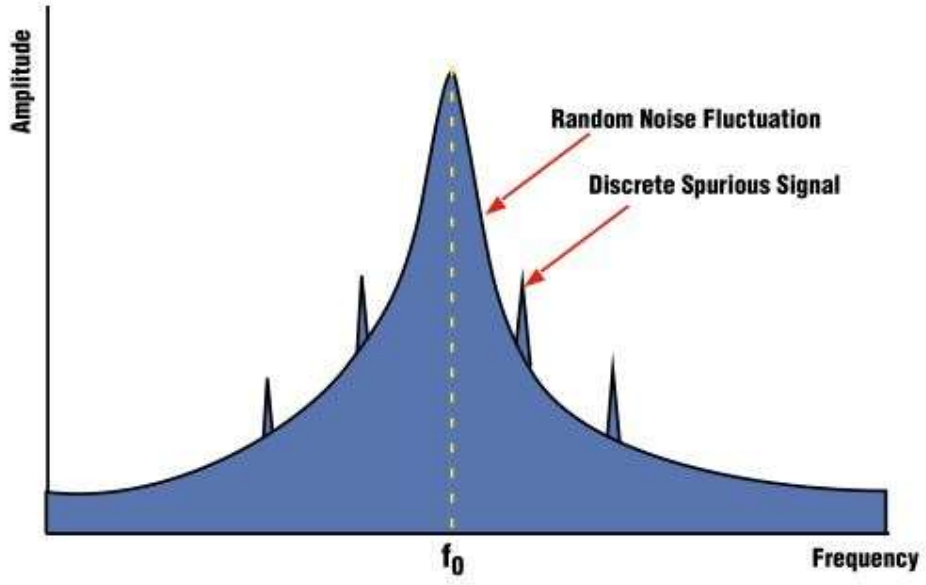

*Figure 21 Phase Noise (*Reprinted from Curtin et al (1999) [1]).

The first, spurious-sidebands, are a form of correlated noise as they have a clear discrete nature and are seen as discrete spikes on both sides of the center frequency. These spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to phase noise. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices. [2.]

An ideal VCO would have no phase noise. Its output as seen on a spectrum analyzer would be a single spectral line. In practice, of course, this is not the case. There will be jitter present at the output in the time domain and a spectrum analyzer would show phase noise. Figure 22 shows phase noise in a phasor representation.

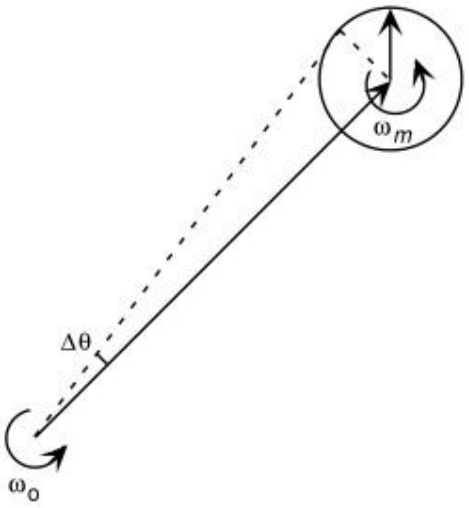

*Figure 22 Phasor representation of phase noise (*Reprinted from Curtin et al (1999) [1]).

ω_o represents an output signal of angular velocity. Superimposed on this is an error signal represented by ω_m. To quantify this error, it is possible to take the rms value of the phase fluctuations and express them as $\Delta\theta$. This is the phase error or jitter and may be expressed in rms picosends (ps rms) or rms degrees (θ rms).

In most communication systems, an overall integrated phase error specification must be met. This overall phase error is made up of the PLL phase error, the modulator phase error and the phase error due to base band components. For example, in GSM the total allowed is 5º θ rms.

4.2 Leeson's Equation

Leeson developed an equation to describe the different noise components in a VCO [2].

$$L_{PM} \approx 10 \times log\left[\frac{FkT}{A}\frac{1}{8Q_L^2}\left(\frac{f_o}{f_m}\right)^2\right] \quad (45)$$

Where:

L_{PM} is single-sideband phase noise density (dBc/Hz)

F is the device noise factor at operating power level A (linear)

k is Boltzmann's constant, 1.38×10^{-23} J/K

T is temperature (K)

A is oscillator output power (W)

Q_L is loaded Q (dimensionless)

f_o is the oscillator carrier frequency

f_m is the frequency offset from the carrier

For Leeson's equation to be valid, the following must be true:

- f_m, the offset frequency from the carrier, is greater than the 1/f flicker frequency.
- the noise factor at the operating power level is known
- the device operation is linear
- Q includes the effects of component losses, device loading and buffer loading.
- a single resonator is used in the oscillator.

In theory, the phase noise power density is made up of equal magnitudes of AM (amplitude-modulated) and PM (phase-modulated) components. This would mean that the total noise power density is twice that given above. However, in practice, PM noise dominates at frequencies close to the carrier and AM noise dominates at frequencies distant from the carrier.

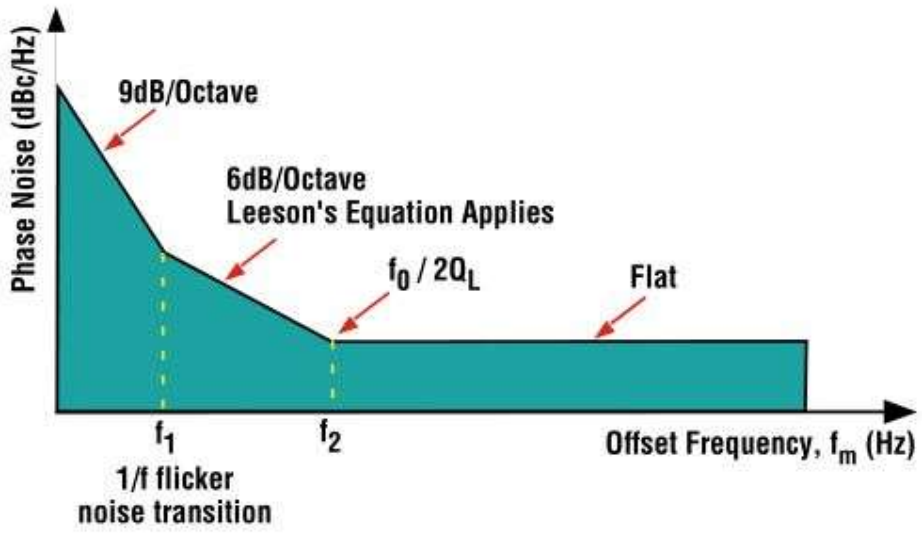

*Figure 23 Phase noise in a VCO vs. frequency offset (*Copied from Curtin et al (1999) [1]).

Leeson's equation only applies in the knee region between the break (f_1) to the transition from the "1/f" flicker noise frequency to a frequency beyond which amplified white noise dominates (f_2). This is shown in Figure 23 [γ=3]. f_1 should be as low as possible; typically, it is less than 1 kHz, while f_2 is in the region of a few MHz. High-performance oscillators require devices specially selected for low 1/f transition frequency.

There are many ways in general to minimize the noise in VCO some of the most common employed techniques are:

1. Use filtering on the dc voltage supply.
2. When buffering the VCO, use devices with the lowest possible noise figure.
3. Maximize average power at the tank circuit output.
4. Keep the tuning voltage of the varactor sufficiently high (typically between 3 and 3.8 V)

4.3 PLO Phase Noise Contributors

Having looked at phase noise in free-running VCO and considered how it can be minimized. The focus is made on the effect of the overall components on phase noise.

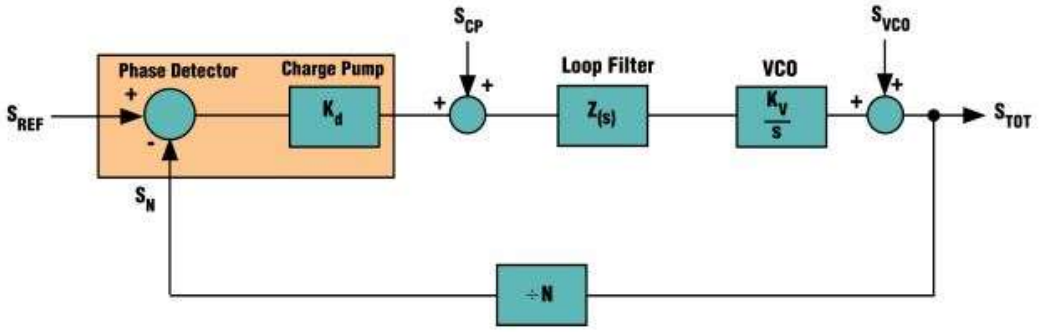

*Figure 24 PLO phase-noise contributors (*Reprinted from Curtin et al (1999) [1]).

Figure 24 shows the main phase noise contributors in a PLL. The system transfer function may be described by the following equations.

$$Closed\ Loop\ Gain = \frac{G}{1 + GH} \tag{46}$$

$$G = \frac{K_d \times K_v \times Z(s)}{s} \tag{47}$$

$$H = \frac{1}{N} \tag{48}$$

$$Closed\ Loop\ Gain = \frac{\left(\frac{K_d \times K_v \times Z(s)}{s}\right)}{1 + \left(\frac{K_d \times K_v \times Z(s)}{N \times s}\right)} \tag{49}$$

S_{REF} is the noise that appears on the reference input to the phase detector. It is dependent on the reference divider circuitry and the spectral purity of the main reference signal. S_N is the noise due to the feedback divider appearing at the frequency input to the phase detector. S_{CP} is the noise due to the charge pump of the phase detector. And S_{VCO} is the phase noise of the VCO as described by equations developed earlier.

The overall phase noise performance at the output depends on the terms described above. All the effects at the output are added in a root mean square fashion to give the total noise of the system. Hence [1.]

$$S_{TOT}^2 = X^2 + Y^2 + Z^2 \tag{50}$$

Where:

S_{TOT}^2 is the total phase noise power at the output

X^2 is the noise power at the output due to S_N and S_{REF}.

Y^2 is the noise power at the output due to $S_{CP.}$

Z^2 is the noise power at the output due to $S_{VCO.}$

The noise terms at the PD inputs, S_{REF} and S_N, will be operated on in the same fashion as S_{REF} and will be multiplied by the closed loop gain of the system.

$$X^2 = (S_{REF}^2 + S_N^2) \times \left(\frac{G}{1+GH}\right)^2 \tag{51}$$

At low frequencies, inside the loop bandwidth,

$$GH \gg 1 \text{ and } X^2 = (S_{REF}^2 + S_N^2) \times N^2 \tag{52}$$

At high frequencies, outside the loop bandwidth,

$$G \ll 1 \text{ and } X^2 \to 0 \tag{53}$$

The overall output noise contribution due to the phase detector noise, S_{CP}, can be calculated by referencing S_{CP} back to the input of the PFD. The equivalent noise at the PD input is S_{CP}/K_d. This is then multiplied by the closed-loop gain:

$$Y^2 = S_{CP}^2 \times \left(\frac{1}{K_d}\right)^2 \times \left(\frac{G}{1+GH}\right)^2 \tag{54}$$

Finally, the contribution of the VCO noise, S_{VCO}, to the output phase noise is calculated in a similar manner. The forward gain this time is 1. Therefore its contribution to the output noise is:

$$Z^2 = S_{VCO}^2 \times \left(\frac{1}{1+GH}\right)^2 \tag{55}$$

G, is the forward loop gain of the closed loop response, is usually a low pass function; it is very large at low frequencies and small at high frequencies. H is a constant, 1/N. The denominator of the above expression is therefore low pass, so S_{vco} is actually high-pass filtered by the closed loop.

5 Design Task

The design task involves the design of the loop filter in the first part and in the later part designing a 1.45 GHz L Band signal.

5.1 Loop Filter Design

This section presents the many technical issues that are involved with the loop filter design. Loop filter design usually involves choosing the proper loop filter topology, loop filter order, phase margin, loop bandwidth, and pole ratios. Once all these parts are chosen, the poles and zeros of the filter can be determined which will lead that the loop filter components to be easily calculated. This section presents the fundamental principles that are prerequisite for understanding loop filter design. [7.]

5.1.1 Loop Filter Topology and Order

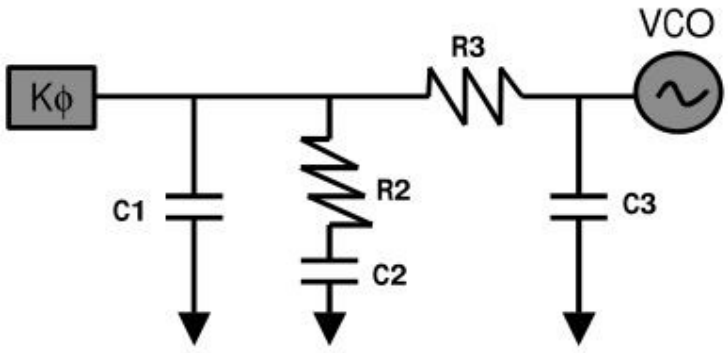

*Figure 25 A Third Order Passive Loop Filter (*Copied from Banerjee (2001) [7]).

Passive loop filters, such as one shown in Figure 25, are widely employed in PLL loop filter design for simplicity and because they have less phase noise, complexity, and cost than the active loop filters. However, active filter is sometimes necessary when, for example, the maximum PLL charge pump voltage is lower than the VCO tuning voltage. If higher tuning voltages are applied to the VCO then the phase noise can be reduced.

In terms of filter order, the most basic is the second order filter. Additional low pass filtering stages can be added to reduce the reference spurs. In Figure 25, R3 and C3 form an additional low pass filtering stage.

5.1.2 Phase Margin, Loop Bandwidth, and Pole Ratios

The phase margin (θ) relates to the stability of the system. This value is typically between 40 and 55 degrees. Practically a phase margin of about 48 degrees gives the optimal lock time. Higher phase margins have the effect of decreasing the peaking response of the loop filter at the expense of degrading the lock time. [5; 7.]

The loop bandwidth (ω_c), on the other hand, is the most critical parameter of the loop filter. Making the loop bandwidth too small will result a design with improved reference spurs rejection and RMS phase error. The most practical method is to choose the loop bandwidth that it is sufficient to meet the lock time requirement with sufficient margin. If there is no lock time requirement, then choosing the loop bandwidth at the frequency where the PLL noise equals the VCO noise is recommended for optimal RMS phase error design. [7.]

The pole ratios (*T31, T41, ..*) have less impact on the design than the loop bandwidth, but still are important. They tell the ration of each pole, relative to the pole T1, for example:

$$T1 = T11 \cdot T1 \tag{56}$$

$$T3 = T31 \cdot T1 \tag{57}$$

$$T4 = T41 \cdot T1 \tag{58}$$

Where:

T1 is trivial and always equal to 1.

Choosing all pole ratios to be one is theoretically the lowest reference spur solution. However, choosing them smaller can make sense when the capacitor in the loop filter next to the VCO is not at least three times the VCO input capacitance (typically 10 -100 pF).

5.1.3 Loop Filter Transfer function and Open Loop Gain

The loop filter transfer function, impedance, is defined as the ratio of the output voltage at the VCO to the current injected at the PLL charge pump. The loop filter transfer function is shown below. [7.]

$$Z(s) = \frac{1 + s \cdot T2}{Ctot \cdot s \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \tag{59}$$

Table 1 shows the loop transfer function the poles and for various filter orders.

Table 1 Transfer Functions for Various Filter Orders [7]

Parameter	2nd Order Filter	3rd Order Filter	4th Order Filter
T1	$\frac{R2 \cdot C2 \cdot C1}{Ctot}$	$\frac{R2 \cdot C2 \cdot C1}{Ctot}$	$\frac{R2 \cdot C2 \cdot C1}{Ctot}$
T2	$R2 \cdot C2$	$R2 \cdot C2$	$R2 \cdot C2$
T3	0	$R3 \cdot C3$	$R3 \cdot C3$
T4	0	0	$R4 \cdot C4$
Ctot	$C1 + C2$	$C1 + C2 + C3$	$C1 + C2 + C3 + C4$

Once the transfer function Z(s), charge pump gain ($K\phi$), and VCO gain (K_{vco}) are known, then the open loop gain G(s) can be obtained as follows:

$$G(s) = \frac{K\phi \cdot K_{vco}}{s} \cdot Z(s) \tag{60}$$

5.1.4 Time Constants Derivation

The phase margin is specified as 180 degrees plus the open loop gain divide by N. Hence,

$$\phi = 180 + \arctan(\omega c \cdot T2) - \arctan(\omega c \cdot T1) - \arctan(\omega c \cdot T1 \cdot T31) - \arctan(\omega c \cdot T1 \cdot T41) \tag{61}$$

Since the ϕ and the pole ratios are known, this can be simplified to an expression involving T1 and T2. A second expression involving T1 and T2 can be found by setting the derivative of the phase margin equal to zero at the frequency equal to the loop bandwidth. This maximizes the phase margin at this frequency. [7.]

$$\left.\frac{d\phi}{d\omega}\right]_{\omega=\omega c} = 0 = \frac{\omega c \cdot T2}{1 + \omega c^2 \cdot T2^2} - \frac{\omega c \cdot T1}{1 + \omega c^2 \cdot T1^2} - \frac{\omega c \cdot T1 \cdot T31}{1 + \omega c^2 \cdot T1^2 \cdot T31^2} - \frac{\omega c \cdot T1 \cdot T41}{1 + \omega c^2 \cdot T1^2 \cdot T41^2} \tag{62}$$

The above preceding two equations represent a system of two equations with two unknowns (T1 and T2). The system can be solved numerically in the case of a second order filter (T3=T4=0), an elegant closed form solution exists.

5.1.5 Component Values Calculation from Time Constants

This will be discussed in depth in the coming section about implementing the loop filter. However, one thing that arises, regardless of filter order, is the total capacitance. This is the sum of all the capacitance values in the loop filter. Considering, for instance, a delta current spike it should be natural that in the long term, the voltages across all the capacitors should be the same and that its voltage would be the same as if all four capacitors values were added together.

C_{tot} can be found by setting the forward loop gain G(s) equal to one at the loop bandwidth.

$$C_{tot} = \frac{K_\phi \cdot K_{vco}}{N \cdot \omega c^2} \cdot \sqrt{\frac{(1 + \omega c^2 \cdot T2^2)}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \tag{63}$$

The input capacitance of the VCO usually becomes an issue with third and higher order loop filter designs, because the capacitor shunt with the VCO should at least three times the VCO input capacitance to keep it from distorting the performance of the loop filter.

The concepts and formulas presented in this section will form the basis for the implementation of the loop filter in the coming section. The second order loop filter is the case when T3=T4=0. The third order loop filter is the case when T3>0 and T4=0. These formulas could be generalised for filters higher than fourth order if required. [7.]

5.2 Loop Filter Component Values Calculation

The order of the system is usually defined as one plus the number of poles in the loop filter. The reason for doing higher order filter designs is reduced spur levels. Fourth order and higher order loop filters become more practical when the spur to be filtered is at least 20 times the loop bandwidth. [5; 7.]

In higher order loops, generally greater than three, finding the exact solution for time constants is generally difficult. The standard method can be used to calculate the time constants, but approximations will be introduced to solve for the component values. For the design of a fourth order loop filter it is necessary that the loop bandwidth, ωc, phase margin, ϕ, pole ratio T31, and pole ratio T41 be specified.

5.2.1 Circuit Topology

A fourth order passive loop filter is shown in Figure 26. Higher order loop filters are possible by adding additional RC filters.

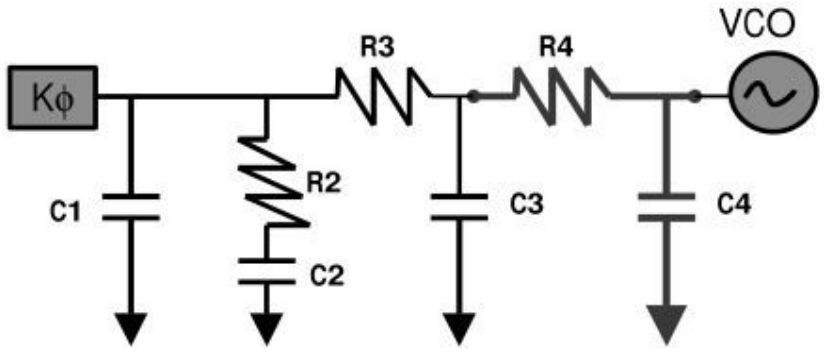

*Figure 26 Fourth Order Passive Loop Filter (*Reprinted from Banerjee (2001) [7]).

5.2.2 Loop Transfer Function and Time Constant Derivation

The loop filter transfer function for the fourth order loop filter is given below:

$$Z(s) = \frac{1 + s \cdot C2 \cdot R2}{s \cdot (A \cdot s^3 + B \cdot s^2 + C \cdot s + D)} \tag{64}$$

$$= \frac{1 + s \cdot T2}{s \cdot Ctot \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \tag{65}$$

Where:

$$Ctot = C1 + C2 + C3 + C4 \tag{66}$$

$$T2 = R2 \cdot C2 \tag{67}$$

$$A = C1 \cdot C2 \cdot C3 \cdot C4 \cdot R2 \cdot R3 \cdot R4 \tag{68}$$

$$B = C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2) \tag{69}$$

$$C = C2 \cdot R2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + R4 \cdot C4 \cdot (C1 + C2 + C3) \tag{70}$$

$$D = Ctot \tag{71}$$

$$T1 = \frac{R2 \cdot C2 \cdot C1}{Ctot} \tag{72}$$

$$T3 \approx R3 \cdot C3 \tag{73}$$

$$T4 \approx R4 \cdot C4 \tag{74}$$

For the k[th] order loop filter, the transfer function and time constants are:

$$Z(s) = \frac{(1 + s \cdot T2)}{s \cdot Ctot \cdot (1 + s \cdot T1) \cdot \prod_{i=3}^{k} (1 + s \cdot T_i)} \tag{75}$$

Where:

$$T1 \approx R2 \cdot C2 \cdot \frac{C1}{Ctot} \tag{76}$$

$$T2 = R2 \cdot C2 \tag{77}$$

$$T_i = R_i \cdot C_i \quad i = 3,4, \ldots k \tag{78}$$

The above equations are good approximations of exact values, although the time constants of the loop filter have been approximated. These approximations hold true as long as:

$$C_i \ll C1 \tag{79}$$

$$I \ll \left(\frac{C_i}{C_{i+I}}\right) + \left(\frac{R_{i+I}}{R_i}\right) \qquad i = 3,4,\dots k \tag{80}$$

One possible way to ensure that the above constraints are satisfied is to choose:

$$T_i \gg 2 \cdot T_{i+1} \tag{81}$$

The time constant can be calculated assuming the phase margin is given by:

$$\phi = 180 + \arctan(\omega c \cdot T2) - \arctan(\omega c \cdot T1) - \prod_{i=3}^{k} \arctan(\omega c \cdot T_i) \tag{82}$$

From the Taylor series analysis, for small value of *x* it can be shown:

$$\tan(x) \approx x \tag{83}$$

$$\arctan(x) \approx x \tag{84}$$

Applying the tangent function and the two previous identities yields the following simplification:

$$T1 + \sum_{i=3}^{k} T_i \approx \frac{\sec(\phi) - \tan(\phi)}{\omega c} \tag{85}$$

As a design constraint itself the phase margin is maximized at the loop bandwidth. Making the derivative of the phase margin equal to zero yields:

$$\frac{T2}{1 + \omega c^2 \cdot T2^2} = \frac{T1}{1 + \omega c^2 \cdot T1^2} + \sum_{i=3}^{k} \frac{T_i}{1 + \omega c^2 \cdot T_i^2} \tag{86}$$

Cross multiplying both sides and applying some approximations yields:

$$T2 \approx \omega c^2 \cdot T2^2 \cdot \left(T1 + \sum_{i=3}^{k} T_i\right) \tag{87}$$

This simplification can be justified as long as:

$$T2 \gg T1 + \sum_{i=3}^{k} T_i \tag{88}$$

Rearranging the equations yields the following:

$$T2 \approx \frac{1}{\omega c^2 \cdot (T1 + \sum_{i=3}^{k} T_i} \tag{89}$$

$$T1 + \sum_{i=3}^{n} T_i \frac{\sec(\phi) - \tan(\phi)}{\omega c} \tag{90}$$

In the case of fourth order loop filter and to satisfy the $T_i \geq 2 * T_{i+1}$, the time constants can be obtained:

$$T1 = \frac{4}{7} \cdot \frac{\sec(\phi) - \tan(\phi)}{\omega c} \tag{91}$$

$$T_3 = T3 = \frac{2}{7} \cdot \frac{\sec(\phi) - \tan(\phi)}{\omega c} \tag{92}$$

$$T_4 = T4 = \frac{1}{7} \cdot \frac{\sec(\phi) - \tan(\phi)}{\omega c} \tag{93}$$

5.2.3 Calculating Component Values from the Time Constants

Once the time constants are known, the other components can be calculated

$$Ctot = \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot \prod_{i=3}^{k} \left(1 + \omega c^2 \cdot T_i^2\right)}} \tag{94}$$

$$C1 = Ctot \cdot \frac{T1}{T2} \tag{95}$$

$$C3 = \frac{C1}{5} \tag{96}$$

$$C4 = \frac{C3}{5} \tag{97}$$

$$C_{i+1} = \frac{C_i}{5} \; i = 4,5,6..(zero\ if\ the\ filter\ order\ is\ four\ or\ less) \tag{98}$$

$$C2 = Ctot - C1 - C3 - C4 - \sum\nolimits_{i=5,6,7,..} C_i \tag{99}$$

$$R2 = \frac{T2}{C2} \tag{100}$$

$$R3 = \frac{T3}{C3} \tag{101}$$

$$R4 = \frac{T4}{C4} \tag{102}$$

$$C_i = \frac{T_i}{C_i} \; i = 4,5,6..(zero\ if\ the\ filter\ order\ is\ four\ or\ less) \tag{103}$$

The components can be more precisely calculated by writing explicitly the impedance for the components R3, R4, C3, and C4 and solving for the time constants T3 and T4 more exactly. This approximation is similar to putting an operational amplifier before R3, except for the time constant T1 still takes into account the loading from the rest of the components of the loop filter.

The components C1, C2, C3 and R2 are calculated as normal, however, the components R3, R4 and C4 are found more exactly by equating the poles to the expressing for the loop filter impedance. The voltage transfer function from the beginning of resistor R3 to the input of the voltage controlled oscillator (VCO) is:

$$\frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + R3 \cdot C4) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4} = \frac{1}{(1 + s \cdot T3) \cdot (1 + s \cdot T4)} \tag{104}$$

Processing this arithmetic gives the values for R3 and R4.

$$R3, R4 = \frac{T3 + T4 \mp \sqrt{(T3 + T4)^2 - 4 \cdot T3 \cdot T4 \cdot \left(1 + \frac{C4}{C3}\right)}}{2 \cdot (C3 + C4)} \tag{105}$$

For real component values, the quantity under the square root sign must be non-negative. Applying this restriction yields:

$$\frac{C4}{C3} \leq \frac{(T3 - T4)^2}{4 \cdot T3 \cdot T4} \tag{106}$$

As a rule of thumb, it is desirable to have C4 as large as possible, so this quantity should be made equal. T3 should be larger than T4, that is T31 > T41, so that the capacitor C3 is not zero and it is at least three times larger as the input capacitor of the voltage controlled oscillator (VCO). Taking account into this gives us:

$$C4 = C3 \cdot \frac{(T3 - T4)^2}{4 \cdot T3 \cdot T4} \tag{107}$$

$$R3 = R4 = \frac{T3 + T4}{2 \cdot (C3 + C4)} \tag{108}$$

Using the equations derived above now it is very trivial to design a simple passive loop filter. This is accomplished by knowing the K_{VCO}, $K\phi$, $F_{OUT,}$ $F_{COMP,}$ and F_C.

The loop filter designed here has the following values that can be used to calculate the values of loop components.

$$K_{VCO} = 85 \ \frac{MHz}{volt}$$

$$K_{\phi} = 0.9 \ mA$$

$$F_{OUT} = 900 \ MHz$$

$$F_{COMP} = 61.44 \ MHz$$

$$F_C = 80 \ kHz$$

Applying the above equations and the values given. The component values for specific frequency and phase detector values can be calculated. In this case, using MathCAD software, the obtained values of the loop components are:

Table 2 Loop Filter Component Values

Loop Component	Value
C1	3.128 nF
C2	55.192 nF
C3	0.626 nF
R2	99.035 Ω
R3	308.689 Ω
R4	308.689 Ω
C4	78.19 pF

The MathCAD code used in the calculation is shown in Appendix 1.

The final loop filter topology is shown in Figure 27.

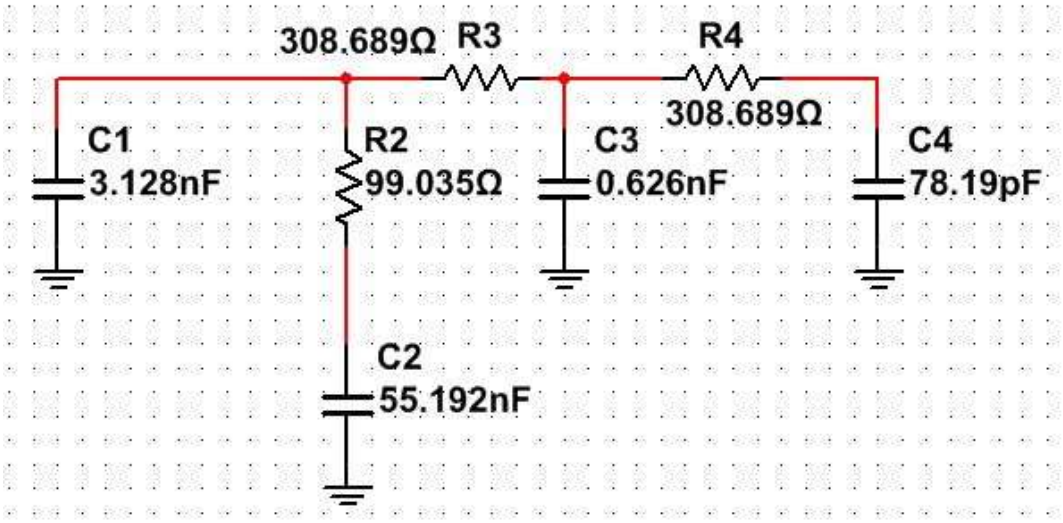

Figure 27 Fourth Order Loop Filter with 80 kHz Loop Bandwidth

5.3 1.45 GHz L-Band signal generation

The phase-locked oscillator discussed can be used to generate a wide range of frequency signals. To showcase this process an L-Band signal of 1.45 GHz frequency is generated and measurement of phase noise is done in the following chapter.

The output frequency of the synthesizer can be calculated as follows [11]:

$$RF_{OUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right) \times \frac{f_{PFD}}{RF\ Divider} \tag{109}$$

where:

RF_{out} is the RF frequency output.

INT is the integer division factor.

FRAC1 is the 24-bit main fractional value.

FRAC2 is the 14-bit auxiliary fractional value.

MOD2 is the 14-bit auxiliary modulus value.

MOD1 is the 24-bit fixed modulus value.

RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times \left[\frac{(1+D)}{(R \times (1+T)}\right] \quad (110)$$

where:

REF_{IN} is the reference frequency input.

D is the reference doubler.

R is the reference division factor.

T is the reference divide by 2 bit (0 or 1).

Assuming a channel spacing of 15 kHz. This value and the phase frequency detector frequency value specify the MOD2 value.

Table 3 1.45 GHz RF Frequency Synthesis Parameters

N	INT	FRAC1	FRAC2	MOD1	MOD2
	94	10824362	683	2^{24}	1024
f_{PFD}	REF_{IN}	D	R	T	
	122.88 Mhz	0	2	0	
$RF_{divider}$	4				
RF_{OUT}	N		f_{PFD}		
	94.645		61.44 MHz		

The equations used to obtain the values shown in Table 3 are presented in Appendix 2.

5.4 System Simulation

The simulation of the system is done using ADIsimPLL. This software makes it easy to design, analyse and simulate the Phase Locked Loop frequency synthesizers using the ADF range of PLL integrated circuits from Analog Devices.

The performance including phase noise, transient response, and lock time to frequency, and phase tolerance is analysed.

The ADIsimPLL is configured to simulate the noise contributions from each component in the loop except the reference crystal. The frequency simulated is in the range of 1.452 – 1.492 GHz. This covers the amateur communication band for Region 1.

5.4.1 Frequency Domain

In the frequency domain the open loop gain and the closed loop gain response of the system are presented.

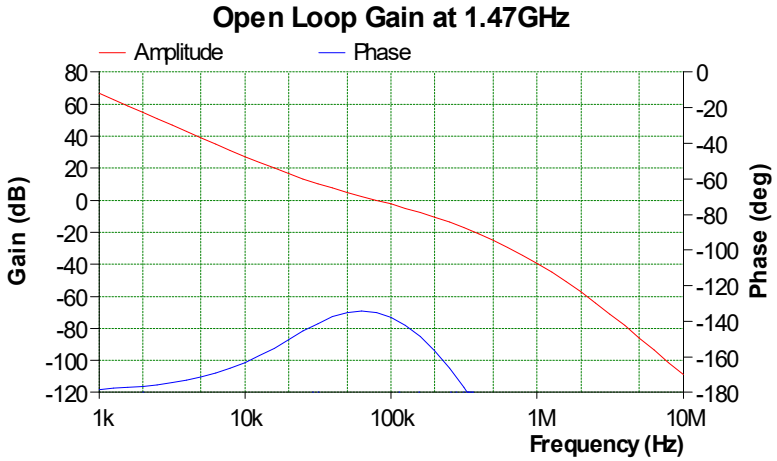

Figure 28 Open Loop Gain at 1.47 GHz Simulated with ADIsimPLL,

Figure 28, also called Phase Margin plot, is useful for analyzing the stability of the system. If the $|G_{ol}(j\omega)| = 0\ dB$ when $\measuredangle G_{ol}(j\omega) = -180^o$ this equals $G_{ol}(j\omega) = -1$ which makes the loop, or system in general, unstable. The Phase Margin tells how far the design is from the instability, usually around 45°.

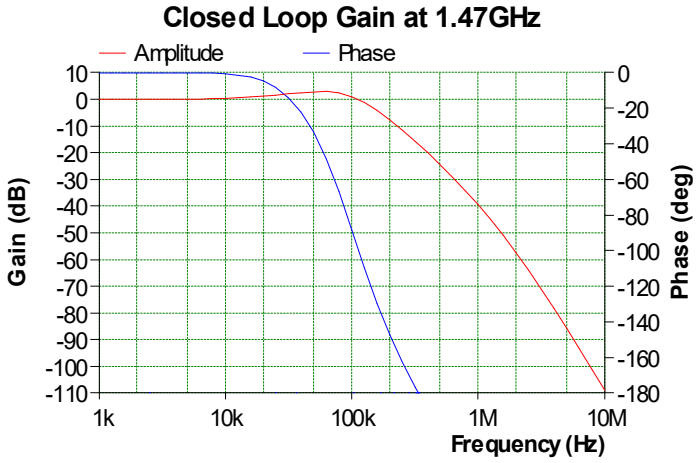

Figure 29 Closed Loop Gain at 1.47 GHz simulated with ADIsimPLL

The Closed Loop Gain in Figure 29 above has a low pass nature. It shows how the noise from the reference or the phase detector is handled by the loop. The noise of the reference oscillator is multiplied by N^2 within the loop bandwidth and shaped by the closed loop response of the Phase Locked Loop (PLL).

At the frequency domain the phase noise contribution of each component is simulated and the overall phase noise of the system.

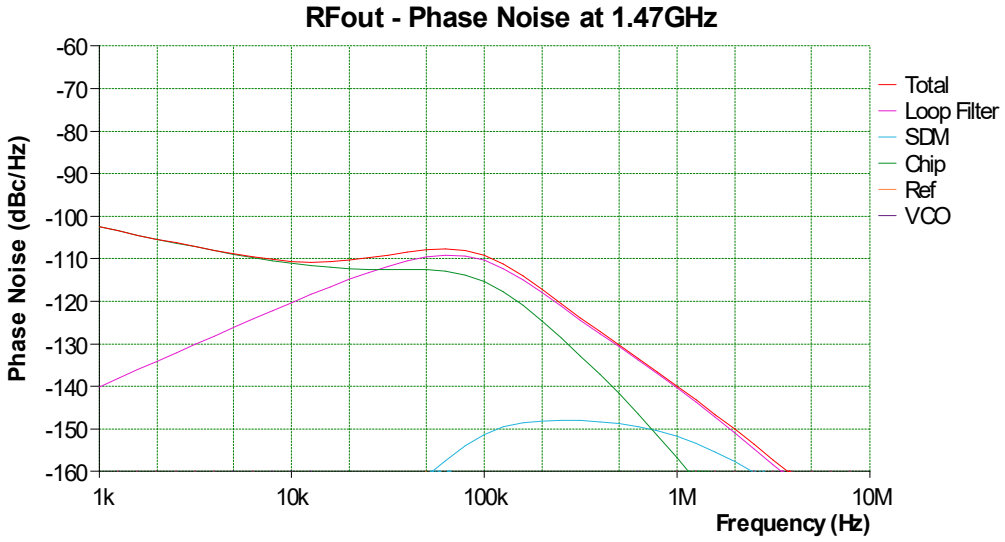

Figure 30 Phase Noise Characteristics of the System simulated with ADIsimPLL

Although the phase noise can be guessed from the graph shown in Figure 30 the ADIsimPLL software can be configured to generate a table at specific offset frequencies.

Table 4 Phase Noise Simulation at 10k, 100k, and 1.0M offset frequency

Offset Frequency	Phase Noise (dBc/Hz)
10.0k	-110.6
100k	-109.1
1.00M	-139.9

5.4.2 Time Domain

Two important parameters are the frequency settling time and output phase error. Both are useful in the simulation phase because the system can be optimized accordingly to meet the requirements of certain standards.

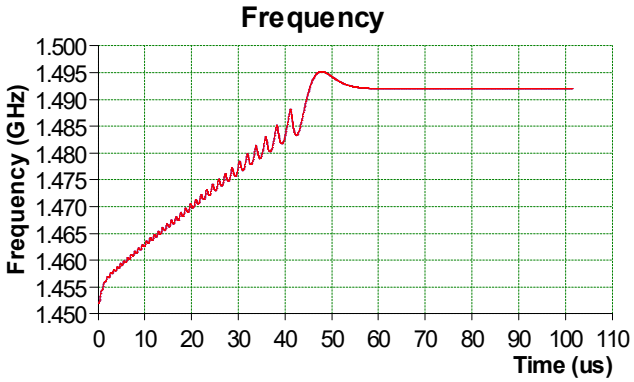

Figure 31 Frequency settling time of the system simulated with ADIsimPLL

Figure 31 shows the VCO frequency for the default frequency transient from 1.455 GHz to 1.495 GHz. Tuning the Loop Bandwidth in ADIsimPLL it possible to simulate its effect on the system by analyzing the graph. In other words, the wider the loop bandwidth the faster the settling time. Most of the time the optimum phase margin from settling time point of view is about 45-50 degrees that will result in an overshoot of step response of about 30-35%. Making the phase margin smaller results slowing the settling time considerably.

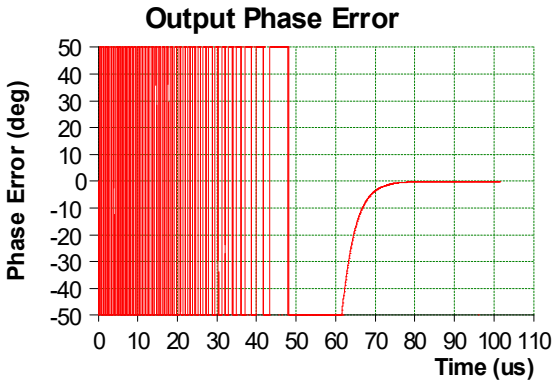

Figure 32 Output Phase Error of the system simulated with ADIsimPLL

From Figure 32 it can be deduced that the phase gets to within 10 degrees of the final value within 65.3 µs.

6 Measurement

6.1 Phase Noise Measurements

The phase noise of an oscillator is a measure of the oscillator's short-term stability and hence an essential quality criterion when designing a phase locked oscillator. Special

phase noise measurement equipment such as Signal Source Analyser or Spectrum analyser when the requirements on the dynamic range are not stringent.is used for doing the measurement.[14.]

Phase noise measurement with a spectrum analyser is referred to as a direct measurement. The Device under Test (DUT) must have a small frequency drift relative to the sweep time of the spectrum analyser or the measurable frequency variation of the oscillator would be too large and invalidate the measurement results. This case does not apply to the design task of the thesis since the frequency is phase-locked which prevents frequency drifting at all most of the time. But when free running voltage controlled oscillator (VCO) phase noise is measured it is better to employ another technique of measurement.

6.1.1 Measurement procedure

For phase-locked oscillators the Single Sideband (SSB) phase noise at certain offset frequency relative to the carrier level within 1 Hz bandwidth is usually of interest. The unit is dBc(1 Hz).

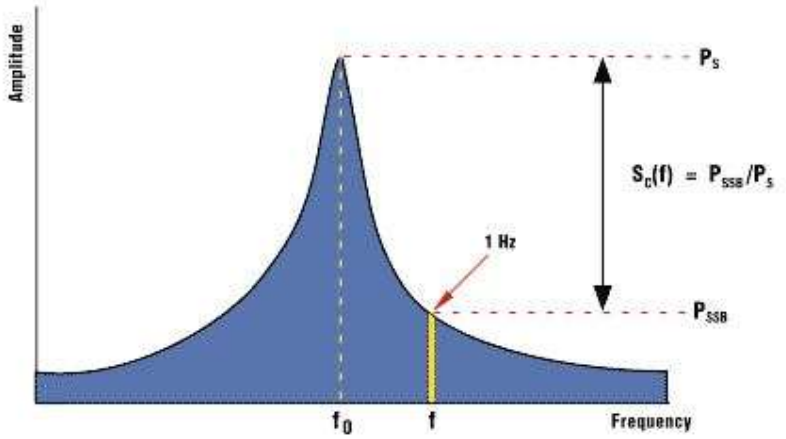

*Figure 33 Single Sideband phase noise (*Reprinted from Curtin et al (1999) [1]).

Phase noise measurement with spectrum analyzer involves two steps:

- Measurement of carrier level L_C.
- Measurement of phase noise level L_{PN} at carrier offset f_{off}.

For evaluating the phase noise measured at a carrier offset f_{off} and resolution bandwidth B is first referenced to a 1 Hz bandwidth. The following equation relates the two when a spectrum analyzer utilizing a RMS detector is used [14]:

$$L_{PN,f_{off}}(dB) = L_{PNM,f_{off}}(dB) - 10 \times log\left(\frac{B}{1\ Hz}\right) \quad (111)$$

Where

$L_{PN,f_{off}}$ phase noise level at carrier offset f_{off} and noise bandwidth B relative to 1 dB and 1 Hz bandwidth.

$L_{PNM,f_{off}}$ phase noise level measured at carrier offset f_{off} and noise bandwidth B relative to 1 dB.

B noise bandwidth of resolution filter.

The phase noise level within 1 Hz bandwidth must now be referenced to the carrier level:

$$L_{f_{off}}(P_c) = L_c(dB) - L_{PN,f_{off}}(dB) \quad (112)$$

Where

$L_{f_{off}}$ relative phase noise level within 1 Hz bandwidth at carrier offset f_{off} relative to carrier power P_c.

$L_{PN,f_{off}}$ phase noise level at carrier offset f_{off} and noise bandwidth B relative to 1 dB and 1 Hz bandwidth.

L_c carrier level relative to 1 dB.

For noise measurement with modern Spectrum Analysers and/or Signal Analysers that have noise marker functionality which takes into account all the calculations and displays the noise level at the marker point at offset frequency. During the measurement this feature will be utilized.

6.1.2 Measurement Setup

The phase noise measurement is done using Rohde & Schwarz Signal Analyser FSIQ3. Phase noise measurement is made using the phase noise soft-key at specific offset frequency of interest.

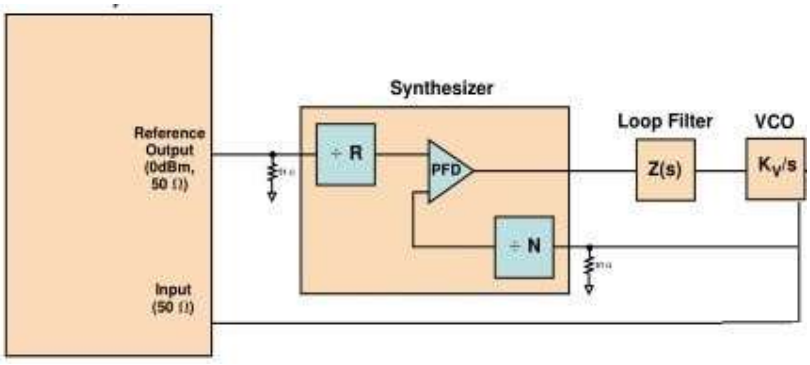

*Figure 34 PLO Measurement Setup with Rohde&Schwarz FSIQ3 Signal Analyzer (*Modified from Curtin et al (1999) [1]).

6.1.3 Measured Phase Noise Values

The measurement is done as shown in Figure 34. The measured values are compared with the values obtained from the ADIsimPLL simulation and presented in Table 4.

Table 5 Phase Noise Measurement at 10 kHz, 100 kHz, and 10 MHz offset frequency

Offset Frequency	Phase Noise (dBc/Hz)
10.0k	-90.30
100k	-92.62
1.00M	-94.12

The spectrum analyser images and ADF4155 connection is shown in Appendix 3.

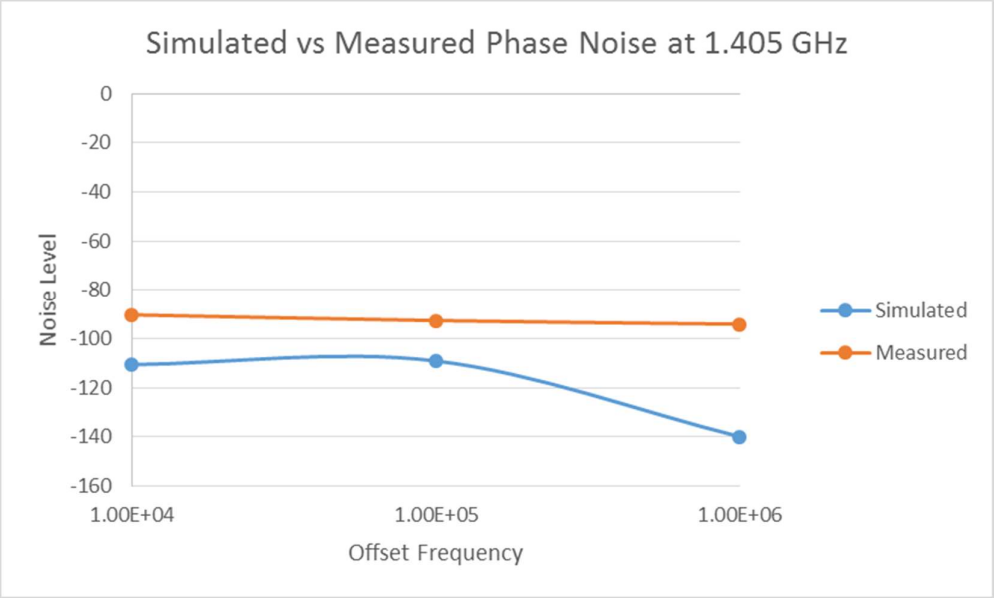

Figure 35 Simulated vs Measured Phase Noise at 1.405 GHz at 10kHz, 100kHz, and 1 MHz offset from carrier.

7 Discussion

The goal of this thesis was to design and investigate the feasibility of frequency synthesis system to be used in conjunction with the Radio Electronics course. The design of the loop filter was simulated but not implemented because the ADF4155 Evaluation Board comes with all the required components to implement a frequency synthesis system.

The system generates the programmed frequencies effectively with required power level which is also programmable. The measurement results obtained in Section 6.1.3 are not exactly as the designed values. This is because there are many challenges involved when precise phase noise measurements are required. The method used for measuring

the noise values is the Direct Method which is the easiest method since the only thing required is spectrum or signal analyser equipment and hence results in poorer phase noise measurement.

Another thing that may be the reason for the discrepancy between the simulated and measured phase noise is the simulated Voltage Controlled Oscillator (VCO) phase noise. The ADIsimPLL does not support the ZComm VCO used hence the phase noise parameters were approximated. Although the reference oscillator is stable the phase noise was also not simulated therefore that may contributing to the discrepancy between measured and the simulated values.

The power source for the board was taken from the Lab supply bench which may contribute also to the overall noise of the system. Moreover, to ensure good performance the input signal levels to the Signal Analyser mixers need to be controlled carefully to avoid intermodulation products. This limits the wide band signal to noise ratio of the Signal Analyser which eventually will limit phase noise measurements that can be performed far from the carrier. The filters also sometimes limit the capability of the measurement.

The system measurement may be improved by using other measurement techniques such as the Delay Line Discriminators, Quadrature Technique, and Digital Direct Measurement. All these measurements are more accurate than the Direct Method used in the measurement phase.

8 Conclusion

In this thesis the phase locked oscillator was analysed, designed, and measured by utilising the ADF4155 Evaluation board. The loop filter design was emphasised during the design phase and was analysed mathematically. A fourth order loop filter was designed and analysed with MathCAD software.

For generating the desired signal the Fractional-N Phase Locked Loop technique was employed which offers the generation of various frequencies than the Integer-N method by using delta-sigma modulators to control the division of the feedback signal.

Phase noise measurement was made at the end and the values obtained were compared with the simulated values. The results were very close, in terms of frequency, to the simulated values. A 1.45 GHz L Band signal was designed and measured as part of the thesis work.

The goal of the thesis work, which was to design a tunable phase locked oscillator was successfully achieved, and the phase locked oscillator can be used when a high spectral purity signal is required.

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MathCAD Code for Loop Filter Calculation

$Kvco := 85\frac{MHz}{volt}$

$K\phi := 0.9mA$

$Fout := 900MHz$

$Fcomp := 61.44MHz$

$Fc := 80kHz$

$\phi := 50deg$

$T31 := 1.0$

$T41 := 0.5$

Calculation

$N1 := \frac{Fout}{Fcomp}$

$\omega c := 2\pi \cdot Fc$

Calculate Pole and Zero

$$T1 := \left(\frac{\frac{1}{\cos(\phi)} - \tan(\phi)}{\omega c}\right) \cdot \left(\frac{1}{1 + T31 + T41}\right)$$

$T3 := T1 \cdot T31$

$T4 := T41 \cdot T1$

$$T2 := \frac{1}{\left[\omega c^2 \cdot (T1 + T3 + T4)\right]}$$

$T1 = 2.896 \times 10^{-7} s$

$T2 = 5.466 \times 10^{-6} s$

$T3 = 2.896 \times 10^{-7} s$

$T4 = 1.448 \times 10^{-7} s$

Calculate component values from time constants

$$Ctot := \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N1} \cdot \left[\frac{1 + \omega c^2 \cdot T2^2}{\left(1 + \omega c^2 \cdot T1^2\right) \cdot \left(1 + \omega c^2 \cdot T3^2\right) \cdot \left(1 + \omega c^2 \cdot T4^2\right)}\right]^{\frac{1}{2}}$$

$$C1 := Ctot \cdot \frac{T1}{T2}$$

$$C3 := \frac{C1}{5}$$

$$C4 := C3 \cdot \frac{(T3 - T4)^2}{4 \cdot T3 \cdot T4}$$

$$C2 := Ctot - C1 - C3 - C4$$

$$R2 := \frac{T2}{C2}$$

$$R3 := \frac{T4 + T3}{2 \cdot (C3 + C4)}$$

$$R4 := \frac{T4 + T3}{2 \cdot (C3 + C4)}$$

Calculated Values:

$C1 = 3.128\,nF$

$C2 = 55.192\,nF$

$C3 = 0.626\,nF$

$R2 = 99.035\,\Omega$

$R3 = 308.689\,\Omega$

$R4 = 308.689\,\Omega$

$C4 = 78.19\,pF$

Simulation

Define loop parameters

$$A1 := R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4$$

$$B1 := C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2)$$

$$Ck := R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + R4 \cdot C4 \cdot (C1 + C2 + C3)$$

$$D := C1 + C2 + C3 + C4$$

$$Z(s) := \frac{1 + s \cdot T2}{s \cdot Ctot \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)}$$

$$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega \cdot i)}{\omega \cdot i}$$

$$\omega := 10kHz$$

$$\omega c1 := root(|G(\omega)| - N1, \omega)$$

$$\frac{\omega c1}{2 \cdot \pi} = 80 \cdot kHz$$

$$\phi 1 := arg(G(\omega c)) \cdot \frac{180}{\pi} + 180$$

$\phi 1 = 49.27$

ADF4155 Synthesizer Values Calculation

$$RF_{OUT} = f_{PFD} \times N$$

$$N = \frac{RF_{OUT}}{f_{PFD}}$$

$$INT = integer\left(N = \frac{RF_{OUT}}{f_{PFD}}\right)$$

$$FRAC1 = 2^{24} \times (N - INT)$$

$$f_{PFD} = REF_{IN} \times \left[\frac{(1 + D)}{R \times (1 + T)}\right]$$

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1}$$

$$MOD2 = \frac{f_{PFD}}{GCD(f_{PFD}, f_{CHSP})}$$

$$FRAC2 = [(N - INT) \times 2^{24} - FRAC1] \times MOD2$$

ADF4155 Evaluation Board and Spectrum Analyser Output

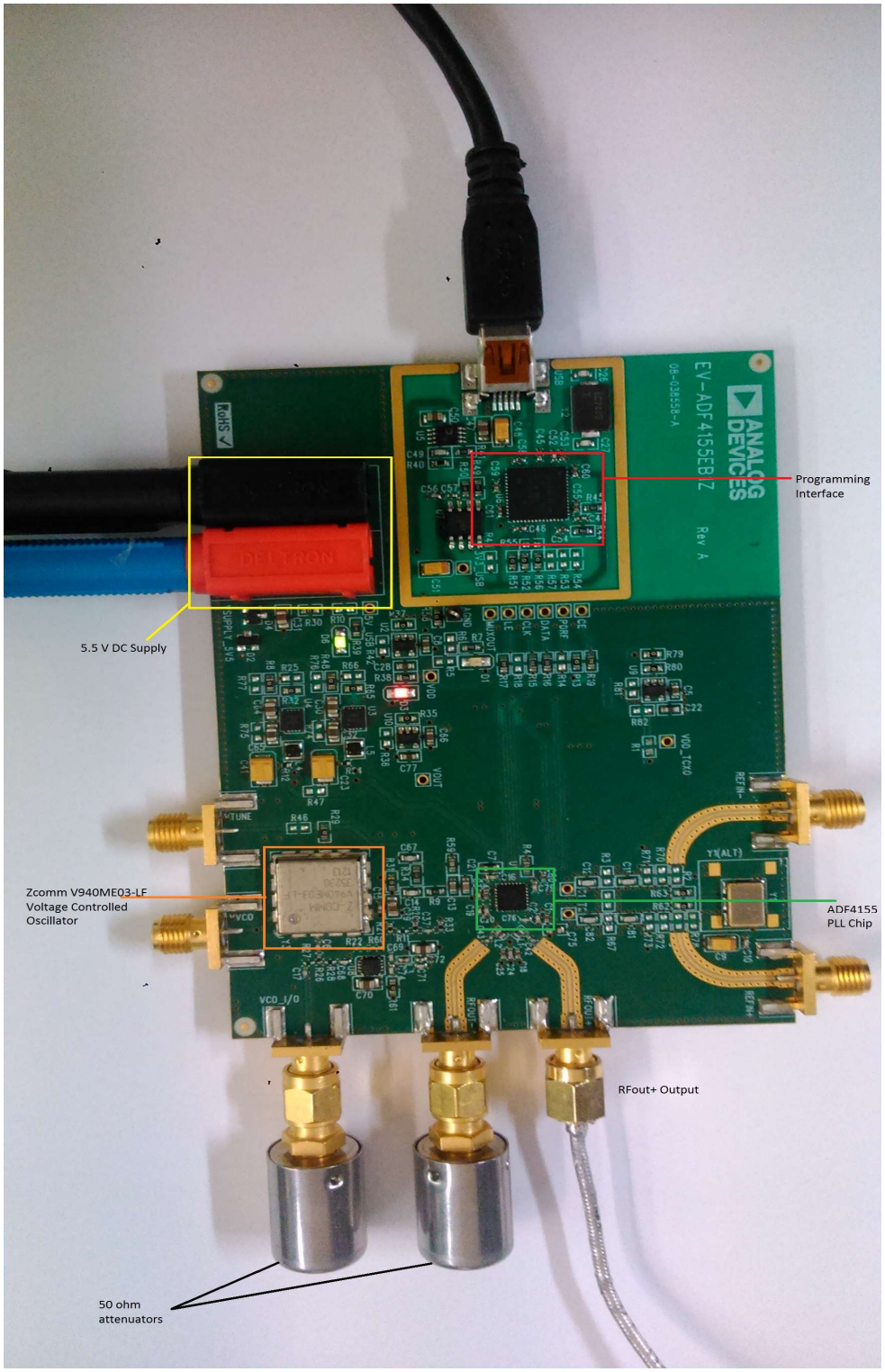

Figure 36 ADF4155 Evaluation Board

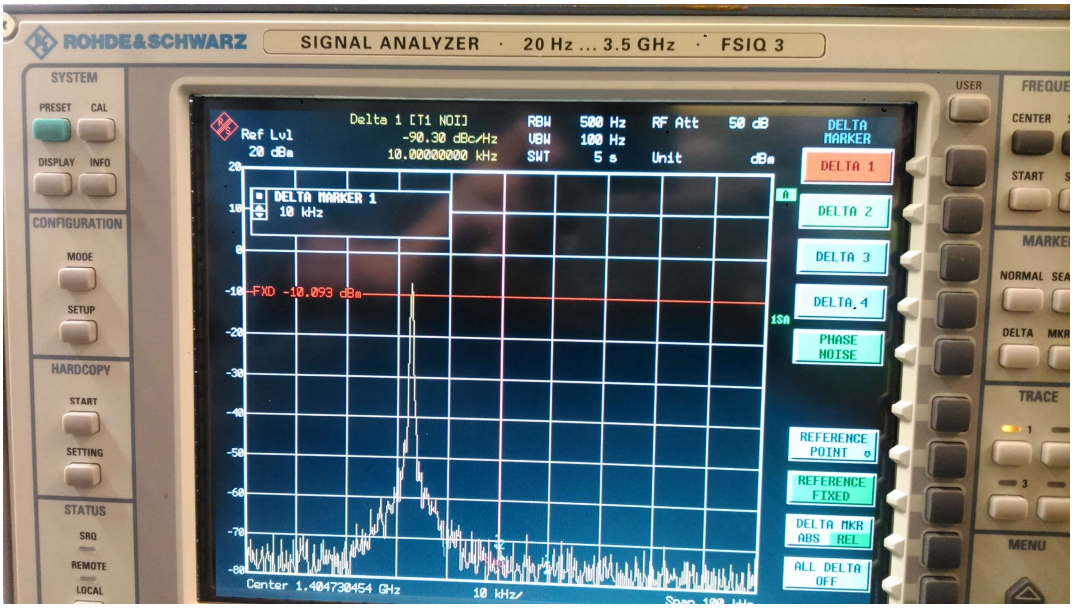

Figure 37 Phase Noise measured at 10 kHz offset displaying a value of -90.30 dBc/Hz

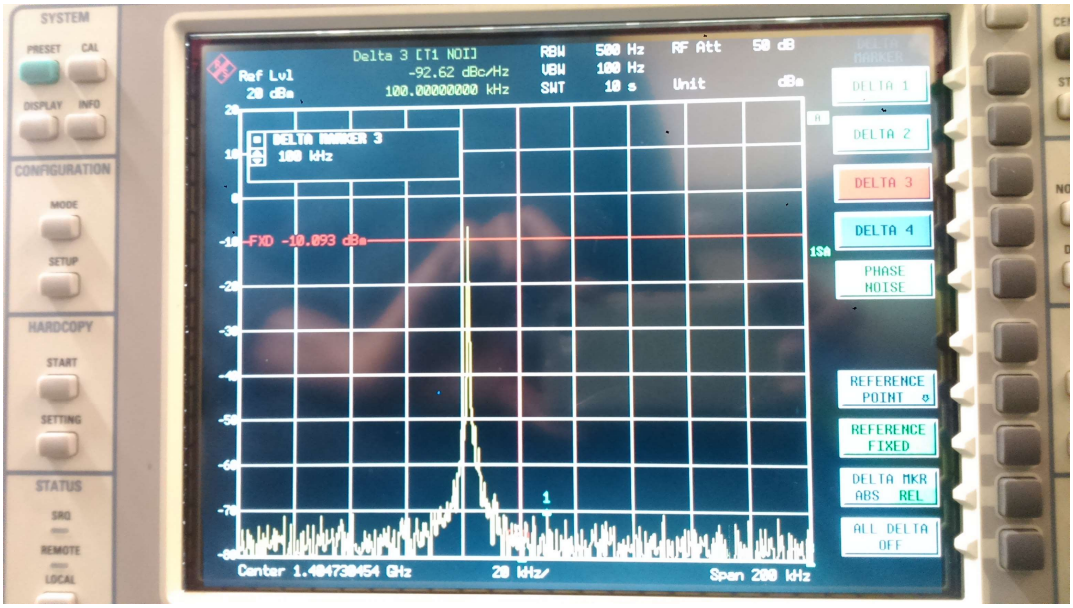

Figure 38 Phase Noise measured at 100 kHz offset displaying a value of -92.62 dBc/Hz

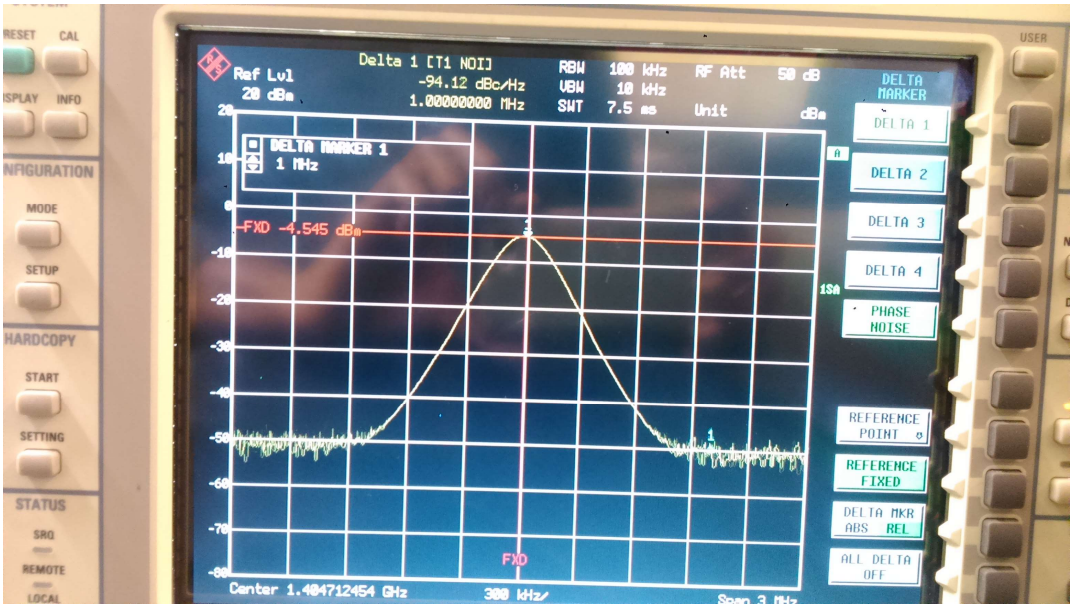

Figure 39 Phase Noise measured at 1 MHz offset displaying a value of -94.12 dBc/Hz