

Visa Tuominen

## Small Form Factor Flyback Converter

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| The goal of this thesis work was to design a small form factor isolated DC/DC power supply <br> to be used in a railway application. The power supply was designed to use 24 V nominal <br> supply voltage and provide a rated 1.2 W output power to a serial link converter device at a <br> nominal output voltage of 5 V. <br> Isolated DC/DC converter topologies were compared and the Flyback topology was chosen <br> based on this comparison. The operation of the Flyback topology was investigated and sim- <br> ulated. Based on the operation theory and simulations, as well as requirements set for the <br> power supply, a prototype was designed. |  |
| Preliminary testing was conducted on the prototype. The efficiency and load regulation of <br> the power supply were measured at different supply voltages, and the output voltage ripple <br> and switching waveforms were measured at the nominal supply voltage, using a load repre- <br> sentative of the serial link converter. <br> Based on the preliminary testing conducted on the prototype, the designed power supply <br> module could supply the required output power at supply voltages ranging from 12 V to 26 <br> V, with acceptable output voltage ripple. <br> Additional testing is needed to validate the power supply's EMI characteristics as well as <br> operation in different ambient temperatures. |  |
| Keywords |  |



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## List of Abbreviations

CCM Continuous Conduction Mode. Operating mode of a switching converter

DC Direct current. Unidirectional flow of electronic charge.

DCM Discontinuous Conduction Mode. Operating mode of a switching converter

EDA Electronic Design Automation (software). A suite of tools to aid electronic design, such as schematic capture and PCB layout

EIA Electronic Industries Alliance, a US based organization.

EMI Electromagnetic interference. An electronic disturbance caused by electromagnetic fields created by other electronic circuits.

IC
Integrated circuit

LED Light Emitting Diode

PCB Printed Circuit Board

## 1 Introduction

This thesis focuses on the electrical design of an isolated, small form factor DC/DC power supply for a serial link converter module used in a railway application.

As a part of a train data system upgrade project, a new serial link connection is made between existing and new devices. To reduce the effect of EMI on the communication between the devices, a conversion from non-differential RS-232 signalling to differential RS-422 signalling is required. The conversion should take place as close to the RS-232 signal source as possible and for this reason, a serial link converter device is fitted straight on to a serial port of the existing device.

The serial link converter requires a 5 V supply voltage. The existing device provides a 24 V supply in an adjacent port to the serial link port the SL converter connects to. A small 24 V to 5 V converter can be designed to connect to the adjacent "power" port to supply the required 5 V to the serial link converter.

In this thesis, the applicability of different isolated DC/DC converter topologies is investigated, after which the operation of the chosen topology is detailed and simulated. Based on these results, as well as requirements set for the power supply, a prototype power supply circuit can be designed, and testing can be conducted on the prototype.

## 2 Isolated DC-DC Converter Topologies

When designing a power converter, the first choice is the selection of the topology for the converter. This selection is largely based upon the desired output power for the converter. For the basic isolated DC-DC converter topologies, the traditional order from lower to higher power output is traditionally Flyback, Forward, Push-Pull, Half-Bridge and Full-Bridge. Other factors to consider during topology selection include component cost, size constraints, noise characteristics and input voltage range. [1.]

Out of the listed topologies, this chapter elaborates on the function and characteristics of the three lowest power output topologies: The Flyback, Forward and Push-Pull.

### 2.1.1 Flyback Converter

The flyback is similar to the buck-boost topology, the difference being that the output is isolated by using a transformer as the power storage inductor [2]. It works by storing energy on the primary side coil in the form of a magnetic field when the controlling switch is closed (Red in Figure 1), and discharging this energy on the secondary side when the controlling switch is opened (Blue in Figure 1).


Figure 1: Flyback converter

The Flyback is generally considered to be the most used isolated topology. It is usually found in low cost and low power applications. The topology requires only a single controlling switch and does not require a separate output inductor in addition to transformer, since the transformer itself is used as the storage inductor. These factors make the topology low cost and easy to implement. The disadvantages of the topology are its poor utilization of the transformer used due to only one of the windings conducting at a time, and the need for extra capacitors at both the input and the output due to high input and output ripple currents. [1.]

### 2.1.2 Forward Converter

The forward converter is essentially a transformer-isolated buck converter. Like the Flyback topology, it is best suited for lower power applications, and offers similar efficiency to the Flyback converter. The amount of minimal required components is higher however, the forward converter requiring an additional reset winding on the primary side of the transformer, as well as an output storage inductor and an additional diode on the secondary side. [2.]

The output current is a combination of two diode currents, marked red and blue on the secondary side in Figure 2. The transformer is magnetized when the primary side switch is closed, resulting in a current through D1 on the secondary side. When the switch is opened, the transformer is demagnetized through the primary side diode to the supply using the reset winding of the transformer, while the load is getting supplied by the output storage inductor and the output capacitor (Lout, $\mathrm{C}_{\text {out }}$ in. Figure 2). [3.]


Figure 2: Forward converter

### 2.1.3 Push-Pull Converter

The push-pull converter can be thought of as a forward converter with two primary windings. The input voltage is supplied to the primary side transformer in a push-pull configuration and switched by two transistors, creating an alternating voltage on the primary side and a transformed alternating voltage on the secondary side. This alternating voltage can then be rectified and filtered for DC applications. [4.]

A simplified diagram of a push-pull converter can be seen in Figure 3. The currents flowing when the switch S 1 is closed are shown in red. The currents flowing when S 2 is closed are shown in blue.


Figure 3: Simplified push-pull converter

Compared to the forward and flyback converters, the push-pull converter utilizes the transformer core more efficiently, since both the push and pull waveform are supplying power to the load. This allows for scaling up to higher power applications. However, since only half of the copper is used at a time, copper losses in the transformer are increased when compared to forward converters. [2.]

### 2.1.4 Topology Selection

Based on the topology features detailed in this chapter, the topology of choice for the power supply required by this thesis project was the Flyback. The required output power of the serial converter is low at 1.2 W , and considering the physical restrictions detailed in section 4.4, the low component count required by the Flyback, when compared to other isolated low-power dc-dc topologies, should help keep the size of the power supply small.

## 3 Flyback Converter Operation Theory

As stated in section 2.1.1, the flyback converter is a transformer-isolated version of the buck-boost converter. Although the magnetic device is represented using the symbol of a transformer, it is used as a "two winding inductor". This means that unlike how a transformer is generally utilised, in a flyback converter current does not flow simultaneously on the primary and secondary windings. [5.]

The operation of a flyback converter can be divided into two stages depending on the state of the controlling switch, as is the case with most switching converters: the 'switch closed' and 'switch open’ stage.

### 3.1 Switch Closed

When the switch is closed, an increasing magnetizing current (ip in Figure 4) flows through the primary winding of the transformer, storing energy in the primary side winding of the transformer in the form of a magnetic field. This energy storage can be modelled by a magnetizing inductance ( $\mathrm{L}_{\mathrm{m}}$ in Figure 4 ) parallel to the primary winding of the ideal transformer. This creates a negative voltage on the secondary, which turns the output diode ( D in Figure 1) off, keeping the secondary from conducting current. This is represented as an open circuit in Figure 4. Energy stored in the output capacitor during the previous cycle is discharged to the load. [5.]


Figure 4: Flyback converter model, switch closed

Assuming ideal components, the currents and voltages noted in Figure 4 can be approximated as follows [5]:

$$
\begin{array}{r}
\text { Inductor voltage } \quad v_{L}=V_{S} \\
\text { Capacitor current } \quad i_{C}=-\left(\frac{V_{O}}{R}\right) \tag{2}
\end{array}
$$

Where $V_{s}$ is the supply voltage, $V_{o}$ is the output voltage and $R$ is the load resistance.

The slope of the rising magnetizing current $i_{P}$ is determined by the transformer primary inductance $L_{p}$ and the supply voltage $V_{s}$. By the property of inductance:

$$
\begin{equation*}
v(t)=L \frac{d i}{d t} \rightarrow \frac{d i_{P}}{d t}=\frac{V_{s}}{L_{p}} \tag{3}
\end{equation*}
$$

The primary side magnetizing current therefore rises to a maximum value $I_{\mathrm{pk}}$, which is dependent on the time that the switch is closed, $\mathrm{T}_{\mathrm{on}}$ :

$$
\begin{equation*}
I_{P K P}=\frac{d i_{P}}{d t} \cdot T_{O N}=\frac{V_{s}}{L_{p}} \cdot T_{O N} \tag{4}
\end{equation*}
$$

This peak current gives the energy stored in the primary side winding, $W$ :

$$
\begin{equation*}
W=\frac{1}{2} L_{P} \cdot I_{P K P}^{2} \tag{5}
\end{equation*}
$$

When the controlling switch is opened, the stored energy $W$ gets transferred to the secondary coil.

### 3.2 Switch Open

When the switch is opened, the primary side magnetizing current (ip in Figure 5) immediately stops, resulting in a decreasing demagnetizing current on the secondary side (is
in Figure 5). This current flows through the output diode and transfers power from the transformer to the load and charges the output capacitor.


Figure 5: Flyback converter model, switch open
During this stage, the primary side coil voltage vL reflects the output voltage over the secondary side coil [6, p. 270]:

$$
\begin{equation*}
v_{L}=-n \cdot V_{O}=\frac{N_{1}}{N_{2}} \cdot V_{O} \tag{6}
\end{equation*}
$$

The capacitor is charged by the transformer secondary coil with current ic:

$$
\begin{equation*}
i_{C}=i_{S}-\frac{V_{O}}{R} \tag{7}
\end{equation*}
$$

Like on the primary side, on the secondary side, the slope of the demagnetizing current $i_{s}$ is dependent on the secondary side inductance $L_{s}$ as well as the output voltage, $V_{0}$ :

$$
\begin{equation*}
\frac{d i_{S}}{d t}=\frac{-V_{o}}{L_{s}} \tag{8}
\end{equation*}
$$

The secondary side peak current that flows right after the switch is opened can be deduced from the property of transformers shown in [6, p. 29]:

$$
\begin{equation*}
\frac{I_{1}}{I_{2}}=\frac{N_{2}}{N_{1}}=\frac{1}{n} \tag{9}
\end{equation*}
$$

Where $n$ is the primary to secondary turns ratio, $N$ the number of turns, and $/$ the current on the primary and secondary sides denoted by subscripts 1 for the primary and 2 for the secondary sides.

By equation (9) it follows that the secondary side peak current $I_{P K S}$, flowing right after the switch opens, is relative to the primary side peak current $l_{P K P}$ by the transformer turns ratio $n$ :

$$
\begin{equation*}
I_{P K S}=n \cdot I_{P K P} \tag{10}
\end{equation*}
$$

### 3.3 Operating Mode

Depending on whether the current flowing in the transformer windings reaches zero during a single cycle, the operating mode of the converter can be classified into either continuous mode or discontinuous mode.

When the supplied load current ( $\mathrm{I}_{0}$ in Figure 6) is sufficiently low, the secondary side coil has time to completely discharge during a single switching cycle $T$. This results in what is called discontinuous conduction mode (DCM) operation. During the period between the secondary coil discharging and the primary side switch closing, the load is being supplied by the output capacitor.


Figure 6: Transformer primary side voltage ( $\mathrm{V}_{\mathrm{L}}$ ), primary and secondary side currents, DCM

Assuming a steady state of operation, the principle of volt-second balance can be applied to the transformer primary winding, meaning that the area of the negative and positive voltage waveforms of $V_{L}$ must be equal [6, p. 270]. This gives an estimate for the switching times of the converter in discontinuous mode:

$$
\begin{array}{r}
T_{O N} \cdot V_{S}=T_{O F F} \cdot n \cdot V_{O} \\
\frac{T_{O N}}{T_{O F F}}=\frac{n \cdot V_{O}}{V_{S}} \tag{12}
\end{array}
$$

When the supplied load current is higher, the switch on the primary side will be closed by the controlling circuitry before the transformer secondary has been completely discharged. This mode of operation is called continuous conduction mode (CCM).


Figure 7: CCM voltage and current waveforms

The average value of the primary winding voltage over a switching cycle must be zero also in CCM, and the same switching time equations apply as in DCM operation [6, p. 269]. In CCM however, there is no time period within a switching cycle where neither the primary or secondary side is conducting, and therefore in CCM, the sum of the ON and OFF times of the primary switch are equal to the switching cycle time T .

The border between the discontinuous and continuous operation mode is called boundary conduction mode. In this operation mode the controlling circuitry lets the secondary winding completely discharge, and as soon as the secondary current hits zero, it closes the controlling switch and charges the primary winding.

Switching controllers monitor the output voltage of the circuit and adjust the switching time T based accordingly. For output voltage monitoring, flyback circuits incorporate a form of feedback from the secondary side to the controller, such as an additional transformer winding to read the output voltage from or an opto-isolator between the primary and secondary sides of the circuit.

In this thesis's application the converter is expected to operate in DCM, since the required output voltage of 5 V is a fraction of the input voltage of 24 V and the required output current supplying capacity of 240 mA is fairly low, even for a small form factor power supply, such as the one required in this thesis.

## 4 Requirements

### 4.1 Electrical Requirements

The serial converter module requires a 4.5 V to 5.5 V supply voltage. This is achieved by converting an existing 24 VDC supply voltage to 5 VDC.

The power supply must be galvanically isolated and be able to supply approximately 1.2 W of power, equivalent to 240 mA of output current. The actual power draw of the serial converter is expected to be closer to $100-150 \mathrm{~mA}$ in normal operation.

The power supply should be designed in a way to minimise its susceptibility to EMI as well as to minimise the EMI caused by the power supply. The importance of EMI optimization is heightened in the design of switching power supplies due to the high amounts of voltage and current fluctuations used in the power conversion process.

### 4.2 Environmental Requirements

The adverse effects of outside factors such as dust ingress, vibration and temperature variation are to be minimised. The installation location's temperature is expected to range from $-25^{\circ} \mathrm{C}$ to $40^{\circ} \mathrm{C}$ and the converter should be able to meet its full performance under sustained temperatures of $15^{\circ} \mathrm{C}$ above ambient.

### 4.3 Component Availability

All the components used should be "in established ranges and in series production", meaning that their availability should be guaranteed for the foreseeable future. This is to
ensure that in case of any malfunctions during the lifetime of project, replacement parts are readily available.

### 4.4 Physical Dimensions

The installation space for the converter will be very limited, as it will be fit inside a cabinet with existing hardware surrounding it. The clearance measured from the serial ports where the converter is to be installed, to equipment mounted on the closed cabinet door (1 in Figure 8) can be as small as 15 mm . As the location of this equipment might vary between train units where the converter is installed, the 15 mm clearance must be considered in the case of a device connecting to the topmost port (2 in Figure 8) as well.


Figure 8: Install location, cabinet door closed
The converter should not cover the LEDs of the card it is connecting to (4 in Figure 9). Its dimensions are limited by the middle port of the card as well as the handles of the card ( 3 and 5 in Figure 9). In addition to the already limited vertical space available, this sets limits to the horizontal space, as well.


Figure 9: Front panel with serial, DC output for converter

### 4.5 Mounting

The converter should be secured in its installation location. Unfortunately, the connectors in the installation location do not have threads. Removal of the card shown in Figure 9 as a part of the converter install process is also undesirable.

## 5 Component Selection

The component selection procedure started with trying to find a suitable component in the company's internal component database. If no suitable component was found, the search was taken to online component suppliers.

### 5.1 Enclosure

The enclosure used for the power supply will be the same as for serial converter module, the Hammond Mfg. 1551L. Using this enclosure leaves a suitable amount of clearance to the surrounding hardware mentioned in section 4.4. The PCB will be mounted to the lid of the enclosure as opposed to the mounting posts to increase the vertical space available for components inside the enclosure to 10 mm , as seen in Figure 10. This will broaden the selection of suitable transformers to be used in the converter. Other components are expected to be well below 10 mm in height.


Figure 10: 2D view of clearance inside enclosure

### 5.2 Controller IC

Comparing Flyback regulators already available in the company database, the LT8300 series regulators by Analog Devices were found to be suitable candidates for the application. The LT8300 series promises a minimal need of external components since the regulators sample the output voltage from the primary side waveform removing the need of an opto-isolator, as well as offer an integrated power switch. The lower power variants also come in a compact SOT-23-5 package. Out of the LT8300 series regulators, the $65 \mathrm{~V}, 1.2 \mathrm{~A}$ (switch maximum ratings) variant LT8301 was chosen. A typical application circuit for the LT8301 can be seen in Figure 11.


Figure 11: Simplified schematic of a Flyback converter utilizing the LT8301 controller IC, copied from [7]

The LT8301 datasheet [7] provides suggestions on some components to use, such as providing a list of recommended transformers and diodes for use with the controller IC. For most components however, calculations based on the operation theory in chapter 3 as well as equations provided in the controller IC datasheet were used to determine the
requirements for components to be used in the circuit, after which a suitable component was searched for in the company's component database.

### 5.3 Transformer

To protect the switching pin (SW in Figure 11) there will be an upper limit on the transformer turns ratio [7, p. 12]. This is a result of the output voltage being reflected on the primary side and being seen on top of the input voltage by the switching pin when the transistor is turned off. Deriving from equation (6):

$$
\begin{equation*}
v_{S W}=V_{S}+v_{L}=V_{S}+n \cdot V_{O} \tag{13}
\end{equation*}
$$

To better account for real world circumstances, an approximation for the forward voltage of the output diode must be considered in this calculation as well. This forward voltage will be reflected on the primary side in addition to the output voltage, as the output diode is in series with the load. Since no output diode has yet been chosen, an estimated forward voltage $\left(V_{f}\right)$ of 0.7 V is used in this calculation.

A margin must also be kept between the calculated switch node voltage $\left(V_{s w}\right)$ and the rated switch maximum voltage of 65 V to account for a voltage spike caused by the leakage inductance of the transformer when the switch is closed. This margin will be noted as $\bigvee_{\text {leakage }}$ :

$$
\begin{equation*}
V_{S W(\max )}>V_{S}+n \cdot\left(V_{O}+V_{f}\right)+V_{\text {leakage }} \tag{14}
\end{equation*}
$$

Rearranging the equation (14) provides an estimate for the upper limit for the transformer turns ratio $n$ :

$$
\begin{equation*}
n<\frac{V_{S W(\max )}-V_{S}-V_{\text {leakage }}}{V_{O}+V_{f}} \tag{15}
\end{equation*}
$$

Setting a recommended 15 V margin [7, p. 9] for the transformer leakage spike and assuming a 0.7 V forward voltage for the output diode results in the following calculation:

$$
V_{S W(\max )}=65 \mathrm{~V}, \quad V_{S}=24 \mathrm{~V}
$$

$$
\begin{aligned}
& n<\frac{65 \mathrm{~V}-24 \mathrm{~V}-15 \mathrm{~V}}{5 \mathrm{~V}+0.7 \mathrm{~V}} \\
& n<4.56
\end{aligned}
$$

Using estimated 85\% efficiency (Figure 11) and listed maximum switch current limit of 1.2 A, the power output for a given primary-to-secondary turn ratio can be estimated [7, p.16]:

$$
\begin{equation*}
P_{\text {out }}=\eta \cdot V_{S} \cdot D \cdot I_{s w(\max )} \cdot 0.5 \tag{16}
\end{equation*}
$$

Where $D=$ Duty cycle $=\frac{N_{p s}\left(V_{\text {out }}+V_{f}\right)}{N_{p s}\left(V_{\text {out }}+V_{f}\right)+V_{\text {in }}}$

Using previously estimated values in equations (16) and (17) gives the following calculation:
$\eta=$ Efficiency $\approx 0.85$
$I_{s w(\max )}=1.2 \mathrm{~A}(\min ), \quad V_{\text {in }}=24 \mathrm{~V}, \quad V_{\text {out }}=5 \mathrm{~V}, \quad V_{f}=0.7$
$P_{N=1}=0.85 \cdot 24 V \cdot \frac{1(5 V+0.7 V)}{1(5 V+0.7 V)+24 V} \cdot 1.2 A \cdot 0.5 \approx 2.3 \mathrm{~W}$
$P_{N=2} \approx 3.9 \mathrm{~W}, \quad P_{N=3} \approx 5.1 \mathrm{~W}, \quad P_{N=4} \approx 6.0 \mathrm{~W}$

According to these results, to achieve 1.2 W output power, the transformer turns ratio will not be the limiting factor.

Since the LT8301 samples the output voltage from the reflected output voltage on the SW pin, there is a 450 ns minimum time the secondary winding must conduct for the switching IC's voltage sampling to function correctly. Additionally, the LT8301 has a minimum switch-on time of 170 ns to protect the switch from turn-on spikes. This places a limitation on the primary side winding inductance of the transformer as well. [7, p. 10 .]
$t_{o f f(\text { min })}=$ Minimum switch off time $=450 \mathrm{~ns}$
$t_{o n(\text { min })}=$ Minimum switch on time $=170 \mathrm{~ns}$
$I_{s w(\text { min })}=$ Minimum switch current limit $=290 \mathrm{~mA}($ typical $)$
$L_{p r i} \geq \frac{t_{\text {on }(\min )} \cdot V_{\text {in }(\max )}}{I_{s w(\min )}}, L_{p r i} \geq \frac{t_{\text {off }(\min )} \cdot N \cdot\left(V_{\text {out }}+V_{f}\right)}{I_{s w(\min )}}$

Since the choice of the output diode will depend on the turns ratio of the transformer used, an estimated forward voltage of 0.7 V is used here as well.
$V_{\text {out }}=5 \mathrm{~V}, \quad V_{f}=0.7 \mathrm{~V}$
Resulting in:
$L_{p r i} \geq \frac{170 \mathrm{~ns} \cdot 30 \mathrm{~V}}{290 \mathrm{~mA}}=18 \mu \mathrm{H}$,
$\mathrm{L}_{\mathrm{pri}(\mathrm{N}=1)} \geq \frac{450 \mathrm{~ns} \cdot 1 \cdot(5 \mathrm{~V}+0.7 \mathrm{~V})}{290 \mathrm{~mA}} \approx 9 \mu \mathrm{H}$,
$L_{p r i(N=2)} \geq 2 \cdot 9 \mu H \approx 18 \mu H$,
$L_{p r i(N=3)} \geq 3 \cdot 9 \mu H \approx 26 \mu H$,
$L_{p r i(N=4)} \geq 4 \cdot 9 \mu H \approx 34 \mu H$

Taking the above calculated limits as well as the 10 mm seating height limitation into account, the transformer 750370047 from Würth Elektronik was chosen. Specifications of the transformed used in calculations can be seen in Table 1.

Table 1: Wurth 750370047 Electrical specifications, copied from [8]

## ELECTRICAL SPECIFICATIONS (3) $25^{\circ} \mathrm{C}$ unless otherwise noted:



The choice of flyback transformers is limited, since many of the components fulfilling the calculated requirements do not fit the minimum vertical space of 10 mm . Within its specification, the 750370047 narrowly provides enough primary side inductance for its turn ratio of 3 , and has a maximum height of 9.14 mm , as seen in Figure 12, fitting barely in the chosen enclosure.


Figure 12: Wurth 750370047 physical dimensions, copied from [8]

Using values listed in Table 1, the maximum load switching frequency can be calculated according to the equation provided in [7, p. 16]:

$$
\begin{equation*}
F_{s w(\max )}=\frac{1}{t_{o n}+t_{o f f}}=\left(\frac{L_{p r i} \cdot I_{s w}}{V_{\text {in }}}+\frac{L_{p r i} \cdot I_{s w}}{N\left(V_{o u t}+V_{f}\right)}\right)^{-1} \tag{19}
\end{equation*}
$$

$$
\begin{equation*}
\text { Where } \quad I_{s w}=\frac{V_{\text {out }} \cdot I_{o u t} \cdot 2}{\eta \cdot V_{i n} \cdot D} \tag{20}
\end{equation*}
$$

$$
\begin{aligned}
& \mathrm{V}_{\text {out }}=5 \mathrm{~V}, \quad \mathrm{I}_{\text {out }}=\frac{\mathrm{P}_{\text {out }}}{\mathrm{V}_{\text {out }}}, \quad \eta=0.85, \quad \mathrm{~V}_{\text {in }}=24 \mathrm{~V} \\
& \mathrm{D}=\frac{\mathrm{N}_{\mathrm{PS}}\left(\mathrm{~V}_{\text {out }}+\mathrm{V}_{\mathrm{f}}\right)}{\mathrm{N}_{\mathrm{PS}}\left(\mathrm{~V}_{\text {out }}+\mathrm{V}_{\mathrm{f}}\right)+\mathrm{V}_{\text {in }}} \approx 0.42 \\
& \rightarrow \mathrm{I}_{\text {sw }}=\frac{5 \mathrm{~V} \cdot \frac{1.2 \mathrm{~W}}{5 \mathrm{~V}} \cdot 2}{0.85 \cdot 24 \mathrm{~V} \cdot 0.42} \approx 0.29 \mathrm{~A} \\
& F_{s w(\text { max })}=\frac{1}{t_{\text {on }}+t_{\text {off }}}=\left(\frac{L_{\text {pri }} \cdot I_{s w}}{V_{\text {in }}}+\frac{L_{p r i} \cdot I_{\text {sw }}}{N\left(V_{\text {out }}+V_{f}\right)}\right)^{-1} \\
& =\left(\frac{30 \mu \mathrm{H} \cdot 0.29 \mathrm{~A}}{24 \mathrm{~V}}+\frac{30 \mu \mathrm{H} \cdot 0.29 \mathrm{~A}}{3 \cdot(5 \mathrm{~V}+0.5 \mathrm{~V})}\right)^{-1} \\
& \quad \approx 1.15 \mathrm{MHz}
\end{aligned}
$$

According to this result, the switching frequency will not be limited by the component selections, as the controller IC limits the switching frequency internally to below 430 kHz [7, p. 7].

### 5.4 Output Diode

As a result of equation (9) describing the relation of the primary and secondary side currents in the transformer, the output diode should be rated for at last the maximum switch current multiplied by the turns ratio of the transformer [7, p. 16]:

$$
\begin{equation*}
I_{f}=I_{s w(\max )} \cdot n=1.2 \mathrm{~A} * 3=3.6 \mathrm{~A} \tag{21}
\end{equation*}
$$

The diode must also be able to withstand a reverse voltage that is a sum of the output voltage and an estimate of the maximum voltage seen by the primary side divided by the transformer turns ratio. For this calculation, an estimated maximum input voltage of 30 V is used:

$$
\begin{equation*}
V_{r}=V_{\text {out }}+\frac{V_{\text {in }(\max )}}{N} \rightarrow 5+\frac{30}{3}=15 \mathrm{~V} \tag{22}
\end{equation*}
$$

According to these requirements the MURD620CT was chosen. The double-diode package is rated for up to a 6 A forward current and has a reverse breakdown voltage of 200 V [9].


Figure 13: Forward voltage vs forward current, copied from [9]

The forward voltage is dependent on the forward current as well as the junction temperature (Figure 13). In this application, the expected external temperature maximum is $55^{\circ} \mathrm{C}$, resulting in forward voltage variation between 0.7 V and 0.8 V .

### 5.5 Output Capacitor

To estimate the capacitance needed to attain a given level of output voltage ripple, the following equation is given [7, p. 17]:

$$
\begin{equation*}
C_{\text {out }}=\frac{L_{\text {pri }} \cdot I_{\text {sw }}{ }^{2}}{2 \cdot V_{\text {out }} \cdot \Delta V_{\text {out }}} \tag{23}
\end{equation*}
$$

Where $\Delta V_{\text {out }}$ is the desired output ripple. Using the previously calculated values of $L_{\text {pri }}=30 \mu H, \quad I_{s w}=0.29 \mathrm{~A}, \quad V_{\text {out }}=5 \mathrm{~V}$

And setting a desired output ripple of $1 \%$ of $V_{\text {out }}=50 \mathrm{mV}$ results in the following calculation:

$$
\begin{equation*}
C_{\text {out }}=\frac{30 \mu H \cdot(0.29 A)^{2}}{2 \cdot 5 V \cdot 0.05}=22 \mu F \tag{24}
\end{equation*}
$$

This is to be considered mostly as an absolute minimum value, since ceramic capacitors lose capacitance with temperature as well as when voltage is applied to them [10]. A smaller capacitance filter capacitor can be added in parallel to filter out higher frequency noise from the output voltage. Using these guidelines, a pair of $47 \mu \mathrm{~F}$ capacitors in EIA 0805 package size, as well as a single 100 nF capacitor in EIA 0603 package size were chosen to be used for output filtering.

### 5.6 Output Voltage Setting Feedback Resistance

Provided all other requirements are met, the output voltage of the converter is programmed by a single sensing (feedback) resistance connected to the switching node SW. This output voltage relies also on the primary to secondary turns ratio of the transformer as well as the forward voltage of the output diode [7, p. 17]:

$$
\begin{equation*}
V_{\text {out }}=100 \mu A \cdot \frac{R_{f b}}{n}-V_{f} \tag{25}
\end{equation*}
$$

Assuming a forward voltage of 0.7 V according to Figure 13, a value for the feedback resistance can be calculated by rearranging the output voltage equation:
$R_{f b}=\frac{n \cdot\left(V_{\text {out }}+V_{f}\right)}{100 \mu A}=\frac{3 \cdot(5 V+0.7 V)}{100 \mu A} \approx 171 \mathrm{k}$

Using a series connection of 162k and 6k04 resistors in package size EIA 0603 was chosen. With a combined feedback resistance $168040 \Omega$, the estimated output voltage is:

$$
\begin{equation*}
V_{\text {out }}=100 \mu \mathrm{~A} \cdot \frac{168.04 \mathrm{k} \Omega}{3}-0.7 \mathrm{~V} \approx 4.90 \mathrm{~V} \tag{27}
\end{equation*}
$$

As seen in the calculation (24), the calculated output voltage is slightly under the desired output voltage of 5.0 V . These values were used in the first prototype and adjustments could be made after the output voltage of a physical circuit was measured.

The chosen resistors used have a tolerance of $+/-1 \%$, resulting in an expected maximum deviation of $+/-56 \mathrm{mV}$ in the output voltages between units resulting from the resistor tolerance.

### 5.7 Snubber Circuit

When the switch of the controller IC opens, the transformer leakage inductance ( $L_{L}$ in Figure 14) Induces a voltage spike to the switch pin (SW). This spike is seen by the switching node on top of the input voltage as well as the transformed voltage of the secondary side. [5.]


Figure 14: Switch off state currents and voltages

Basing on equation (13), and using an estimate of 0.7 V for the output diode forward voltage, the switch voltage during the OFF state can be calculated:
$V_{s w}=V_{s}+\left(V_{o}+V_{f}\right) \cdot n=24 V+(5 V+0.7 V) \cdot 3 \approx 41 V$

Without voltage clamping or attenuation, the ringing resulting from the resonance between the parasitic capacitance of the switch and transformer and the leakage inductance of the transformer will result in unwanted electromagnetic interference created by the circuit, and it might even damage the switch [5, p. 9]. Therefore, commonly a snubber circuit is used to mitigate these effects. An illustration of the switch node ringing as well as the effects of a diode-zener (DZ) and resistor-capacitor (RC) snubbers can be seen in Figure 15.


No Snubber

with DZ Snubber

with RC Snubber

Figure 15: Maximum Voltages for SW Pin Flyback Waveform, copied from [7]

Due to the relatively low input and output voltages used in this thesis's application, there is roughly 24 V of headroom for ringing before the 65 V maximum voltage rating of the switch. Nevertheless, to reduce interference as well as provide better load regulation, an RC snubber will be used [7], consisting of a capacitor and resistor in series between the supply voltage and the switching node (Rs, Cs in Figure 14).

The operation of an RC snubber is based on the capacitor storing the charge stored by the transformer leakage inductance and the resistor then dissipating this charge before ringing occurs. The values for these components can be determined by measuring the ringing of the switching node from a prototype circuit and adding capacitance parallel to the transformer primary. [11.]

This method of measuring snubber values is described in detail section 10.1.

### 5.8 Connectors

The prototype will use a male (pins) DB-25 connector (Yellow in Figure 16) for interfacing with the existing hardware, as well as an internal 3-pin variant of the JST XH-series
connectors (Gray in Figure 16) for connection to the serial converter. Only two of the pins will be in use in both connectors. The DB25 connector is rated for currents up to 5 A [12], and the XH series connectors for 3 A [13].


Figure 16: Harting DB-25 and JST XH connectors' 3D models

Using the XH series connector will limit the cross-section of used wires to $0.34 \mathrm{~mm}^{2}$. Wire selection charts published by manufacturers such as Sab Cables [14] and JST [15] rate single or up to three $0.34 \mathrm{~mm}^{2}$ conductors for 3 A , and Sab Cables rates cables up to six conductors at 2.4 A . Based on these recommendations, $0.34 \mathrm{~mm}^{2}$ cable is sufficient for carrying the expected 0.240 A current in this thesis's application.

## 6 Estimations After Component Selection

Some additional currents and voltages in the circuit can be estimated based on the operation theory and equations in chapter 3. The calculations in this chapter will be using the following values:

Supply voltage $V_{s}=24 V, \quad$ Output voltage $V_{o}=5 V, \quad$ Output power $P=1.2 \mathrm{~W}$
Load resistance $R=21 \Omega$, Output diode forward voltage $V_{f}=0.7 \mathrm{~V}$
Estimated operating efficiency $\eta=0.85$
Transformer primary to secondary turns ratio $n=3$
Transformer primary side inductance $L_{p}=30 \mu \mathrm{H}$
Transformer secondary side inductance $L_{s}=\frac{L_{p}}{n^{2}}=\frac{30 \mu \mathrm{H}}{3^{2}} \approx 3.3 \mu \mathrm{H} \quad[6$, p.29]

### 6.1 Current Waveforms

The LT8301 datasheet approximates a switching frequency of $200-210 \mathrm{kHz}$ for a supplied current of 240 mA , as seen in Figure 17:


Figure 17: Switching Frequency vs Load Current, copied from [7]
To achieve the planned 1.2 W output power, the secondary needs to supply the output power divided by the converter estimated efficiency of $85 \%$. This power figure can be divided by the switching frequency to give the amount of energy transferred by the transformer each cycle, W :

$$
\begin{equation*}
W=\frac{P}{f_{s w} \cdot \eta}=\frac{1.2 W}{210 k H z \cdot 0.85} \approx 6.7 \mu \mathrm{~J} \tag{29}
\end{equation*}
$$

This energy gives an estimate of the primary and secondary side peak currents when used in equations (5) and (10):

$$
\begin{gather*}
W=\frac{1}{2} L_{P} \cdot I_{P K P}^{2} \rightarrow I_{P K P}=\sqrt{\frac{2 W}{L_{P}}}=\sqrt{\frac{2 \cdot 6.7 \mu J}{30 \mu H}} \approx 670 \mathrm{~mA}  \tag{30}\\
I_{P K S}=n \cdot I_{P K P} \rightarrow I_{P K S}=3 * I_{P K P} \approx 2.0 \mathrm{~A} \tag{31}
\end{gather*}
$$

The result of calculation (31) can be used to approximate the ON time (Ton) of the switching, using equation (4):
$I_{P K P}=\frac{V_{S}}{L_{p}} \cdot T_{O N} \rightarrow T_{O N}=\frac{L_{P} \cdot I_{P K P}}{V s}=\frac{30 \mu H \cdot 2.0 A}{24 V}=0.836 \ldots \mu \mathrm{~s} \approx 0.84 \mu \mathrm{~s}$

By rearranging equation (11), the OFF time can be calculated, as well:
$\frac{T_{O N}}{T_{O F F}}=\frac{n \cdot V_{O}}{V_{S}} \rightarrow T_{O F F}=\frac{T_{O N} \cdot V_{S}}{n \cdot V_{O}}=\frac{0.84 \mu s \cdot 24 V}{3 \cdot(5 \mathrm{~V}+0.7 V)}=1.174 \ldots \mu \mathrm{~s} \approx 1.2 \mu \mathrm{~s}$

Using the above calculated values, the estimated current waveforms under 1.2 W load can be drawn, as seen in Figure 18.


Figure 18: DCM Voltages and currents

### 6.2 Snubber Circuit Power Dissipation

The transformer datasheet lists a maximum $1 \mu \mathrm{H}$ leakage inductance for the primary side [8]. Each switching cycle, the snubber resistor will have to dissipate the power stored in this inductance. Assuming a steady state of operation and a constant leakage inductance, an estimation of the energy stored in the leakage inductance during each cycle can be made based on the primary side switching current calculated in calculation (32):

$$
\begin{equation*}
W_{L}=\frac{1}{2} L_{L} \cdot I_{P K P}^{2} \tag{34}
\end{equation*}
$$

Multiplying this energy with the switching frequency will give the average power dissipated by the snubber resistor:

$$
\begin{equation*}
P_{L}=W_{L} \cdot f_{s w}=\frac{1}{2} L_{L} \cdot I_{P K P}^{2} \cdot f_{s w} \tag{35}
\end{equation*}
$$

Where $L_{L}$ is the leakage inductance, $I_{P K P}$ is the primary winding peak current and $f_{s w}$ is the switching frequency. Using the maximum rated leakage inductance of $1 \mu \mathrm{H}$, calculated primary side peak current of 670 mA and a conservative estimate for the switching frequency of 250 kHz results in the following calculation:

$$
\begin{equation*}
P_{L}=\frac{1}{2} 1 \mu H \cdot 670 \mathrm{~mA}^{2} \cdot 250 \mathrm{kHz} \approx 56 \mathrm{~mW} \tag{36}
\end{equation*}
$$

The estimated power dissipation suggests that the used resistor should be sized 0402 (imperial) or above, as even the 0402 resistors are rated for $1 / 16 \mathrm{~W}(62 \mathrm{~mW})$ power dissipation [16]. To account for possibly higher switching frequencies and ambient temperatures, a 0603 sized resistor will be used in the snubber circuit of this thesis's application.

### 6.3 Output Diode Power Dissipation

Based on the estimated output power draw and the output diode forward voltage, an estimation for the dissipated power in the output diode can be calculated:

$$
\begin{gather*}
P_{D}=V_{f} \cdot I_{\text {out }}=V_{f} \cdot \frac{P_{\text {out }}}{V_{\text {out }}}  \tag{37}\\
P_{D}=0.7 \mathrm{~V} \cdot \frac{1.2 \mathrm{~W}}{5 \mathrm{~V}} \approx 0.17 \mathrm{~W} \tag{38}
\end{gather*}
$$

Using this power figure, the operating junction temperature can be calculated by using the junction-to-ambient thermal resistance in the diode datasheet [9]:

$$
\begin{equation*}
\Delta T=P * \theta_{J A} \tag{39}
\end{equation*}
$$

Where $\Delta T$ is the junction to ambient temperature delta and $\theta_{J A}$ the diode junction-to ambient thermal resistance ( $80^{\circ} \mathrm{C} / \mathrm{W}$ ).
Resulting in the following calculation:

$$
\begin{equation*}
\Delta T=0.17 W \cdot 80 \frac{{ }^{\circ} \mathrm{C}}{W} \approx 14^{\circ} \mathrm{C} \tag{40}
\end{equation*}
$$

Given the maximum operation junction temperature of the diode, $175^{\circ} \mathrm{C}$, the estimated maximum operating temperature is roughly $160^{\circ} \mathrm{C}$. This suggests that the diode will most likely not be the first component to fail due to ambient temperature fluctuation. For example, the JST connector is only rated for temperatures up to $85^{\circ} \mathrm{C}$.

## 7 Simulation

To better estimate the operation of the converter circuit, as well as validate some of the calculations made in previous chapters, simulations were run by using the LTSpice XVII simulation software by Analog Devices, as well as an online Flyback circuit simulator, by a Dr. Heinz Schmidt-Walter \& co. [17]. The values used for the components in the simulation were based on the component selections made in chapter 4.

### 7.1 Generic Online Flyback Converter Simulation

In addition to providing insight into the operation of different types of switching mode power supplies, the website created by Schmidt-Walter \& company provides an online simulation tool for a generic flyback converter circuit (Figure 19). The used components are mostly assumed to be ideal, except for the used transformer (L1 in Figure 19) and the output diode. The simulator uses a value of 0.7 V for the forward voltage of the output diode. The simulation parameters used can be seen in Table 2.


Figure 19: Schmidt-Walter Flyback converter diagram, copied from [17]

Table 2: Simulation parameters

| Parameter | Description | Value |
| :--- | :--- | :--- |
| Vin | Supply voltage | 24 V |
| Vout | Output voltage | 5 V |
| lout | Output current | 0.24 A |
| L | Primary coil inductance | $30 \mu \mathrm{H}$ |
| $\mathrm{N} 1 / \mathrm{N} 2$ | Primary to secondary turns ratio | 3.0 |
| f | Switching frequency | 210 kHz |

As seen in Figure 20, the simulated values for the currents and voltages are close to the calculated values in chapter 6 . This is to be expected since the mathematical rules governing the operation of the converter are identical.


Figure 20: Flyback simulation results, as calculated by Schmidt-Walter flyback simulator [17]

### 7.2 LTSpice Simulation

The LTSpice simulation was conducted using the circuit shown in Figure 21. The circuit was largely based on the template LT8301 circuit included in the LTSpice installation's built-in libraries. The transformer model (L1, L2 in Figure 21) was updated based on the used part's datasheet, and the diode model (D1 in Figure 21) was replaced by a part comparable to the one chosen in section 5.4. The load was set resistor was set at $20 \Omega$, representative of a 250 mA current at an output voltage of 5 V .


Figure 21: LTSpice Flyback converter circuit
The simulated primary and secondary winding currents are seen in Figure 22 with their respective peaks and conduction times.


Figure 22: LTSpice winding currents. Primary winding L1 in blue, secondary winding L2 in green.

The simulated primary side conduction time was measured to be $0.78 \mu \mathrm{~s}$, and the secondary side conduction time $1.08 \mu \mathrm{~s}$. The switching frequency was measured to be roughly 256 kHz, which is higher than the estimated 210 kHz frequency in Figure 17. By equation (27), the current waveforms in Figure 22 represent an output power of 1.25 W , assuming an $85 \%$ operating efficiency. This is representative of the expected 250 mA output current at 5 V .

In Figure 23, the switch node voltage is overlaid with the coil currents. The switch node voltage was measured at 41 V at its peak right after transistor turn off, in line with
previous calculations. Due to the lack of transformer leakage inductance in the simulation, the voltage spike induced by it does not present itself in the simulation either.


Figure 23: Switch node voltage overlaid with coil currents

## 8 Mechanical Considerations

The serial connection board was sent in for measurements by the customer. Based on these measurements a 3D model was created using the VariCAD modelling software. The model can be seen in Figure 24.


Figure 24: 3D model based on measurements taken from module

Using 3D models of the D-sub connector, transformer, JST connector as well as a strain relief for the 5 V output power cabling, a rough model was made for the PCB layout and this was fitted inside a 3D model of the enclosure. This was done to avoid running into mechanical constraints after the PCB layout. The PCB was sized to fit a strain relief for the power cable inside the enclosure, and the D-sub connector was positioned in a way
that the enclosure would not interfere with the connection board's handles, and so that the internal JST connector would fit adjacent to it.


Figure 25: Physical layout of components

This preliminary component layout was exported as a wireframe drawing and used as a guide during the PCB design process.

A drawing was made of the new holes to be drilled to the enclosure for mounting the PCB and the strain relief. Holes were added also for the D-sub connector as well as for routing a power cable out of the enclosure. An overview of the modifications can be seen in Figure 26.


Figure 26: Modified enclosure. Existing holes noted with "E"

## 9 PCB Layout

Using the KiCAD EDA software, a schematic was drawn based on the component selections made in chapter 4. Footprints were created for the components that did not have a readymade footprint in the KiCAD libraries. After this, a layout for a prototype PCB was created. The schematic diagram can be seen in Appendix 1 and the prototype PCB layout in Appendix 2.

### 9.1 Component Footprints

Most of the components were in standard packages, so their PCB footprints could be found in the built in KiCAD footprint libraries, or additional free libraries provided by online component retailer DigiKey. New PCB footprints (Figure 27) had to be created for the SMD mounted DB-25 connector, the JST-XH connector and the used transformer. These were made using the recommended landing patterns found in each component's datasheet.


Figure 27: Footprints left to right: JST-XH 3-pin, transformer, D25 connector

### 9.2 Layout Features

For isolation, a keep-out zone ( 1 in Figure 28) separates the 24 V input side from the 5 V output side. At its narrowest, this zone is a little over 5 mm wide providing isolation of roughly 2400 V according to IPC2221B [18] (internal conductors), making the transformer (3 in Figure 28) the limiting factor in isolation with 1500 VAC isolation [8].

The main switching current will be flowing through the supply voltage node (2 in Figure 28), through the transformer (3 in Figure 28), the switching node (4 in Figure 28), through the switching IC and to the ground node. Due to the pin layout of the switching IC, instead
of using a ground route on the top side of the board, the switching IC ground pin is connected to ground using multiple vias positioned close to the pin (6 in Figure 28), leading to the bottom side of the board to the ground plane (Figure 29).


Figure 28: PCB v1 front copper layer
The bottom layer of the board shown in Figure 29 features separate planes for the supply ground as well as the isolated output ground using same sized isolation gaps as the front layer does.


Figure 29: PCB v1 back copper layer
To minimize the electromagnetic interference created by the switching circuitry, the size of the switching node (green in Figure 30) was kept minimal. Due to size constraints on the PCB, the snubber loop (red in Figure 30) remains relatively large.


Figure 30: Switching node (Green), snubber loop (red)

### 9.3 Via Current Capacity

To estimate the current carrying capacity of a via, a calculation method based on a paper published by UltraCAD Design Inc. [19] was followed.

Using the prototype PCB manufacturer's estimate [20] of minimum through hole plating thickness of $18 \mu \mathrm{~m}$ ( $T$ in Figure 31), and a via hole diameter of 0.3 mm , an estimate of
the cross-sectional area can be calculated by calculating the cross section of a hollow cylinder created by the via copper plating as illustrated in Figure 31:


Figure 31: Hollow cylinder cross-section
$r=\frac{D}{2}=\frac{0.3 \mathrm{~mm}}{2}=150 \mu m, \quad T=18 \mu m$
$A=\pi r^{2}-\pi(r-T)^{2}=\pi\left(r T-T^{2}\right)$
$A=\pi\left(150 \mu m \cdot 18 \mu m-(18 \mu m)^{2}\right)$
$\approx 7464 \mu \mathrm{~m}^{2}=7.464 \cdot 10^{-9} \mathrm{~m}^{2}$

The ampacity of an external copper trace according to IPCC221 [18] can be calculated using the following formula:

$$
\begin{equation*}
I_{M A X}=0.048 \cdot \Delta T^{0.44} \cdot A(m i l s)^{0.725} \tag{41}
\end{equation*}
$$

Where $\Delta T$ is the maximum allowed temperature rise of the trace from ambient and A(mils) is the conductor cross-sectional area in square mils. Since a mil is a thousandth of an inch $(25.4 \mathrm{~mm}) 1$ square metre equates to $1.55 \cdot 10^{9}$ square mils:
$I_{M A X}=0.048 \cdot\left(10^{\circ} \mathrm{C}\right)^{0.44} \cdot\left(7.464 \cdot 10^{-9} \mathrm{~m}^{2} \cdot 1.55 \cdot 10^{9}\right)^{0.725} \approx 0.8 \mathrm{~A}$

From this result it can be assumed that the 3 vias on the switching side of the PCB (Figure 32) and 4 vias on the supply connector side should be capable of carrying the rated maximum switch current of 1.2 A continuously, even when considering that using multiple vias will give diminishing returns when it comes to heat dissipation due to the thermal conductivity of the surrounding copper layers.


Figure 32: Ground vias on primary (switching side) of PCB (left) and supply connector side (right)

## 10 Prototype

A prototype PCB was assembled with the layout and component selections listed in previous chapters. Photos of the prototype are shown in Appendix 3. This chapter describes the measurements and observations made on the prototype.

### 10.1 Snubber Measurements \& Calculations

A common method of RC snubber design was followed based on measuring the switching node ringing period after the switch turns-off with and without added snubber capacitance [11]. Adding capacitance and resistance parallel to the transformer leakage inductance (primary coil) essentially creates an LC resonator circuit between the snubber capacitance and the parasitic components, as seen in Figure 33:


Figure 33: Parasitic and snubber "components" -

The un-snubbed circuits resonant period is then given by:

$$
\begin{equation*}
T_{0}=2 \pi \cdot \sqrt{L_{p} \cdot C_{p}} \tag{43}
\end{equation*}
$$

Adding capacitance will result in a longer period:

$$
\begin{equation*}
T_{s}=2 \pi \cdot \sqrt{L_{p} \cdot\left(C_{p}+C_{s}\right)} \tag{44}
\end{equation*}
$$

By manipulating the above equations, formulas can be derived for calculating the parasitic components from the period difference resulting from added capacitance:

$$
\begin{align*}
& T_{s}-T_{0}=2 \pi \cdot \sqrt{L_{p} \cdot\left(C_{p}+C_{s}\right)}-2 \pi \cdot \sqrt{L_{p} \cdot C_{p}} \\
& T_{s}^{2}-T_{0}^{2}=4 \pi^{2} L_{p}\left(C_{p}+C_{s}\right)-4 \pi^{2} L_{p} C_{p} \\
L_{p}= & \frac{T_{s}^{2}-T_{0}^{2}}{4 \pi^{2} C_{s}}, C_{p}=\frac{T_{0}^{2}}{4 \pi^{2} L_{p}} \tag{45}
\end{align*}
$$

The first step is to estimate the parasitic component values by first measuring the switch node ringing when the switch is opened during operation. The circuit was supplied with a 24 V voltage and a $31 \Omega$ load was connected to the output. The initial ringing period was measured to be 25 ns , and the voltage spike on switch turn-off had a peak of 18 V on top of the switch node voltage of $\sim 41.5 \mathrm{~V}$. This resulted the switch pin reaching a voltage of 60 V at the highest peak of the ringing.


Figure 34: Switch off ringing without snubber

After the first measurement, capacitance can be added to the circuit. The recommended value to start with is 100 pF [7]. More capacitance then is added until the period of the ringing is roughly doubled

Adding a 100 pF capacitor resulted in the period lengthening to approximately 37 ns . Increasing the capacitor size to 180 pF resulted in a 47 ns period in the ringing. Using this change in period the parasitic inductance and capacitance could be calculated using equation (42):

$$
\begin{aligned}
& L_{p}=\frac{(47 n s)^{2}-(25 n s)^{2}}{4 \pi^{2} \cdot 180 p F} \approx 223 n H \\
& C_{p}=\frac{(47 n s)^{2}}{4 \cdot \pi^{2} \cdot 223 n H} \approx 71 p F
\end{aligned}
$$

The damping factor for an RLC circuit is given by:

$$
\begin{equation*}
\zeta=\frac{R_{s}}{2} \sqrt{\frac{C_{p}}{L_{p}}} \tag{46}
\end{equation*}
$$

Which can be arranged for the snubber resistance:

$$
\begin{equation*}
R_{s}=2 \zeta \sqrt{\frac{L_{p}}{C_{p}+C_{s}}} \tag{47}
\end{equation*}
$$

From the doubling of the resonant period results that the value of $\sqrt{L_{p} \cdot\left(C_{p}+C_{s}\right)}$ has doubled compared to the un-snubbed, which means the value under the square root has quadrupled. Since the parasitic inductance has remained constant, the capacitance value must have quadrupled, thus giving $\left(C_{p}+C_{s}\right) \approx 4 C_{p}$, and simplifying the snubber resistance calculation:

$$
\begin{aligned}
& R_{s}=2 \zeta \sqrt{\frac{L_{p}}{4 \cdot C_{p}}}=\zeta \sqrt{\frac{L_{p}}{C_{p}}} \\
& \text { Substituting } \quad L_{p}=223 \mathrm{nH}, \quad C_{p}=71 p F, \quad \zeta=1 \quad \text { (for critical damping) } \\
& R_{s}=\sqrt{\frac{223 n H}{71 p F}} \approx 56 \Omega
\end{aligned}
$$

The snubber capacitor value chosen was 220 pF as closest available value to the calculated optimal capacitance of $3 \cdot C_{p}$. The snubber resistance was set at $49.9 \Omega$. After the component changes the performance of the snubber was very similar to the previous measurement, but with the voltage spike reduced by another $\sim 1 \mathrm{~V}$, as seen in Figure 35.


Figure 35: Vsw spike with snubber circuit in place
10.2 Switching Frequency

Using a load resistance of $30 \Omega$, the switching period was measured from the switch node waveform seen in Figure 36 to be approx. $4,83 \mu \mathrm{~s}$, resulting in a switching frequency of 207 kHz .


Figure 36: Switching node waveform

### 10.3 Output Pre-Loading

Due to its minimum load requirement, the controller IC delivers a minimum amount of energy even without any load connected. In testing, this resulted in unnecessarily high voltages of over 20 V on the secondary side if no load was connected. In lab testing disconnecting the load also resulted in high and potentially damaging temperatures of the switching IC in under a minute of operation. This had not been taken to account on the design of the first prototype and was noted as a potential issue, since these voltages far exceed the maximum voltage ratings of the serial converter ICs the circuit will be supplying power to. In the case the serial converter would not pull enough power, the supply voltage could rise and damage the serial converter ICs as well as the power supply IC.

To solve this, the controller IC datasheet suggests using a Zener diode slightly larger than the designed output voltage of the power supply Connected parallel with the load, as shown in Figure 37:


Figure 37: Output preloading Zener

Adding a "1SMA5.0" diode with a $6.4-6.7 \mathrm{~V}$ breakdown voltage between the output 5 V and ground pins resulted in the output voltage staying at $\sim 6.7 \mathrm{~V}$ with no load connected. The 24 V input showed a current draw of 0.7 mA for the circuit, corresponding to a 15 mW power consumption on the secondary side, assuming an $85 \%$ operating efficiency for the circuit.

### 10.4 Efficiency And Load Regulation

The efficiency and load regulation of the prototype was measured at supply voltages of $12 \mathrm{~V}, 24 \mathrm{~V}$ and 36 V , using load resistances of $10 \Omega$ to $\sim 1 \mathrm{k} \Omega$, resulting in output currents of 5 mA to 500 mA . An illustration of the measurement setup can be seen in Figure 38. Tables of the measurement results are shown in Appendix 4. For the $10 \Omega$ load resistance, the second load resistor was moved and connected parallel to the first load resistor. The input and output currents were measured using ammeters (A1, A2 in Figure 38). An additional voltage measurement was taken over a $20 \Omega$ resistance ( V in Figure 38).


Figure 38: Efficiency \& load regulation measurement setup
10.4.1 Nominal Supply Voltage, 24 V

At the nominal supply voltage of 24 V , the efficiency of the converter was measured to be approximately 79 \% (Figure 39). This is below the expected efficiency of $85 \%$, likely due to the converter using a relatively small transformer for the application as a result of size constraints.


Figure 39: Efficiency, Vs = 24 V

The current readings given by the ammeters were noted to be less consistent when compared to currents calculated from the voltage drop over the $20 \Omega$ "shunt" resistor. This is likely due to the internal resistances of the current measurement device, measured to be approximately $6 \Omega$ in the max. 200 mA setting, resulting in a significantly different measurement result in the $100-200 \mathrm{~mA}$ range.

The load regulation (Figure 40) was measured to be $\sim 30 \mathrm{mV}$, equating to $\sim 0.6 \%$, within the normal operational current range of up to 250 mA . At a higher load of 500 mA , the output voltage rose slightly to 5.12 V , resulting in load regulation of $\sim 1.2 \%$.


Figure 40: Load regulation, Vs = 24 V
10.4.2 Low Supply Voltage, Vs = 12 V

Since the switching controller IC is rated to work between $2.7 \mathrm{~V}-42 \mathrm{~V}$, operational characteristics were measured at a lower supply voltage of 12 V , as well. However, under normal operation the supply voltage to the converter is expected to remain constant due to the device connecting to a regulated voltage source.

Compared to the nominal supply voltage operation, the efficiency of converter is slightly higher at 12 V supply, as seen in Figure 41 . With a lower supply voltage, the conduction times of the primary and secondary coils will be longer, likely reducing switching losses in the parasitic components of the circuit.

A slight dip in efficiency can be seen in the "Ammeter" measurement at 120 mA , likely due to a measurement error such as poor connection to the test leads, et cetera.


Figure 41: Efficiency, Vs = 12 V
The load regulation at 12 V (Figure 42) is comparable to nominal operation, at $30 \mathrm{mV} \approx$ 0.6 \% and a slight rise in the output voltage at a higher load.


Figure 42: Load regulation, Vs = 12 V

### 10.4.3 High Supply Voltage, Vs $=36 \mathrm{~V}$

A higher supply voltage within the theoretical operating limits of the converter was tested, setting the supply voltage for the converter to 36 V . As lowering the supply voltage resulted in lower switching losses due to lower di/dt in the transformer coils, using a higher supply voltage resulted in a loss of conversion efficiency, as seen in Figure 43.


Figure 43: Efficiency, Vs $=36 \mathrm{~V}$
At $40 \mathrm{mV} \approx 0.8 \%$, the load regulation at a 36 V supply voltage (Figure 44) was comparable to the operation under nominal and low supply voltage.


Figure 44: Load regulation, Vs = 36 V

### 10.5 Output Voltage Ripple

The LT8301 evaluation board DC2138B manual [21] shows the following instructional image on scope placement for measuring input or output ripple:


INPUT OR OUTPUT CAPACITOR

Figure 45: Proper Scope Probe Placement for Measuring Input or Output Ripple, copied from [21]
The goal of this is to minimize the exposed area of the measurement leads to minimize the effect of interference from the switching circuit or other sources of electromagnetic radiation. Due to physical limitations of the probe used, the length of the measurement leads was longer compared to the instructional image, resulting in $\sim 50 \mathrm{mV}$ spikes showing in the measurement. These are a product of the switching operation of the circuit. In Figure 46, the switching ripple can be seen to be close to 30 mV .


Figure 46: Output voltage ripple ( $100 \mathrm{mV} / \mathrm{div}$ )

The ringing visible in the output voltage lines up with the switching transistor changing state. In Figure 47 the transistor can be seen switching on (closing) at $t=0 \mathrm{~s}$ and switching off (opening) at roughly $t=700 \mathrm{~ns}$.


Figure 47: SW node (pink), Vout (blue)

## 11 Conclusion

The goal of this project was to design an isolated power supply fitting the power requirements set by the serial converter circuit, and the physical and environmental requirements set by the install location.

Based on the preliminary testing done on the prototype, the power supply is capable of delivering the required 1.2 W output power in room temperature at supply voltages varying from 12 V to 36 V . Additional testing is required to validate the operation of the circuit in different temperatures, as well as to measure the EMI susceptibility and emissions of the power supply.

The power supply has been fitted in its install location along with the serial converter module, and fits the physical requirements set for the module concerning the physical dimensions of the device.

Additional tests have been planned to be conducted on the prototype and subsequent revisions of the power supply and serial converter modules, such as EMC testing and testing the operation of the device in different operating temperatures.

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## Appendix $1 \quad$ Prototype Schematic



Figure 48: Prototype schematic

Appendix 2
Prototype PCB Layout


## Appendix $3 \quad$ Photos of Prototype



Figure 50: Prototype PCB before components


Figure 51: Populated PCB (no snubber)

## Appendix 4 Efficiency and Load Regulation Measurements

Table 3: Measurements, Vs $\approx 12$ V

| Vin (V) | $\mathbf{R}$ | lin (mA) | Vout | lout (mA) | Eff <br> (calc.) | Voltage <br> over 20R | I over 20R (mA) | Eff from 20R <br> (calc.) |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| 11.96 | 11.2 | 270 | 5.12 | 500 | 0.792766 | 5.12 | 512 | 0.811792394 |
| 11.71 | 20 | 137.7 | 5.09 | 250 | 0.789163 | 5.04 | 252 | 0.795476745 |
| 11.91 | 40 | 68.5 | 5.07 | 121.8 | 0.756925 | 2.52 | 126 | 0.78302598 |
| 11.89 | 60 | 46.4 | 5.08 | 82.7 | 0.761499 | 1.65 | 82.5 | 0.759657493 |
| 11.99 | 80 | 35 | 5.07 | 62.5 | 0.755094 | 1.247 | 62.35 | 0.753281306 |
| 12.01 | 100 | 28.3 | 5.07 | 50.1 | 0.747337 | 1.002 | 50.1 | 0.747336583 |
| 12.04 | 231 | 12.84 | 5.06 | 21.7 | 0.710262 | 0.435 | 21.75 | 0.711898811 |
| 12.04 | 996 | 3.04 | 5.06 | 5.1 | 0.705051 | 0.1013 | 5.065 | 0.700212559 |
| 12.04 | no load | 1.3 | 6.61 |  |  |  |  |  |

Table 4: Measurements, Vs $\approx 24 \mathrm{~V}$

| Vin (V) | $\mathbf{R}$ | lin (mA) | Vout | lout (mA) | Eff (calc.) | Voltage <br> over 20R | I over 20R (mA) | Eff from 20R <br> (calc.) |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| 24 | 11.2 | 138.3 | 5.12 | 500 | 0.77127 | 5.12 | 512 | 0.78978067 |
| 24 | 20 | 69.2 | 5.09 | 250 | 0.766197 | 5.08 | 254 | 0.778456166 |
| 24 | 40 | 35.5 | 5.06 | 122.1 | 0.725148 | 2.52 | 126 | 0.748309859 |
| 24 | 60 | 24.3 | 5.08 | 82.6 | 0.719492 | 1.697 | 84.85 | 0.739091221 |
| 24 | 80 | 18.73 | 5.07 | 62.5 | 0.704919 | 1.273 | 63.65 | 0.717889082 |
| 24.1 | 100 | 15.26 | 5.07 | 50.2 | 0.692054 | 1.02 | 51 | 0.703082939 |
| 24.1 | 231 | 7.15 | 5.08 | 21.8 | 0.642683 | 0.44 | 22 | 0.648579636 |
| 24 | 996 | 1.74 | 5.08 | 5.1 | 0.620402 | 0.1021 | 5.105 | 0.621010536 |
| 24 | no load | 0.79 | 6.64 |  |  |  |  |  |

Table 5: Measurements, Vs $\approx 36 \mathrm{~V}$

| Vin (V) | R | lin (mA) | Vout | lout (mA) | Eff (calc.) | Voltage <br> over 20R | I over 20R (mA) | Eff from 20R <br> (calc.) |
| ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| 35.6 | 11.2 | 94.2 | 5.08 | 500 | 0.757413 | 5.08 | 508 | 0.769531716 |
| 35.8 | 20 | 48.5 | 5.1 | 250 | 0.73432 | 5.09 | 254.5 | 0.747537868 |
| 35.7 | 40 | 25.1 | 5.06 | 121.6 | 0.686661 | 2.52 | 126 | 0.711506914 |
| 35.7 | 60 | 17.43 | 5.08 | 82.4 | 0.672706 | 1.693 | 84.65 | 0.691074824 |
| 35.7 | 80 | 13.55 | 5.09 | 62.4 | 0.656591 | 1.275 | 63.75 | 0.670795994 |
| 35.7 | 100 | 11.14 | 5.08 | 50.2 | 0.64123 | 1.021 | 51.05 | 0.652087765 |
| 35.7 | 231 | 5.36 | 5.08 | 21.9 | 0.5814 | 0.441 | 22.05 | 0.585381914 |
| 35.7 | 996 | 1.321 | 5.08 | 5.1 | 0.549367 | 0.1023 |  | 5.115 |
| 35.9 | no load | 0.66 | 6.6 |  |  |  |  | 0.550983149 |

