SAVONIA

Motherboard design for an X-ray beam profile monitor system

Jussi Malin

Thesis

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Bachelor's degree

SAVONIA-AMMATTIKORKEAKOULU **OPINNÄYTETYÖ**
Tiivistelmä

Koulutusala Tekniikan ja liikenteen ala	
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Tiivistelmä

Tämän opinnäytetyön tarkoituksena oli kehittää emolevy 64-kanavaiseen röntgensäteilyn profiilinmittauslaitteistoon. Röntgensäteilyn mittalaitteistoa käytetään hiukkaskiihdyttimen elektronisuihkun profiilin mittaukseen ja suuntaamiseen. Tavoitteena oli suunnitella ja valmistaa piirilevyt, jotka mahdollistavat luotettavan ja suurinopeuksisen röntgensäteilyn profiilin mittauksen ja digitalisoinnin. Suunnittelu tehtiin PADS-suunnitteluohjelmistolla Havaijin yliopiston mittalaitelaboratoriossa.

Työ on osa Japanin KEKB-hiukkaskiihdyttimen päivitystä SuperKEKB-kiihdyttimeksi. Päivityksen tarkoituksena on nostaa hiukkaskiihdyttimen elektronisuihkun energia 20 kertaa alkuperäistä laitetta korkeammaksi. Tämä voidaan saavuttaa joko nostamalla elektronisuihkun intensiteettiä tai kohdistamalla elektronisuihku pienemmälle pinta-alalle. KEKB-päivityksessä käytettäväksi menetelmäksi valittiin elektronisuihkun pinta-alan pienentäminen. Tämän seurauksena elektronisuihkun poikkipinta-ala vähenee mikrometrialueelta nanometrialueelle. Tällä hetkellä mittauslaitteistot eivät pysty tunnistamaan nanometriluokan objekteja, minkä vuoksi on kehitettävä uusi laitteisto elektronisuihkun profiilin mittausta varten.

Työn tuloksena syntyi toimiva emolevy sekä laitteiston vaatimat vahvistin- ja digitalisointipiirilevyt. Työssä saavutettiin kaikki emolevylle asetetut vaatimukset.

Seuraava kehitysaskel tulee olemaan 128-kanavainen mittalaite, joka tuplaa kanavamäärän. Pääpaino seuraavan sukupolven laitteen kehityksessä on entistä nopeampi ja laajempi elektronisuihkun mittaus yhdessä nopeamman ja tarkemman AD- muunnoksen kanssa.
Seuraavan sukupolven laitteen mittaustarkkuuden ja nopeuden suunnittelukriteerit päätetään tässä työssä tehdyn laitteen käyttökokemusten ja suorituskyvyn perusteella.

Avainsanat
STURM2, SuperKEKB, Instrumentation Development Laboratory (IDLab), BELLE2

SAVONIA UNIVERSITY OF APPLIED SCIENCES **THESIS**
Abstract

Field of Study Technology, Communication and Transport			
Degree Programme Degree Programme in Electronic Engineering			
Author(s) Jussi Malin			
Title of Thesis Motherboard Design for an X-ray Beam Profile Monitor System			
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Project/Partners University Hawaii at manoa, Instrumentation Development Laboratory			

Abstract

The purpose of this thesis was to develop a motherboard for a 64 channel x-ray beam profile monitor system. The x-ray monitor system is used for measuring a beam profile and alignment of the collider's electron beam. The goal was to design and manufacture circuit boards that would allow reliable and high speed measurement and digitalization of the x-ray beam profile. The development of the motherboard was done at the Instrumentation Development Laboratory in University of Hawaii at Manoa using the PADS circuit board design software.

The work is part of the Japanese KEKB - electron-positron collider upgrade to SuperKEKB. The main goal of the upgrade is to increase the luminosity of the collider to a value 20 times higher than the original value. This can be done by either increasing the beam intensity, or reducing the beam cross section, therefore making the beam more dense. The method used to upgrade KEKB is changing the density of the beam. This means that the cross section of the beam reduces from a micrometer to a nanometer scale. Present devices used to measure the beam profile and alignment of the electron beam cannot detect nanometer scale objects. Therefore, a new beam profile measurement device is needed.

As a result, a fully functioning motherboard was made, along with amplifier and digitalization circuit boards needed for the device. The motherboard reached all of its design criteria.
Further development of the monitoring system will be a 128-channel device, which will double the amount of measurement channels. The focus on the next generation measuring device will be to achieve faster measurement with more samples from each electron bunch, along with faster and more accurate AD conversion.
The desired monitoring accuracy and speed along with other design criteria will be decided based on the experience and performance of the 64-channel device.

Keywords
STURM2, SuperKEKB, Instrumentation Development laboratory (IDLab), BELLE2

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Forewords

This thesis was done for the Instrumentation Development Laboratory at University of Hawaii. During this thesis I learned a great deal of new skills in the field of electronics engineering, as well as improved my existing skills to a higher level. The experience gained from working on an international project and workgroup as well as the improved skills in English will most definitely serve me well in my future career.

I would like to thank Dr. Gary S. Varner for providing this great opportunity for the thesis, and for his guidance during the exchange period.

I would like to address my thanks to my supervisor Ari Suopelto for his feedback and support.

Kuopio 2012

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Jussi Malin

1 Introduction

STURM stands for Sampler of Transients for the Uniformly Redundant x-ray Mask. This project has it's origin in upgrading the KEKB electron-positron collider, shown in Figure 1, at the KEK High Energy Physics Laboratory in Tsukuba Japan to Super-KEKB. When the upgrade is finished, the Super-KEKB will have the world's highest luminosity. This higher luminosity is needed for the upgraded BELLE2 detector, which is used to measure charge-parity violations. The upgrades will allow this experiment to continue with much higher precisions. The BELLE2 detector is located at 7A in Figure 1. The STURM2 measuring device will be installed at close proximity of the point 7B in Figure 1, which is the location of the quadruple superconducting magnet and also the point of collision.

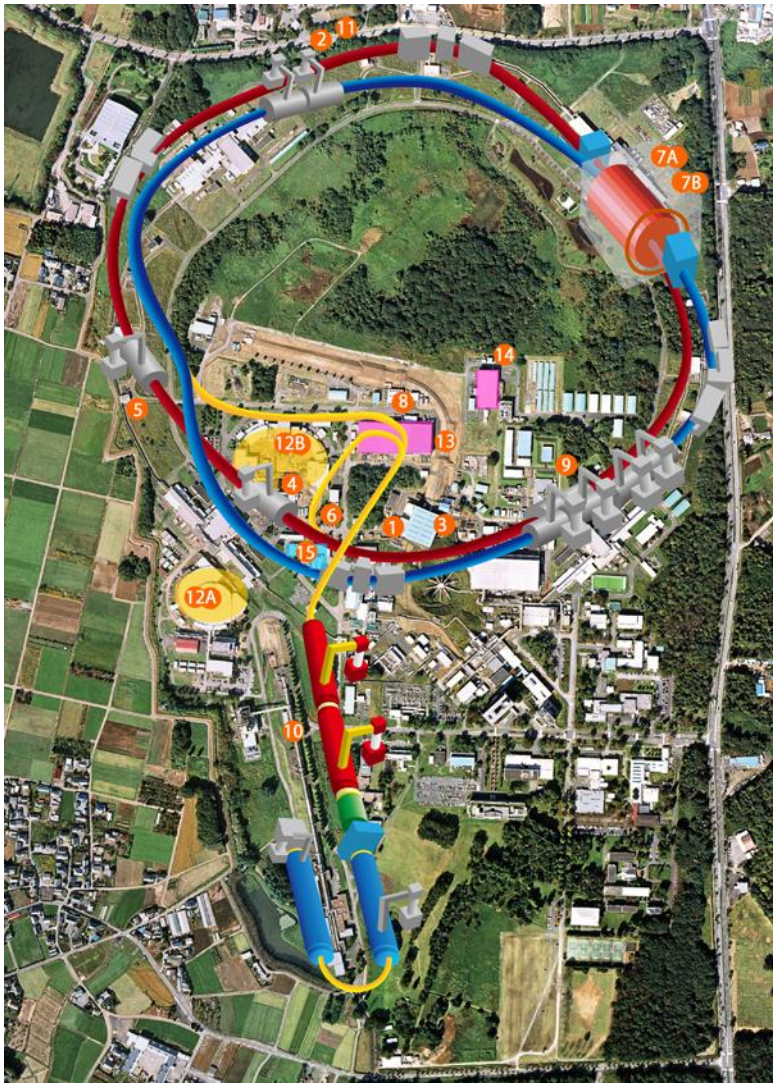


FIGURE 1. KEKB facilities and components. Picture High Energy Accelerator Research Organization, (KEK) 2012

At the Super-KEKB collider, the beams will be squeezed to nanometre scale. Therefore, the previous measuring devices can no longer track the beam at the collision point. Without reliable tracking and monitoring equipment it is impossible to collide the beams with proper accuracy. Also, the collision of the beams will not always happen head on. Depending on the experiment, the beam bunches will be driven together with an 1 to 5 degree angle. The STURM2 can measure the location, profile and angle of the beam right before the collision point, allowing the physicist to adjust the beam as he desires. When implemented, the STURM2 device will be the most accurate real-time, turn-by-turn monitoring system. (High Energy Accelerator Research Organization, KEK).

2 Device performance criteria

The STURM2 monitoring device consists of three key components. A fast fermionics sensor with RF amplification, a 10 to 100 Giga-samples per second digitizer, and a fast acquisition back-end transmitting the data to the main control room. Before setting out to design any of the components, it is crucial to understand the design criteria for all the devices. Before any of the design work was started, the most critical values were calculated. In the Super-KEKB, the most important values are the available time for the measurement, and the amplification needed for the RF signal.

In the Super KEKB collider, the electron bunch travels nearly at the speed of light, which will set a high demand for the measuring speed. In addition, the distance where the sensor can pick up the X-ray beams, is only 5 millimetres. The time T available for the measurement can be found in equation 1.1.

$$T = \frac{L}{V} = \frac{5{,}00*10^{-3}\ m}{2{,}99*10^{8}\ m/S} = 16{,}72\ pS \qquad [1.1]$$

Where

L is the length of the fermionics sensor
V is the light speed constant

To calculate the needed amplification to reach the desired output voltage, the sensor's own output voltage must be solved first. The energy of the electron beam at Super-KEKB collider can reach 4 KeV, meaning that the most energetic x-ray beam can also reach 4 KeV. Depending on the angle of the beam when it passes the sensor, the estimated energy of the beam varies between 2 to 4 KeV. For these calculations, the energy of the x-ray beam was assumed to be 3.6 KeV, which is well between the possible fluctuation.

When the x-ray beams hit the surface of the sensor arrays, they release electron – hole pairs. With the material used in the fermionics sensor, 3.6 electron volts is needed to release one pair. Therefore, 3.6 KeV will release 1,000 electron – hole pairs.
(STURM-based x-ray Monitor Meeting page)

Now the sensor's response time must be taken into account to solve the sensor output current, in order to solve the output voltage. The sensor used in this device has a low-high response time of 0.25 nS as can be seen in Figure 2. When signal intensity changes, the sensors output current changes accordingly. The change from low- to high and high- to low is identical, so the current change ΔI has to be calculated in only one case.

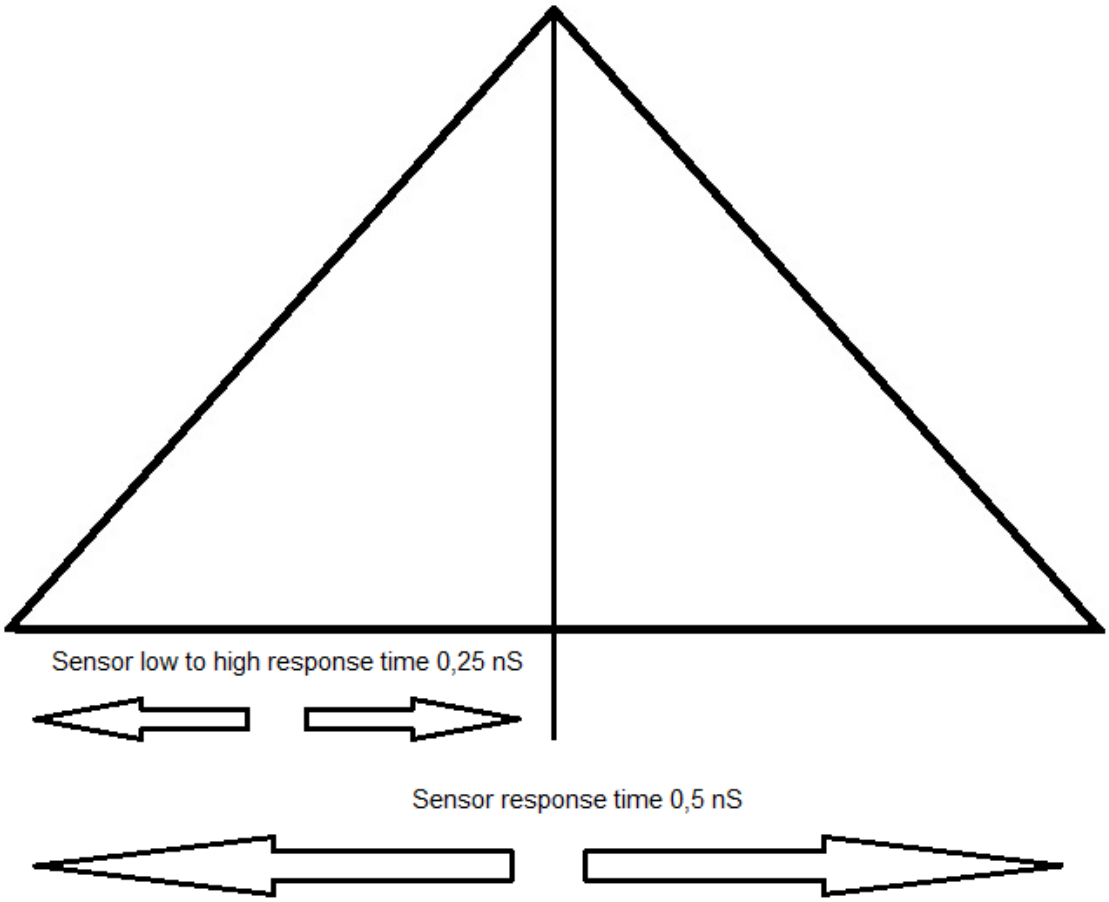


FIGURE 2. Sensor response time.

One electron – hole pair has the charge of 0.16 attocoulomb, Therefore 1,000 pairs will have the charge of 0.16 femtocoulomb. The coulomb is defined by ampere in seconds, so change in amperes ΔI can be solved with equation 1.2. (STURM-based x-ray Monitor Meeting page)

$$\Delta I = \frac{\Delta C}{\Delta t} = \frac{1000i}{2{,}5*10^{-10}S} = \frac{0{,}16*10^{-15}C}{2{,}5*10^{-10}S} = 0{,}64\ \mu A \qquad [1.2]$$

Before setting out to do the design work, the impedance of all RF transfer lines was set to be 50 Ω. Several attributes will affect the impedance of the transfer line, including trace width, height, thickness and the relative permittivity of the dielectric. The impedance fitting was done by changing the trace width, which is the easiest and most cost efficient way. The trace width calculations were done by online calculation software, provided by the PCB manufacturer.

Using Ohm's law, the voltage change ΔV in the 50 Ω transfer can be solved with equation 1.3.

$$\Delta V = \Delta I * R = 0{,}64 * 10^{-6} A * 50\ \Omega = 32\ \mu V \quad [1.3]$$

The 32 microvolt output voltage is too small for accurate measurements. A voltage this small will be lost in the background noise, corrupting the results. Prior to any design work, an output voltage of 10 millivolts was chosen to be an adequate voltage level. The amplification G needed can be solved with equation 1.4

$$G = 20 * Log_{10} \frac{U_{out}}{U_{in}} = 20 * Log_{10} \frac{10*10^{-3}\ V}{32*10^{-6}\ V} = 49{,}89\ dB \approx 50\ dB \quad [1.4]$$

Instead of using one massive amplifier, the amplification was broken into three stages. By doing the amplification in three stages it is possible to remove possible interferences from the signal by placing necessary filters between the amplifiers. Also a design of 20 dB amplifier is less complex than designing a 60 dB amplifier, and can be done in a much shorter timeframe. (STURM-based x-ray Monitor Meeting page)

3 Amplifier board

The STURM2 device holds three amplifiers for each of the 64 channels, a 192 amplifiers altogether. The amplifier board's function is to perform a 20 dB amplification to the sensors RF signal. The amplifier is located on its own circuit board, and it will be plugged in to the STURM2 motherboard. This method has several benefits compared to that if the amplifiers would be physically located on the motherboard. This method makes it possible to change individual amplifiers in case of amplifier failure. In future, if a new version of the amplifier is created with more advanced components, it is very easy to upgrade the device. It is also possible to test individual amplifiers, and remove those boards that do not meet their performance criteria before they are plugged in.

The amplifier board consists of four planes. Primary component plane, power plane, ground plane and RF component plane. These are shown in appendix 2. Along with the amplifier board, another board was also made for testing purposes, called the carrier board.

The carrier board has the same type of connectors as the motherboard will eventually have, and the amplifier board can be plugged into it for performance testing. The benefit of having a carrier board is that the testing of the amplifier design can begin at earlier stages of the project. Carrier boards only function is to provide SMA connectors for the amplifier boards RF input and output signal, and for amplifier board power connector.

The first version of the board used a single connector for the RF input and output and power. This design never reached the design criteria. In the second version of the board, the RF connectors were replaced with solid steel splinters, and the board was connected by soldering these splinters to make a permanent joint. The solder applied by hand caused interferences in the transfer line, and this design was scrubbed as well. The second version of amplifier board is shown in Figure 3, along with the corresponding carrier board. (STURM-based x-ray Monitor Meeting page)

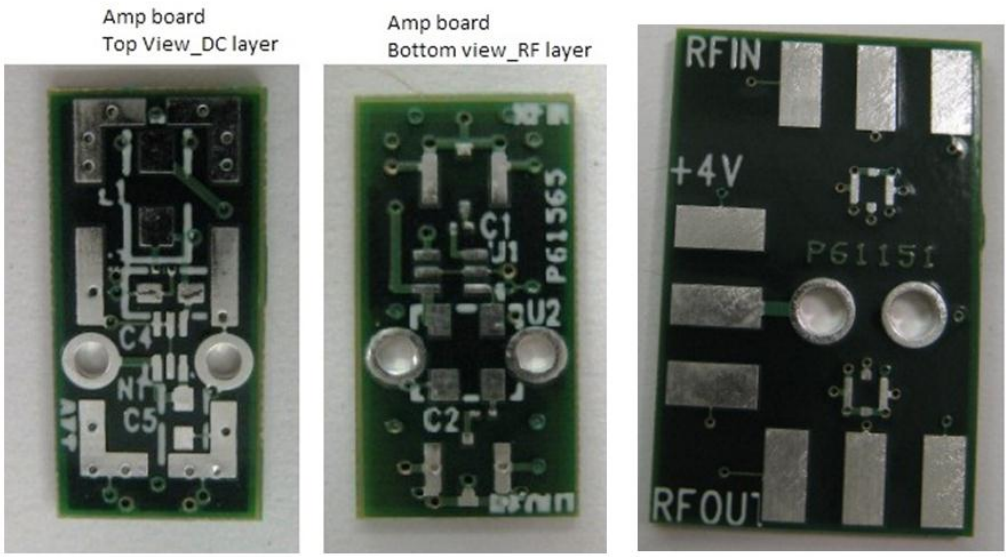


FIGURE 3. Amplifier board version 2. Picture Xi Zhao 2011

The amplifier board used in the device is the third design version. There were two main issues which made the amplifier board design challenging. The frequency of incoming RF signal is over 2 GHz. This combined with the fact that the board has to connect to another board with RF connector caused the main issues. To minimize signal losses, the transfer lines were designed as short as possible throughout the whole device. This meant that the RF connectors used to connect the amplifier board to the motherboard had to have the same impedance as the transfer lines, and to minimize further losses, they needed to be as small as possible. The third version of the amplifier board is shown in Figure 4 along with the corresponding carrier board. (STURM-based x-ray Monitor Meeting page)

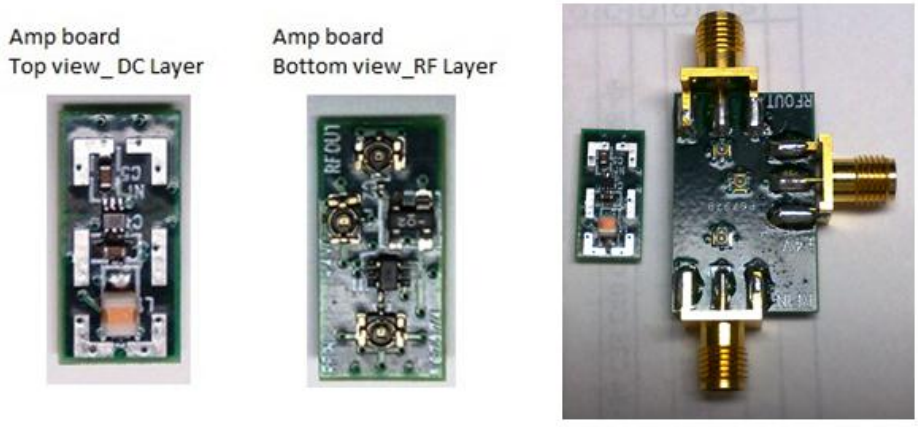


FIGURE 4. Final version of the STURM2 amplifier board and carrier board.

3.1 Amplifier board assembly

The small RF connectors, highlighted in Figure 5, on the amplifier and carrier board made assembly of the boards very difficult. The copper pads on both of the boards are significantly larger than the legs of the RF connector. This means that placement of the RF connector can vary a lot, while it is still within the borders of the copper pad on the circuit board. Alignment of all of the three RF connectors turned out to be a major issue, especially when the tolerances in the RF connector are less than a millimeter.

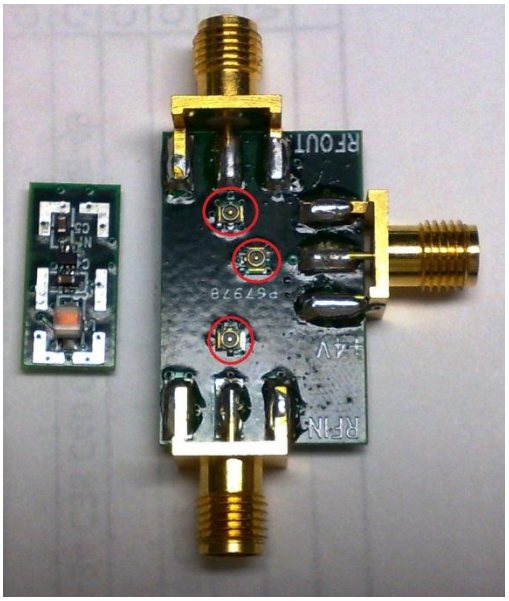


FIGURE 5. RF connectors on the carrier board

Before placing a large order of all the amplifiers, three amplifiers were assembled by hand for testing purposes. The alignment of the RF connectors took several attempts, and the final placement still was not satisfactory. This problem was solved by following method: The connectors on the carrier board were soldered first, and the amplifier board connectors were attached to connectors on the carrier board. Then a small amount of flux was placed on the bottom side of the amplifier board connectors, which were now facing upwards.

The amplifier board was then pressed against the upward facing connectors carefully under microscope. Now the flux on the connectors left marks on the amplifier board copper pads. Using this flux marks it was possible to solder the RF connectors on the amplifier board to proper place.

This kind of method is only good for assembling a few boards, since it is very slow and not accurate method. As a result, one amplifier board only connected properly to one specific carrier board. As a mass production phase, this alignment will be done with proper equipment by a local company where the board assembly is done.

3.2 Amplifier board testing

Testing of the board performance was done using a network analyzer. The network analyzer measures four signal parameters, known as S-parameters. The parameters are split to transmission and reflection. The two transmission parameters tell how much the signal strength changes, and the reflection parameters tell the reflection that happens between the devices input and output port. The Parameters are marked [S21], [S12], [S11], [S22]. In the S-parameters the first number tells the output port, and the second number tells the input port.

What we are interested in the testing phase is the [S21] parameter that tells how much the signal is amplified when it is fed through the amplifier. This measurement is shown in Figure 6, which also shows the performance of the version 2 amplifier, marked revision B.

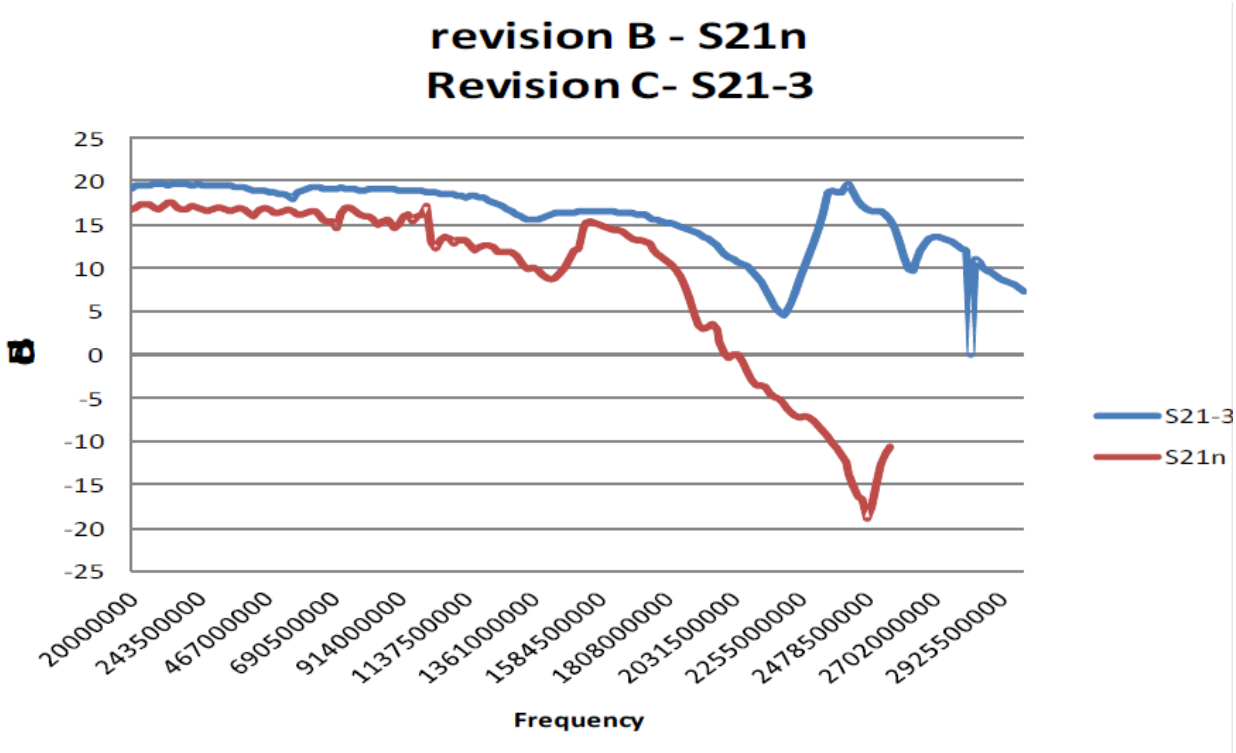


FIGURE 6. Amplifier revisions B and C [S21] parameter, amplification.

In Figure 6 it can be seen that the revision C amplifier will reach the desired 20 dB amplification up to the frequency of 2.5 GHz. Equation 1.4 shows that total amplification needed is 50 dB, which means that one amplifier only has to reach 16.6 dB. However, at 2.5 GHz the amplification drops dramatically. This is caused by the reflection in the output port, parameter [S22] shown in Figure 7. At 2.5 GHz nearly 10 dB of the signal strength is reflected back.

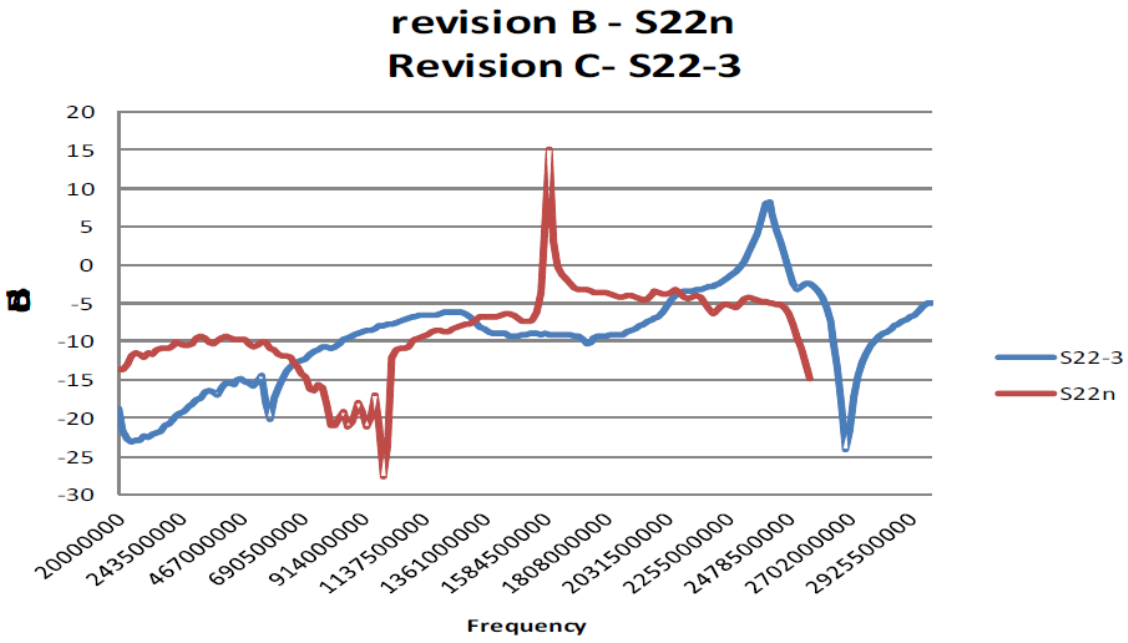


FIGURE 7. Amplifier revisions B and C [S22] parameter, reflection at output port.

Figures 6 and 7 show that amplitude of the reflection matches the drop in the signal output. The performance can be improved by adding a low pass filter to the motherboard between the amplifier stages. The low pass filter will eliminate the reflection spike therefore improving the amplifier performance. This low pass filter for the design was chosen by Dr Gary S Varner. More details about the low pass filter can be found in Appendix 5, pages 3 – 8.

The other remaining parameters are [S12], which tells the change in the signal strength from output to the input port, and [S11], which tells the reflection at the input port. Figure 8 shows that the [S12] parameter is negative. This is because the output signal is much greater than the input. The attenuation in the [S12] is greater than the amplification in the [S21]. This is because all the signal losses in the amplifier board components are also added to the [S12]. In an ideal device, the amplification of the [S21] would be the same as the attenuation of the [S12].

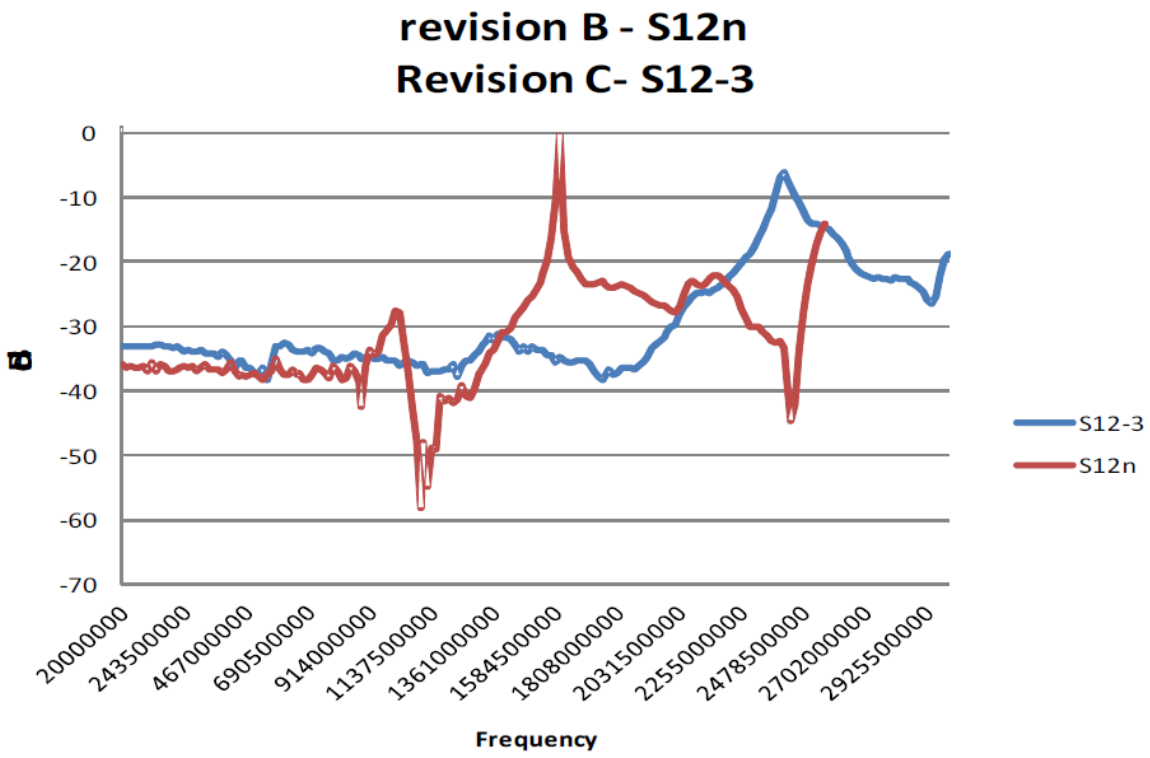


FIGURE 8. Amplifier revisions B and C [S12] parameter, signal strength change from output to input.

Figure 9 shows the reflection in the amplifier board input port. Again a spike appears between 2.25 GHz and 2.5 GHz. This can be also eliminated with a properly matched low pass filter.

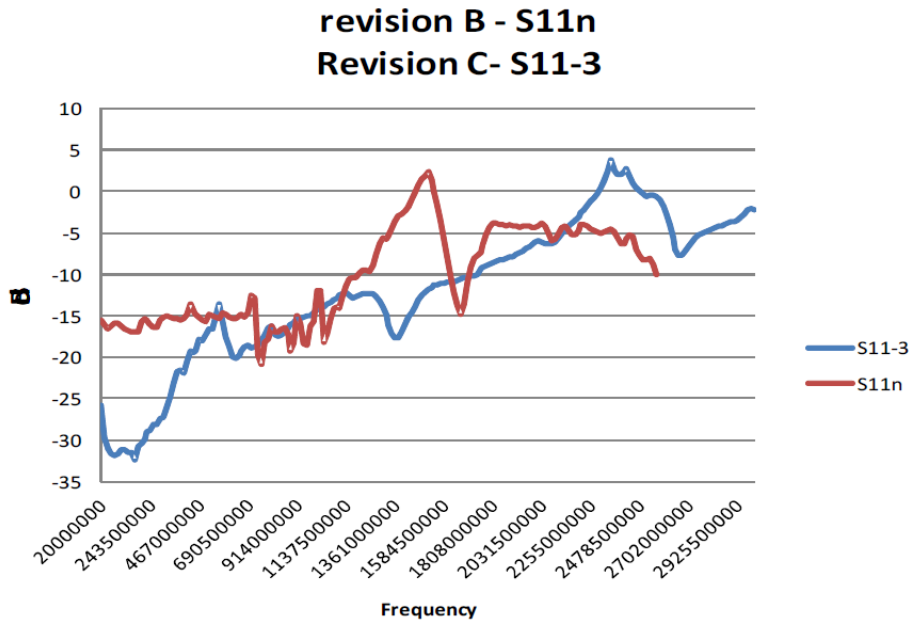


FIGURE 9. Amplifier revisions B and C [S11] parameter, reflection at the input port.

The final phase of amplifier testing is to make sure that all three amplifiers have the same performance. If one of the amplifiers is not performing adequately, the whole amplifier stage is affected, and the results from that RF signal line are corrupted. The three amplifiers assembled by hand and tested individually, and the testing results were plotted into same graph. Figure 10 shows the testing results of these three amplifiers.

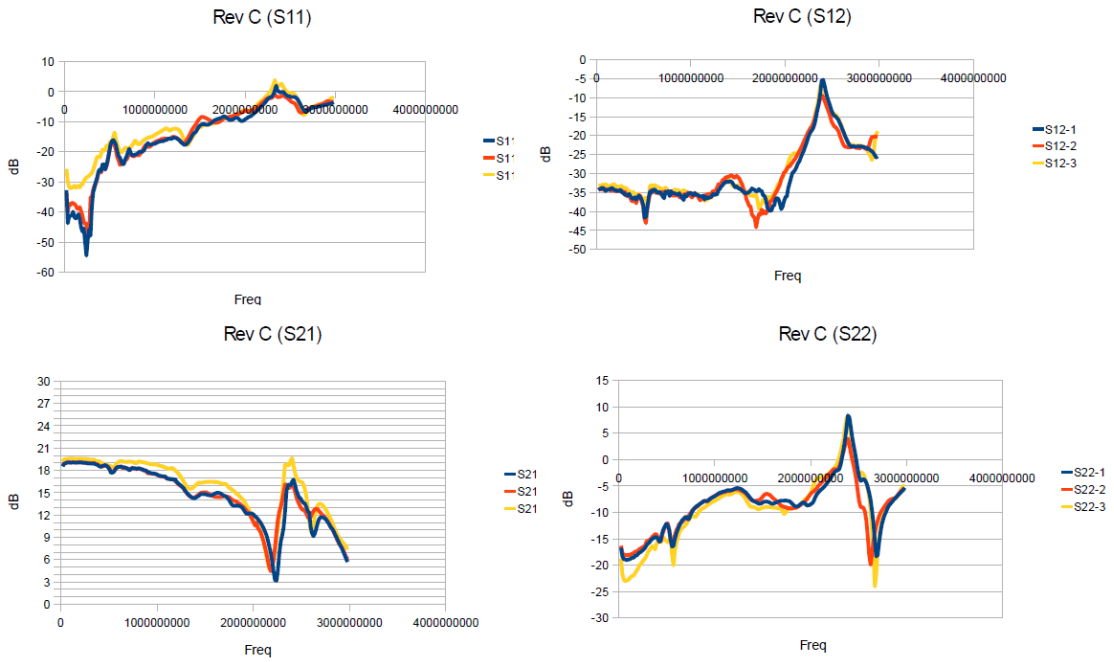


FIGURE 10. Amplifier revision C testing results.

Figure 10 shows that all three amplifiers have a very similar performance. The small differences can be assumed to be caused by the method of how the RF connectors were aligned and soldered. When using proper machinery at the manufacturing process, these differences will be significantly smaller.

4 ASIC board

After the amplifier stage, the signal is fed to the ASIC board. The main function of the ASIC board is to house the STURM2 ASIC chip, provide its operating voltages and supporting devices, and to connect the signal line to the acquisition back-end. The ASIC board processes eight RF signals simultaneously, and it is connected to the motherboard with an 80 pin input and output connectors. The board has four electrical layers, top and bottom for component placing and ground and power as internal layers. The board has two operating voltage levels, 2.5 volts and 5 volts. To ease the routing, the power plane is split into two areas, one for each voltage level, and the components are placed on areas that match their voltages. The schematics and layout of the ASIC board are found in Appendixes 3 and 4.

The board's only input signals are the RF signals from the amplifier stages, and power and ground for the components it houses. The signals that are used to control the STURM2 ASIC are controlled through the acquisition back-end, a device known as SCROD. SCROD is device developed earlier in the instrumentation development laboratory. It is used in various projects to provide connection between digital devices such as STURM2 ASIC and a PC environment. The operation of the STURM2 ASIC is covered more deeply in Chapter 6 of this thesis. (STURM-based x-ray Monitor Meeting page)

To test the STURM2 device as whole, one ASIC board was assembled by hand at the Instrumentation Development Laboratory. Already in the assembly phase, several serious flaws in the design were discovered. The footprint of the input and output connector was poorly designed, making the soldering extremely difficult. The most critical flaw in the design was that the distance between these connectors was also improper, and as a result it could not be connected to the motherboard. Two other critical issues concerning component placement were also found. All these flaws put together, it was impossible to properly test the function of the ASIC board. After completion of the main goals of this thesis, a revision B of the ASIC board was made in which all the design flaws were corrected.

5 STURM2 ASIC

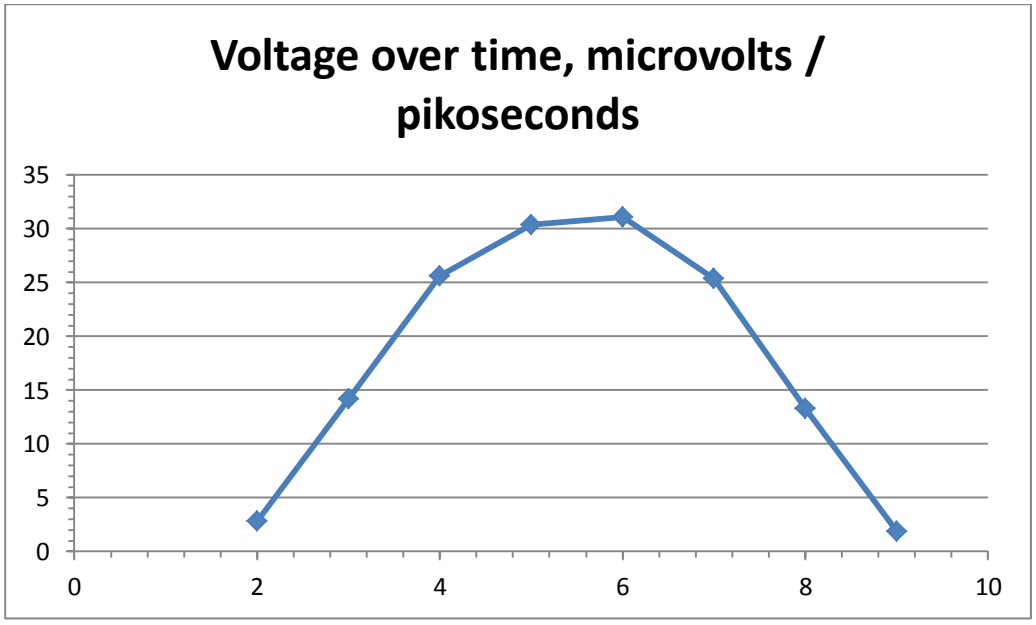
STURM2 ASIC is a chip designed earlier in the Instrumentation Development Laboratory. The main features of the STURM2 ASIC are following:

- Dimensions 3.3 x 3.3 mm
- 8 input channels
- 4 x 8 flash samples/channel
- On chip ADC conversion (~12.5us/256 samples)

Each of the input channels has its own sampling and digitalization circuits built into the chip, so the data of all channels can be processed in parallel. (STURM2 design review, Dr. Gary S. Varner 2009) More detailed information of the STURM2 ASIC signals can be found in Appendix 3.

5.1 Sampling

Each of the channels has 4 flash memory slots, and each of those can hold 8 samples. As the x-ray beam passes through the detector, the measured signal profile is similar to the curve shown in Graph 1. To measure the profile of the x-ray beam, several samples of the signal must be taken.



GRAPH 1. Example of the STURM2 ASIC sampling.

The current STURM2 ASIC version takes eight samples from each channel, and performs a 12-bit AD conversion. The sampling time can be adjusted with four individual TSA lines, which each hold eight voltage delay circuits, shown in Figure 11.

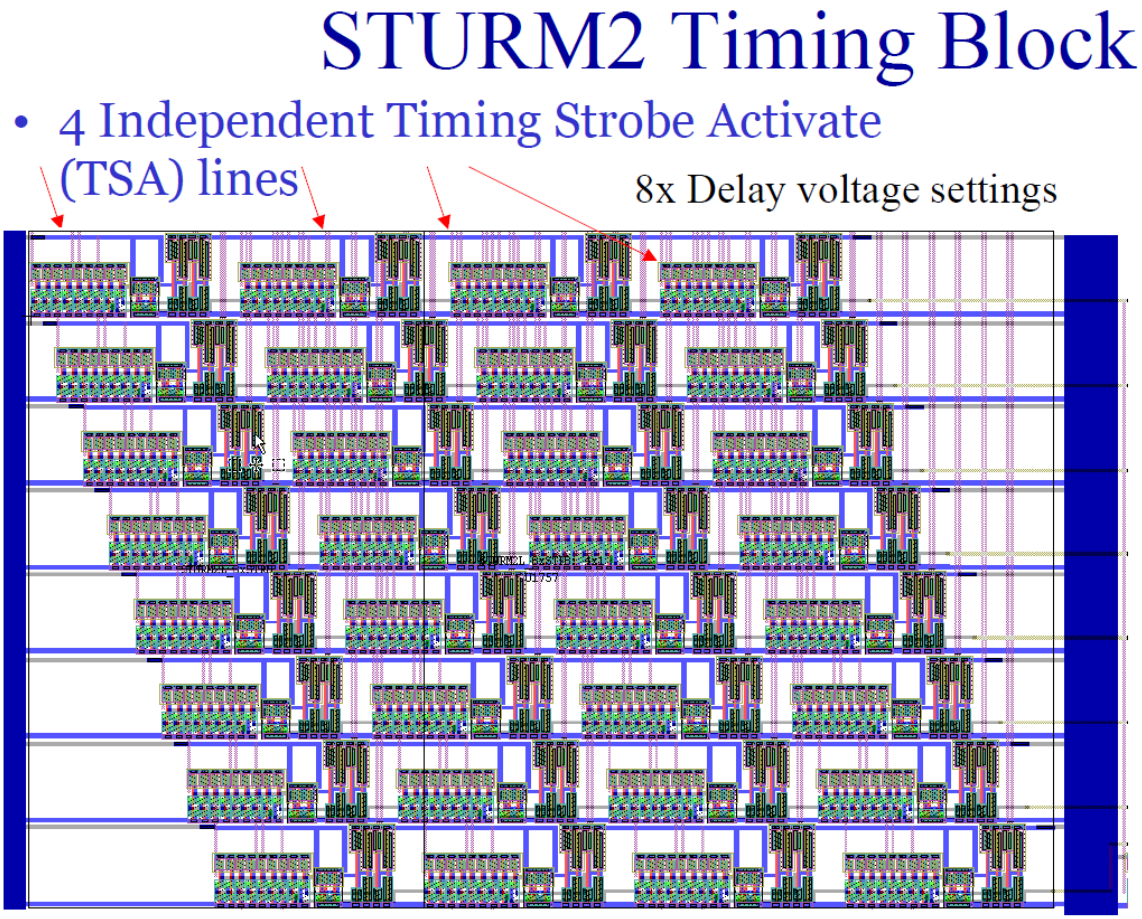


FIGURE 11. STURM2 timing block. Picture Gary Varner 2009

Each of these eight voltage delay circuits can also be adjusted individually with VDLY signals. The physicist using the device can therefore adjust the starting point of the sampling process, and the delay between individual samples.

5.2 Digitalization

To digitalize the analog signal, STURM2 ASIC uses the Wilkinson conversion, which one great benefit is excellent linearity. The main components needed for the Wilkinson conversion are a comparator, ramp generator, gray code counter, and a clock circuit. The principal of the Wilkinson conversion is shown in Figure 12. (STURM2 design review, Dr. Gary S. Varner 2009)

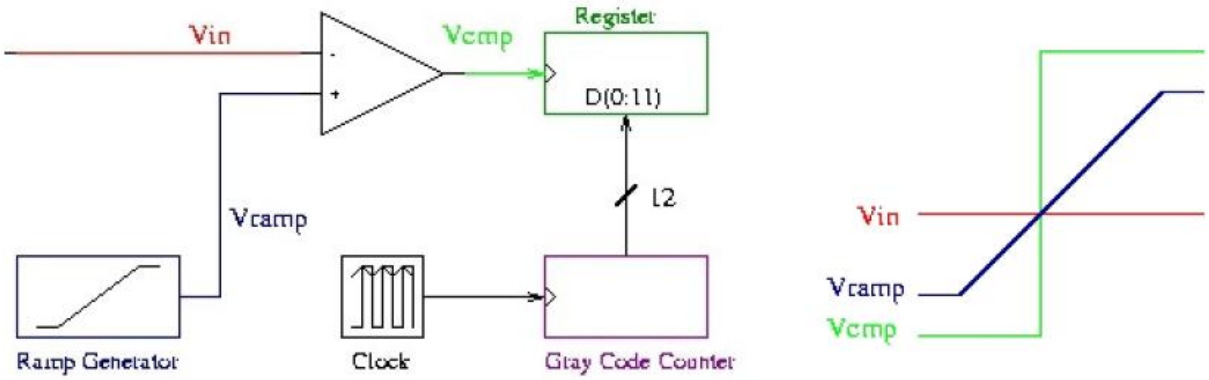


FIGURE 12. Wilkinson conversion.

When the conversion is started, the comparator starts to compare the ramp generator signal to the input signal V_{IN}. At the same time the gray code counter counts upwards, and the counter value is stored in the 12-bit register. Both the comparator and the gray code counter use the same clock. When the ramp generator voltage value equals the input signal value, the comparator sends the signal to the register to ignore future values from the gray code counter. When the value of the each step upwards is known the exact input voltage can be solved by multiplying the register value with the ramp generator step value. Figure 13 shows the good linearity of the Wilkinson conversion. After the ADC, the 12-bit values are then transmitted to the SCROD circuit board, and to the main control room. (STURM2 design review, Dr. Gary S. Varner 2009)

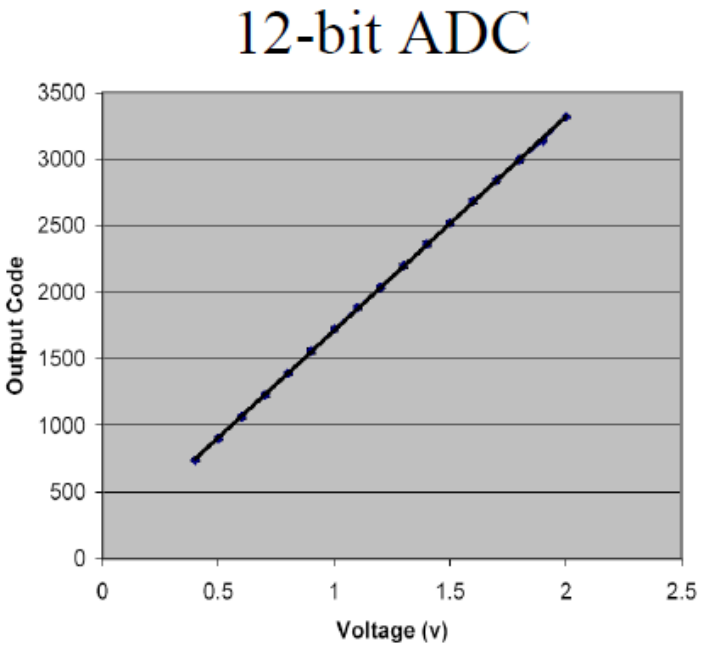


FIGURE 13. Wilkinson ADC linearity. Picture Gary S. Varner 2009. STURM2 design review

6 STURM2 Firmware

The firmware for the STURM2 ASIC was developed by Larry L. Ruckman in 2007. Before implementing the firmware to all of the eight ASIC boards, it is important to test the firmware and perform necessary updates and debugging.

The design environment in this case was Xilinx ISE, and coding language used was VHDL. Physical devices in the testing phase included a unique STURM2 evaluation board, designed at the Instrumentation Development Laboratory along with the STURM2 ASIC chip. The evaluation board allows a direct connection from the ASIC to PC, allowing programming and readout functions. The board also has an input connector for the signal testing. The testing setup was the following:

A signal generator was used to create the input signal, a high frequency sine wave in this case. When the actual x-ray beam passes the sensor, its profile is very close to the sine wave profile, as shown on Graph 1. The same input signal would also be used as a trigger signal that starts the measurement. The testing would focus on single shot testing, in which the evaluation board would stop taking new measurements after one full measurement. Adjusting the constant values in VHDL it is possible to test several different performance values. To readout the data from the ASIC chip, specially designed readout software was used. This software was designed by the same person as the ASIC firmware, Larry L. Ruckman. (STURM-based x-ray Monitor Meeting page)

The testing of the ASIC chip firmware included following steps:

- Sampling rate
  - The sampling rate would be raised by giving a new value for the sample rate constant in the VHDL code after each successful measurement until ASIC could no longer keep up.

- DAC linearity
  - The evaluation board would be connected to the ramp generator, which generates a voltage that increases at each step. The readout software has a function that automatically plots the results. The software is given the value of how much the ramp generator ups the voltage in each step, and the software compares that result to the measured values.

- Analog bandwidth
    - Signal generator frequency is raised after each successful measurement to the point where the ASIC could no longer produce a good quality profile of the beam. The result of the ASIC would be compared to one taken by a high quality oscilloscope.

- Signal noise
    - The exact signal amplitude would be measured in a shielded environment with a high precision oscilloscope. The same measurement would be done again in unshielded environment.

- - 3 dB frequency
    - Signal generator frequency is raised after each successful measurement to the point where the output signal value drops 3 dB.

- Time base VS temperature
    - Measurements above would be taken again, this time the evaluation board would be cooled / warmed between measurements.

The STURM2 evaluation board is unique device, and only two boards are ever made, one located in KEK High Energy Physics Laboratory in Tsukuba Japan, and other in the Instrumentation Development Laboratory in University of Hawaii. When starting the test physical setup, the STURM2 evaluation board could not be located, despite the IDLab has storage unit with very good inventory of all the devices. Last person to use that had obviously misplaced the board. To get the physical setup completed, the other existing board had to be flown in from Tsukuba Japan, with expensive rush air cargo delivery.

After the physical testing setup was in place and the test steps were agreed a number of very serious issues were discovered. To begin with, the firmware VHDL code was broken into dozens of fragments each located in an individual file. To understand how these small fragments came to together to form a functioning firmware requires a careful examining the firmware documentation. In this case, no such documentation existed. Also, the code does not include a single comment line, and many of the signal names and variables were named differently than what was decided at the beginning of the STURM2 project.

The lack of the documentation and comment lines, along with differently named variables made understanding the full function of the firmware extremely difficult. However, with the help of good readout software, it is possible to understand the function quicker by making changes in the VHDL code and examining the effects that they have on the ASIC readout.

The Xilinx ISE design software requires a Windows environment when the STURM2 readout software was designed to be used in a Linux environment. Several different attempts were made to get both of the software to run under one and the same environment, which caused a big delay in the testing process. Eventually it became clear that it was impossible to do so with the equipment in hand. Attempts were made to test the firmware by first examining the code under the Windows environment, and then change to the Linux environment for testing. This kind of working method is extremely slow and ineffective. When combining this with the time it took for the readout software to process all the test data, it was possible to make only few changes a day into the firmware code. As a result of all these issues, the firmware testing was postponed until more suitable testing software could be used.

The issues discovered during the firmware testing were by far the biggest setback during this thesis. But on the other hand, it does serve as a very good example of the way things should not be done. When one person only focuses on his own work and fails to realize the demands and goals of the entire project, the results are unsatisfactory at best. After all these issues were explained to all the people involved in the project, another worker had to be brought in to try make the firmware operational again. Now one person’s lack of following the project criteria caused a double workload and extra costs, not to mention the time lost when software that was supposed to be finished was not.

7 Fermionics sensor

The fermionics sensor is the component that detects the x-ray beams and produces a weak analog voltage signal. The output signal strength and needed amplification is explained in Chapter 2. The fermionics sensor, shown in Figure 14 has 128 detectors. In this design, 64 detectors are used to measure the x-ray beams and 16 detectors are connected to fixed VPED voltage. These 16 detectors with VPED voltage level are located at the edge of the x-ray detectors, eight detectors at both left and the right side. This is to make sure that the unused detectors at the edges of the sensor will not affect the x-ray detectors. The sensor in Figure 14 is already attached to the CPG18020 socket with bonding wires.

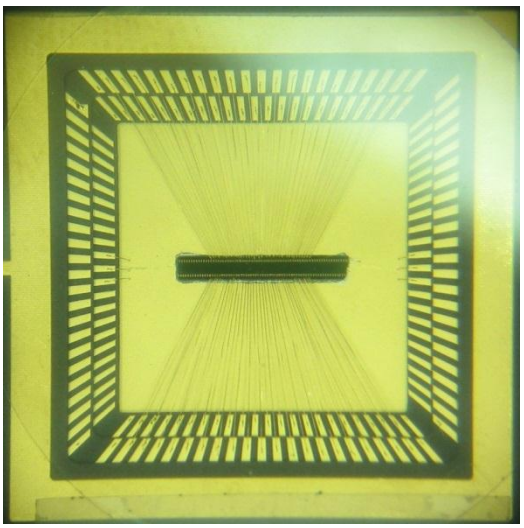


FIGURE 14. Fermionics sensor in CPG18020 socket.

The CPG18020 socket holding the sensor is then attached to PGA socket shown in Figure 15, which is fixed on the motherboard. This is a lever action socket, and the CPG18020 that houses the fermionics sensor can be attached and removed from the motherboard by using the locking lever.

FIGURE 15. Lever operated GPA socket

Installing the sensor by this method provides several benefits. A broken sensor can be quickly replaced, and when a more advanced sensor appears in the future, the device can be quickly updated.

The sensor and both sockets were already manufactured by other companies and were ordered online. The task that remained to be done at the Instrumentation Development Laboratory was to design the most effective bonding option. To accomplish this, there are two main ways of doing it. The first attempt was to design the bonding wires in a way that detector number one on the fermionics sensor would be connected to the lower left corner of the CPG18020 socket, detector number two next to detector one and so on. This would make the routing of the signal line from CPG socket to amplifiers easier and less complex. However, the connection between wire bond pads and connectors in the bottom of the socket are in completely random order. This means that some of the bonding wires between sensor wire bond pads and fermionics sensor detectors would inevitably cross each other, causing short circuits. This design method was found ineffective. More detailed information about connections between the wire bond pads and socket bottom connector pins can be found in Appendix 7.

The other way of designing the bonding wires is to focus on keeping the bonding wires as far away from each other as possible, and completely ignore the bottom connector pins. However, in this kind of approach two other design criteria's must be taken into count. The angle of which the bonding wires connect to the fermionics sensor detectors must be kept as low as possible for better performance.

Also, the wire bonding pads on the socket are located at two different heights. If both the upper and lower row is used, some of the wires would be in top of the lower row. This limited the bonding options into two. The first one allows a higher connection angle and avoid bonding wires to be placed into two different heights, which is shown in Figure 16.

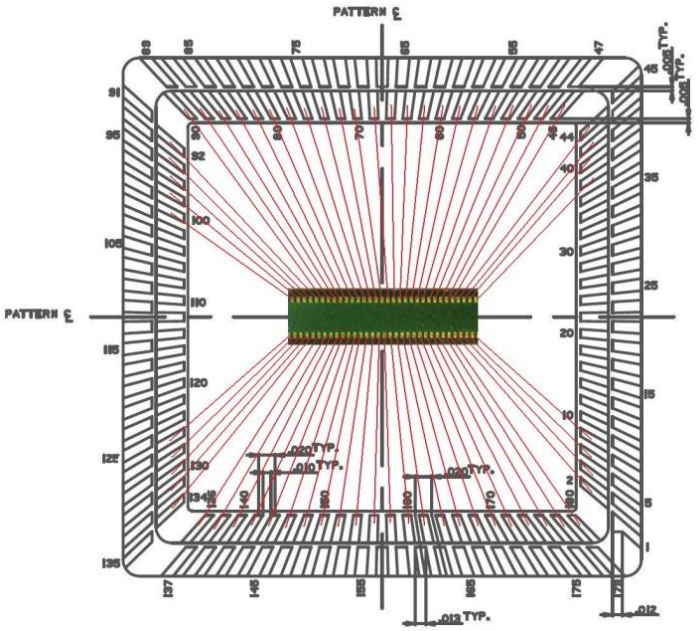


FIGURE 16. Fermionics sensor bonding option 1.

The second is keeping the connection angle as small as possible and allowing the bonding wires to be placed into two different heights, risking a short circuit in case one the upper wires would come loose, shown in Figure17.

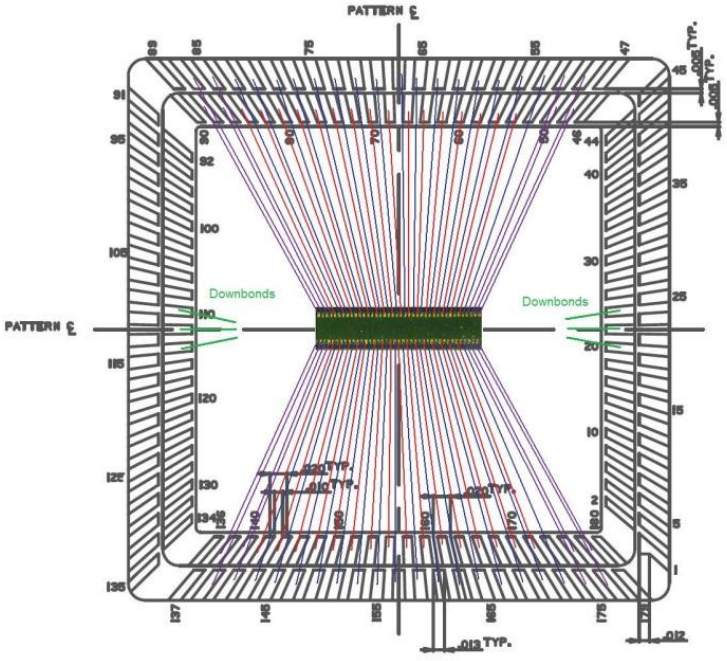


FIGURE 17. Fermionics sensor bonding option 2.

After consulting with experts at the company which would do the wire bonding, option two were the focus is in minimal connection angles was decided to be the better of these two. In addition to the x-ray detector bonding wires the fixed VPED voltage

wires for 16 detectors and six down bond wires were added to design. These down bond wires will be connected to the external voltage source with an SMA connector, thereby enabling an adjusted voltage level. The purpose of these down bond wires is very similar to VPED wires, to keep the bottom plane of the CPG18020 socket at a constant voltage. Finally, a map of the socket bottom pins was created to ease the routing planning. This map is shown in Figure 18. (STURM-based x-ray Monitor Meeting page.)

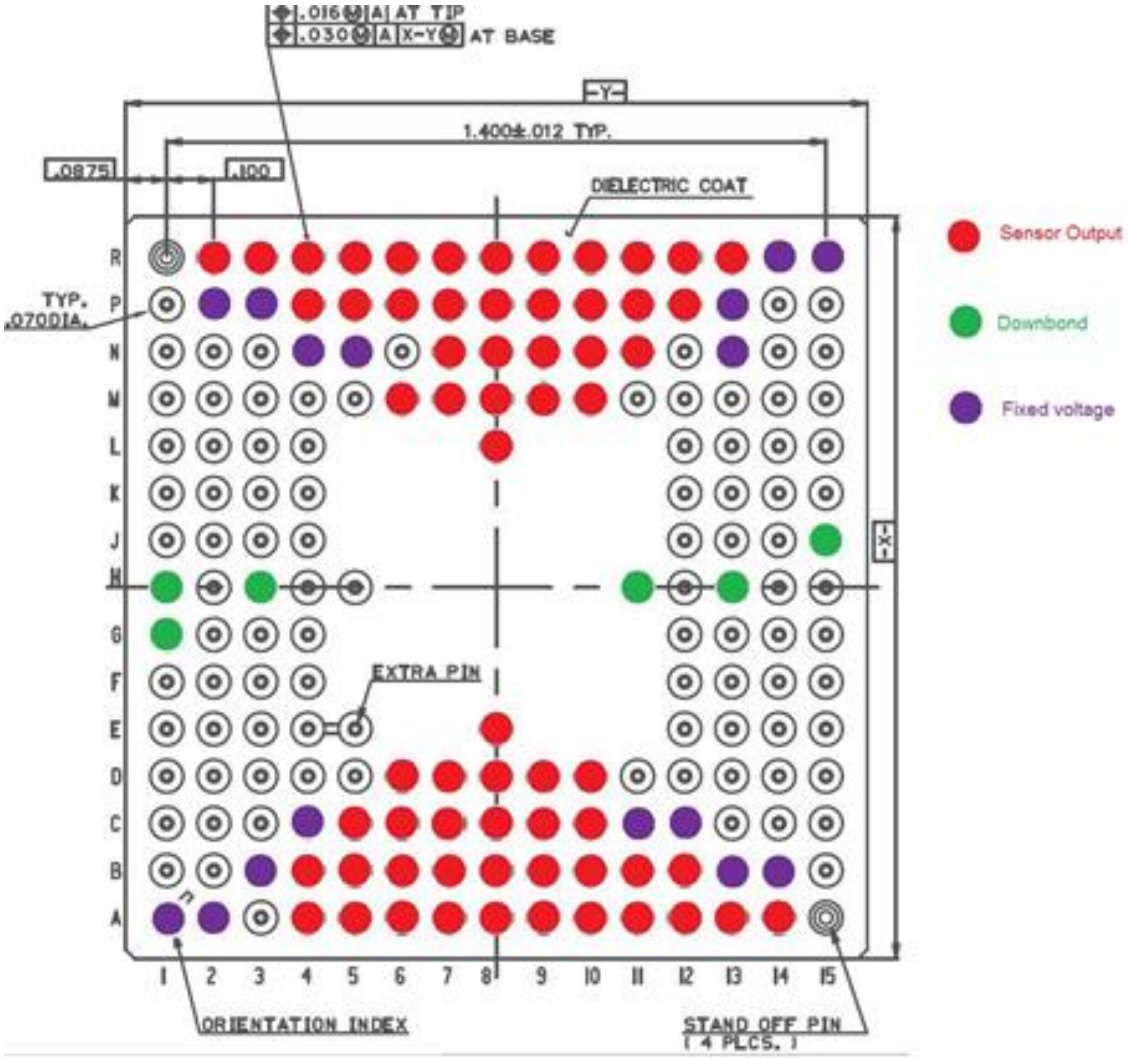


FIGURE 18. CPG18020 pin map.

The actual routing is explained in more detail in Chapter 8.

8 Motherboard

The STURM2 Motherboard is the largest and most complex circuit board in the device, and also the main focus in this thesis. The function of the motherboard is to house all the STURM2 components, provide all necessary voltage levels and power for the other circuit boards, and allow physical attachment to the Super-KEKB. (STURM-based x-ray Monitor Meeting page.) The main features of the motherboard are following:

- Board dimensions 10.9 X 12 inches
- Eight electrical layers
- Houses all other STURM2 circuit boards and components
    - 192 Amplifier boards
    - Eight ASIC boards
    - One fermionics sensor
    - SCROD
    - Two power connectors
    - Five SMA connectors
    - Four ground test points
    - Cooling planes on top and bottom
- Provides operating different voltage levels and power
    - 1.2 volts for SCROD
    - 1.8 volts for SCROD
    - 2.5 volts for SCROD and VPED
    - 3.3 volts for SCROD
    - 4 volts for amplifiers
    - 5 volts for daughter boards
    - Adjustable voltage for down bonds
    - Total power consumption 30 Watts

8.1 Motherboard design rules

Before setting out to place components and starting the routing, design rules were determined. The main factor that influenced the design rules was the company that would be used to manufacture the circuit board. Different companies have different design rules based on the equipment they are using. For this design, a company called Advanced Circuits, based in Denver Colorado was chosen. Advanced Circuits also provides free printed circuit board file check software. It is possible for the customers to upload their designs and have them checked for free. The purpose of this software is to make sure that the company can produce all designs their customers send them. Based on Advanced Circuit design rules the PADS layout design rules were set as shown in Figure 19. In this case, only the clearance rules needed to be set. Other design rules for example including transfer line impedance, was set by hand during routing by chancing the trace width. (PADS PCB Design Tools)

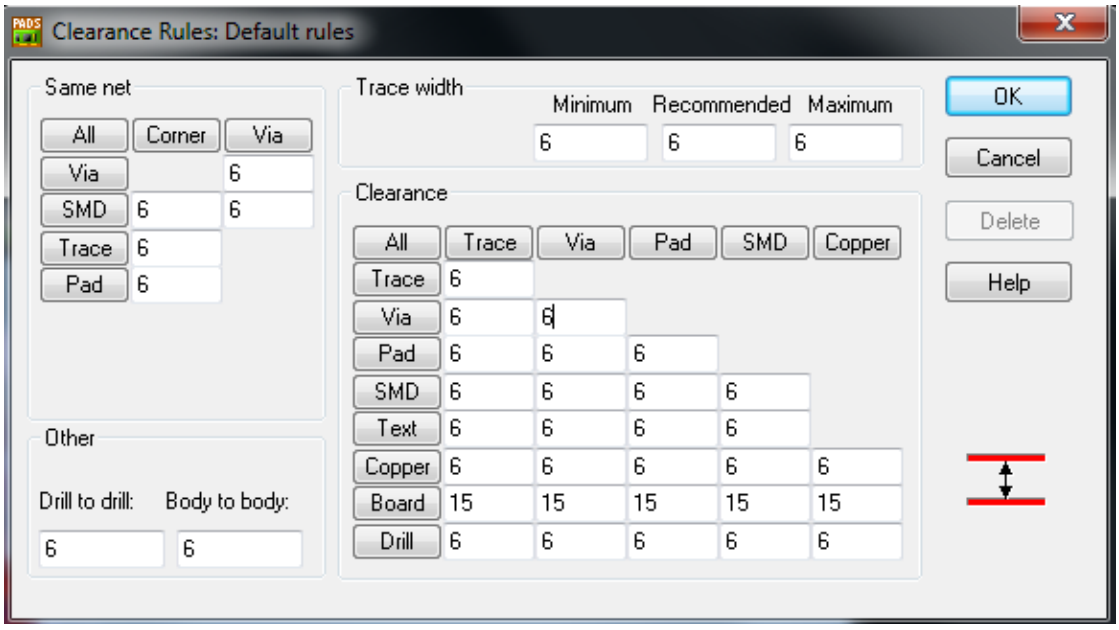


FIGURE 19. STURM2 motherboard PADS layout clearance rules.

Figure 19 shows that all except the clearance from the board sides is six mils. This is a minimum distance Advanced Circuits can handle in their manufacturing process. Despite the fact that the motherboard has eight electrical layers and is relatively large in size, it will have several hundred signal lines. Therefore it wise to allow the traces to be as near as possible to each other, otherwise there would be a risk of running out of space.

The close proximity of two signal lines does also great a risk of crosstalk between two traces. This would be hazardous especially to the analog signal lines from the sensor to the amplifiers. In this case this problem does not arise, since the distance between signal lines is still long enough, and the signal strength is very weak.

Another main design factor is the layer definition. Certain features like copper and plane areas can only be placed on certain type of layers. The layer definition also includes the thickness of the layers, which will have significant impact on the transfer line impedance. The motherboard, amplifier board and the ASIC board must have the same layer thickness in those layers that hold the analog signal, and the trace width must also be equal so that the entire transfer line has the same impedance. Since the amplifier board id the first board that was made, another boards use the same thickness and trace width. Figure 20 shows the layer thickness definitions of all the motherboard layers. More detailed information about layer definition can be found in Appendix 5, page 1.

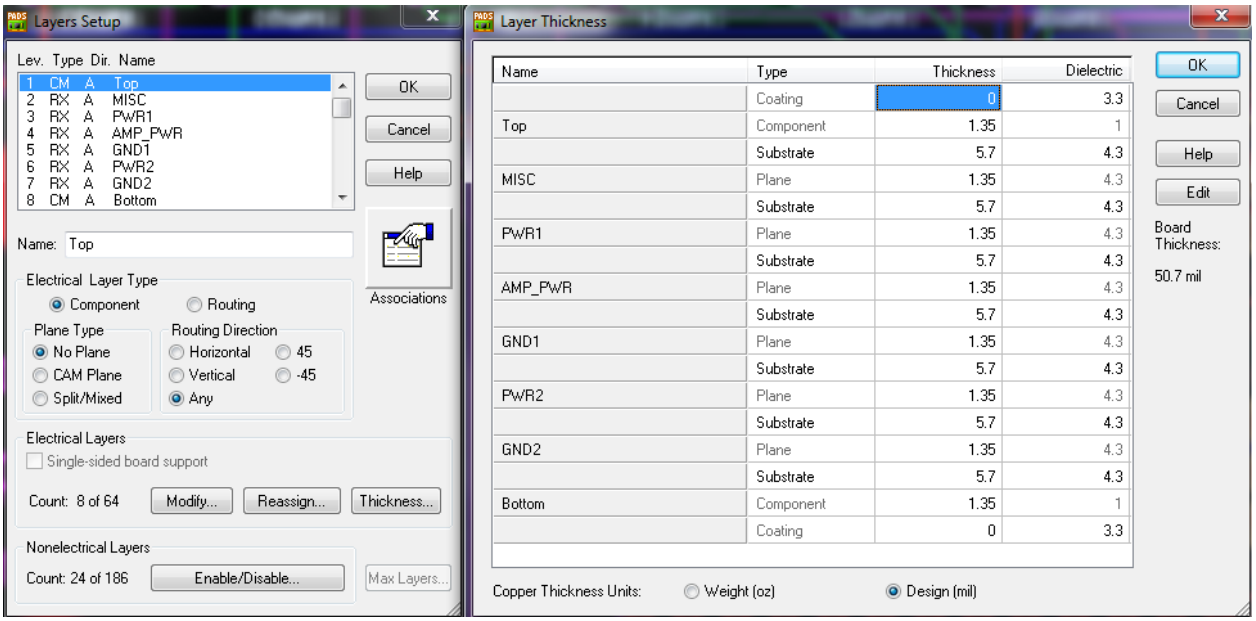


FIGURE 20. STURM2 motherboard layer definitions.

8.2 Component placing

The large area of the motherboard allows the designer to place the components relatively easily with one exception. The signal lines from the fermionics sensor to amplifiers must be kept as short as possible to keep the signal losses minimal. Given the fact that 192 amplifiers must be placed on the board, the logical solution is to place the fermionics sensor in the middle of the board, and divide the amplifiers to the top and bottom layer, surrounding the sensor. Another thing to consider, especially with a large number of amplifier boards, is the distance from one board to another. Since this device is the first of its kind and only one or two will be made, the attachment of the amplifier boards to the motherboard will be done by hand.

The distance between two boards must be great enough to allow easy physical access to each board. The amplifier boards were placed 70 mils apart from each other, which was agreed to be a sufficient distance. The regulators that provide the various voltage levels can basically be located anywhere on the board. The focus was to place the regulators near the components or circuit boards they provide power to.

All the external connections, power, SMA and SCROD where placed on the same edge of the board. This makes the installation of the board easier when only one side of the board needs to be accessible. The several standoffs needed to physically stabilize the board were also put into place at this point. If placed later on, there would be a high chance that at least one of the standoffs would interfere with signal traces. Also the number of standoffs needed is high, 26 in total. This is because the board cannot bend at all in the point when the amplifier and ASIC boards are plugged in. Even a small bent could cause one of the small RF connectors in the amplifier boards to come loose, and therefore corrupting the measurement in that channel.

As explained in Chapter 3.2, a fixed value low pass filter was placed between the amplifiers in each channel so that one low pass filter is between amplifiers one and two and second between amplifiers two and three. A surface mount LFCN 1325 low pass filter manufactured by Mini Circuits was chosen for the design. Between 2.2 – 2.6 GHz it will damp the signal 30 dB, removing the spike found in the testing phase. These filters are shown in Figure 22.

8.3 Power planes and plane areas

To ease the routing, several different power planes and areas were created into the internal layers of the motherboard. Layers 3 and 6 were assigned for power distribution, and layers 5 and 7 for ground. The power planes provide power to different components, while all the ground pins are connected to both ground planes. Since the amplifiers draw by far the most amount of current, they have their own power connector, which is connected to the power plane PWR1 on layer 3. All the other components on the board are powered with the other power connector, connected to plane PWR2 on layer 6. Four different types of plane areas were created for different voltage levels. These plane areas are:

- VPED plane on top layer
- Amplifier power planes on AMP_PWR layer
- VPED plane on MISC layer
- Down bonds plane on MISC layer

The VPED voltage is used in the fermionics sensor as explained in Chapter 7, and in the ASIC board. The VPED voltage level is half of the ASIC operating voltage, and also needed for many of the ASIC inputs. The original plan was use a single regulator to provide the VPED voltage to all the ASIC boards and the sensor. During the design project it became obvious that a better solution would be to use individual regulators for each plane. The ASIC board regulators were moved from motherboard to ASIC board, and plane areas were created around the ASIC board input connectors to make sure all the VPED connection pins would have the exact same voltage level. However, the PADS design software does not understand planes that are tied to same net (meaning they have same voltage), but are not connected together.

The reason why these plane areas are not connected together is following. The output voltage of the same type regulators is never exactly the same, there are always small differences, although they are very small. The regulator with the smallest output voltage would be running at maximum output to keep up with the rest. And like discussed before, it is never wise to run a component on its absolute maximum. Therefore the VPED plane for sensor VPED voltage is named VPED, and the planes for ASIC board are named VPED1 – VPED8. Now PADS realizes that these planes don’t need to be connected to each other, and it won’t give an error message.

Another problem rose during the VPED plane area creations around the ASIC board input connectors on the motherboard. The input has many oncoming connections, and PADS pour manager module had serious difficulties to flood the plane area in a way that would not disturb the other connections.

The problem was solved by changing the width of the traces in the plane area down to 5 mils. As can be seen in Figure 21, the plane area flooding is not solid, but a grid like. The yellow highlighted pins are the VPED pins. This was easier for the pour manager module to handle than a solid pour, and it works equally well as a solid pour.

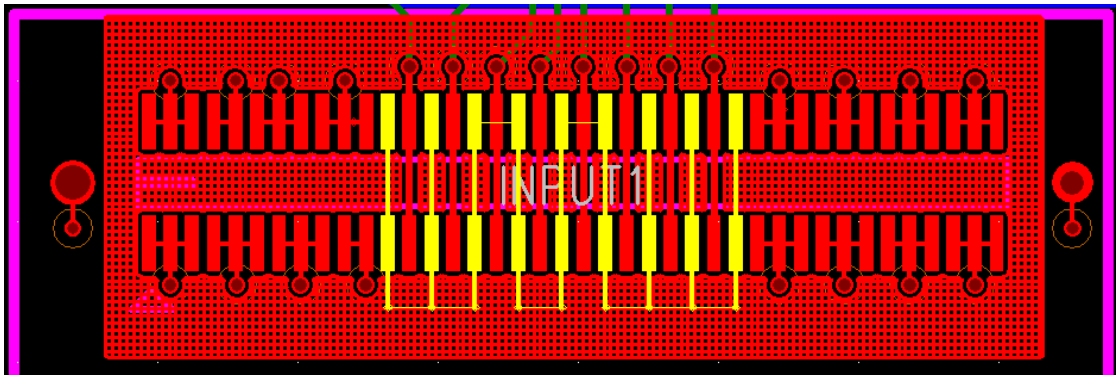


FIGURE 21. VPED plane area around the ASIC board input connector

The amplifier power planes provide power to the amplifiers stages. One plane area provides power to one stage at the top layer and one on the bottom layer. The regulator chosen for this is a surface mount MCP1702, which has the maximum output current of 250 mA. Each of the amplifiers requires 30 mA, measured in the testing phase. Powering three stages of amplifiers would exceed the maximum output, and powering only one stage would take about one third of the maximum output current. Powering to stages with one regulator takes 70 % of the maximum current, which does not stress the regulator needlessly.

Similar to the VPED planes, all the amplifier power planes are separated and given a different name. Figure 22 shows the amplifier plane areas, and the plane drafting properties window. The area of amplifier stage 0 is highlighted. The Figure 22 also shows the placements and connections of the MCP1702 regulators, labeled V5 – V11 in Figure 22.

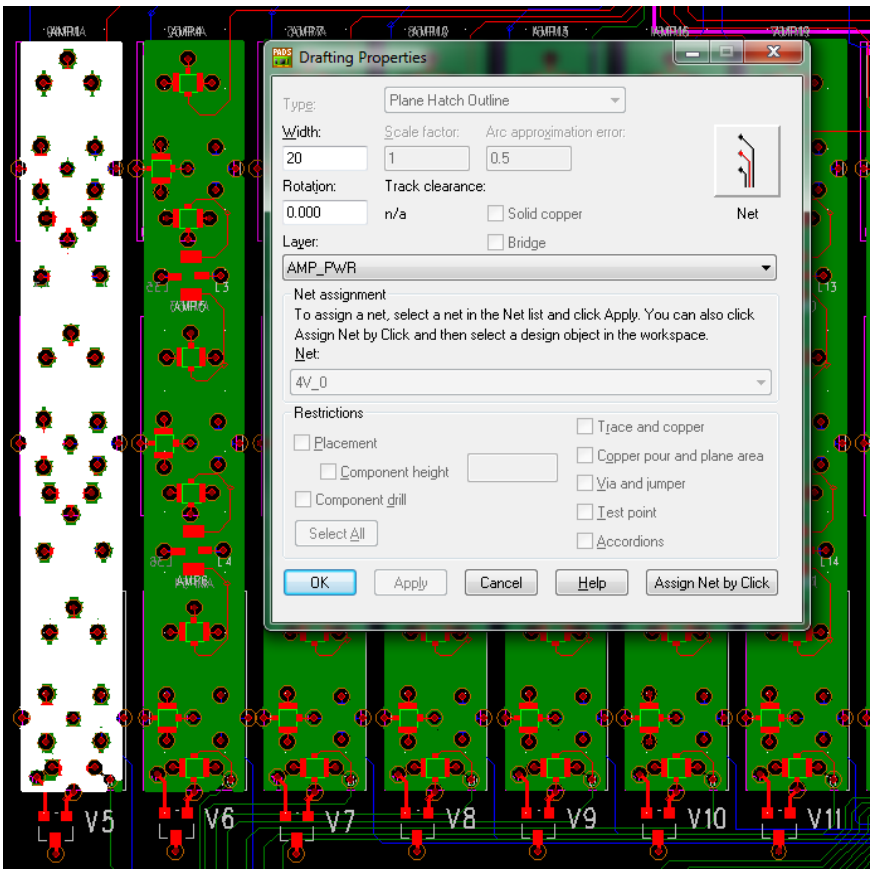


FIGURE 22. Amplifier power planes.

The MISC plane holds three plane areas, two for the VPED voltage, and one for down bonds. Figure 23 shows all these planes. The VPED planes are in the top and lower edge of the sensor socket, with corresponding pins highlighted yellow, on the left side of the picture. The left side of the Figure 23 also shows the connection of the VPED regulator. More detailed schematic can be found in Appendix 5, page 2.

The right side of the Figure 23 shows the down bonds plane area with corresponding pins highlighted yellow, and the low pass filter with 100 MHz cut off frequency. (STURM-based x-ray Monitor Meeting page.)

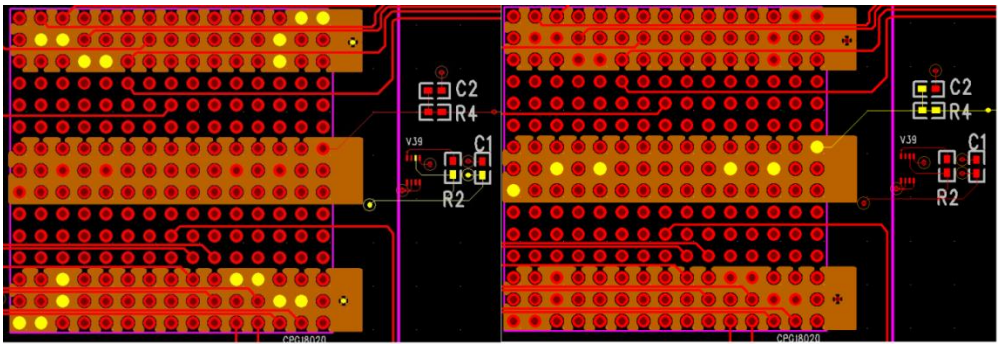


FIGURE 23. VPED and down bond plane areas on the MISC layer.

8.4 Analog signal routing

Analog signal routing, especially the signal lines from sensor to amplifiers is the most crucial. This was the first phase of the routing. These signal lines have the highest priority. To route the signal lines to sensor pins, four different layers were used. Other four layers in the design are reserved for power and ground. The sensor routing is shown in Figure 24. To make the Figure 24 clearer to read, only the signal traces are shown.

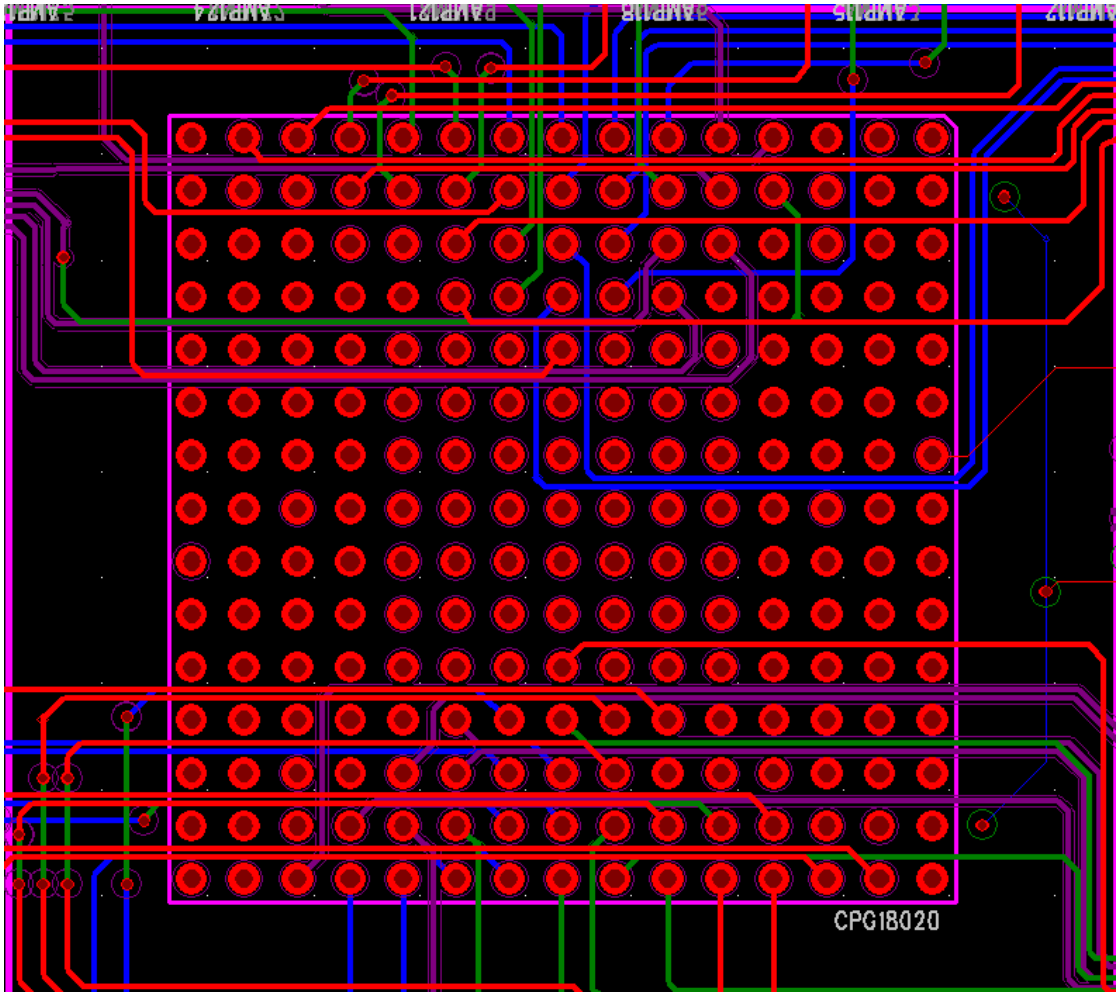


FIGURE 24. Fermionics sensor routing.

Figure 24 shows that the routing turned out to be very complex. Many of the pins located on the right side of the sensor need to be routed to amplifiers located on the left side, and visa versa. What made routing more difficult was that only two traces could pass between two sensor pins. This phase of the routing was the most difficult and time consuming.

Since the sensor pins are in completely random order, it is very difficult to plan the whole routing beforehand. Also the placement on the signal lines 0 – 31, shown at bottom edge of the sensor in Figure 24, is very different from the placement of the signal pins 32 – 63. It took several attempts to complete the routing. In all cases, the four last ones were the most difficult, since nearly all the room between sensor pins was already used.

The other routing part done by hand was the connections on the several regulators needed for the SCROD. The SCROD requires four different voltage levels. The schematics and layout of these regulators is shown in Figure 25.

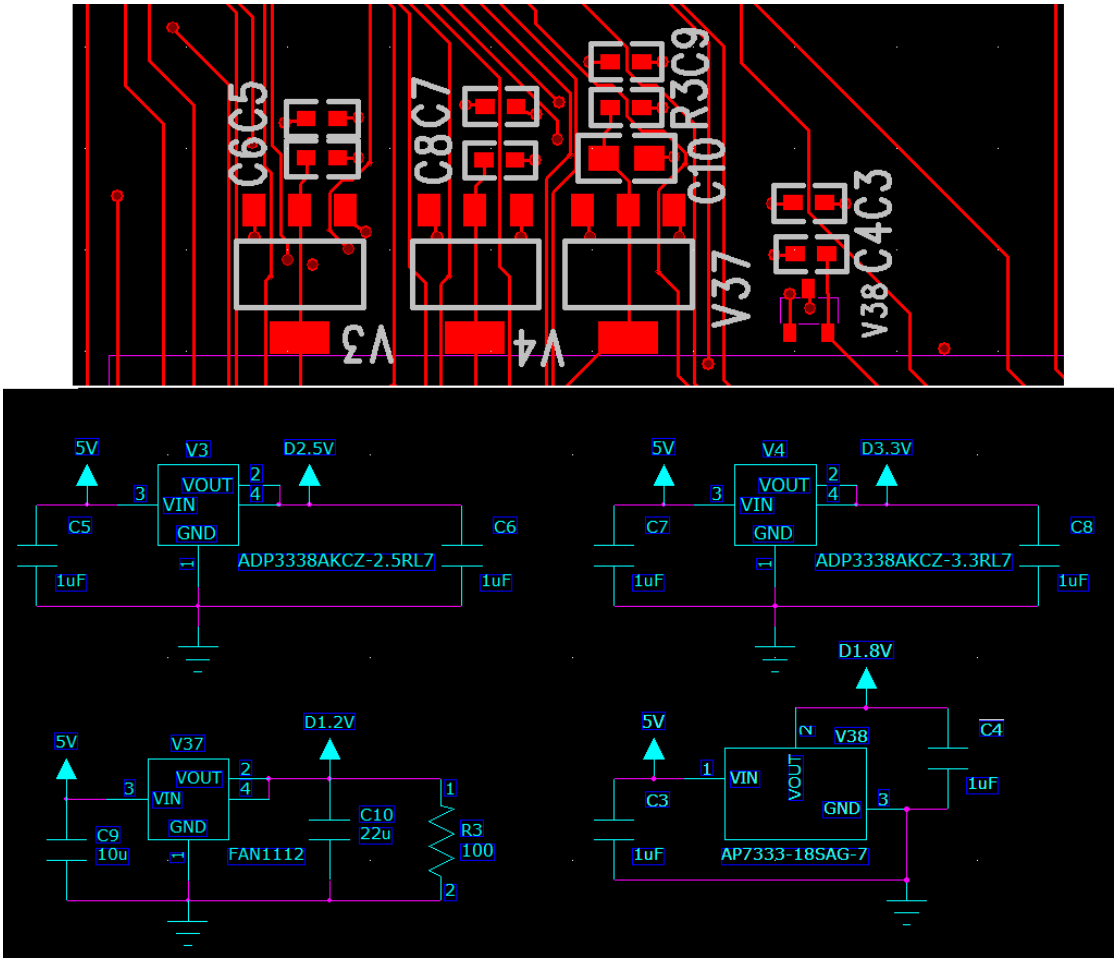


FIGURE 25. SCROD regulators schematic and layout.

8.5 Digital signal routing

The digital signal routing includes the signals from ASIC board's outputs to SCROD. The SCROD footprint was taken from Instrumentation Development Laboratory footprint library and attached to the motherboard design. The SCROD was designed with large number of input pins, 440 in total so it would meet all the demands for several years to come. This design was already pushing the limits of the input pins with 399 digital signal lines. Figure 26 shows all the signal lines in the motherboard design. The digital signals are those that connect SCROD, located in the middle at right side of the Figure 26 to the eight ASIC boards, four on the lower and four on the upper edge of motherboard.

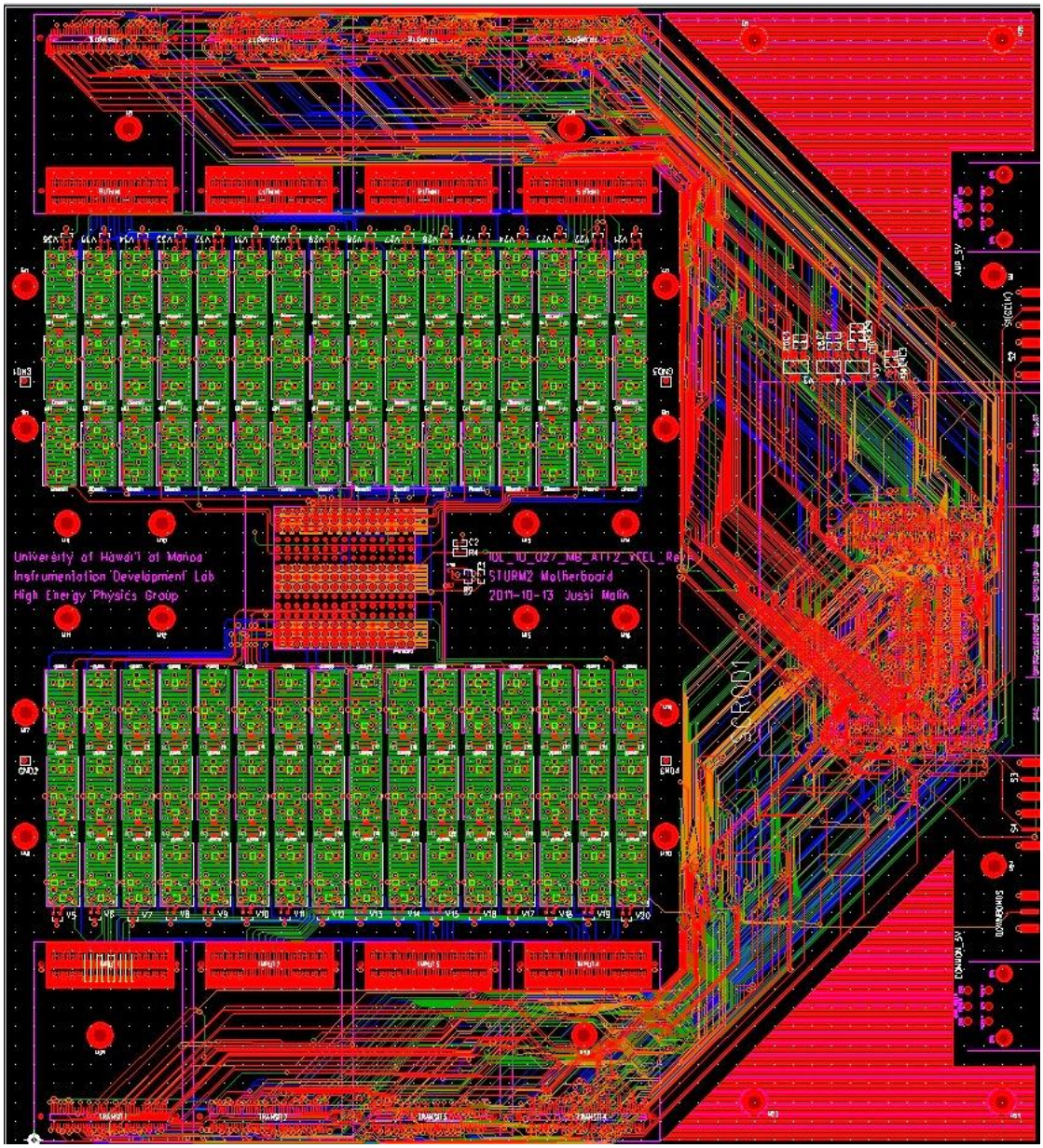


FIGURE 26. Motherboard signal lines.

For the digital routing, the PADS has the auto router module, which is very helpful when dealing with a such high number of signal lines. When starting PADS router, designer can setup the routing strategy, which has great impact on the routing result. Designer can also choose to let router work on the background while continuing with other design work. Figure 27 shows the auto router link window and various action options.

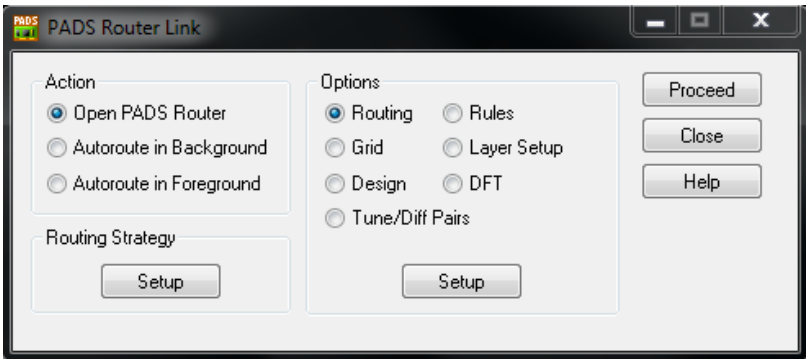


FIGURE 27. PADS router link window.

The routing strategy is the most important setup in the routing process. Modern software's can do the routing many times faster than any human could, but they have absolutely no understanding how the design is supposed to work. The more detailed information the designer can give to the router module, the better the outcome is. Figure 28 shows the various routing strategy options. (PADS PCB Design Tools)

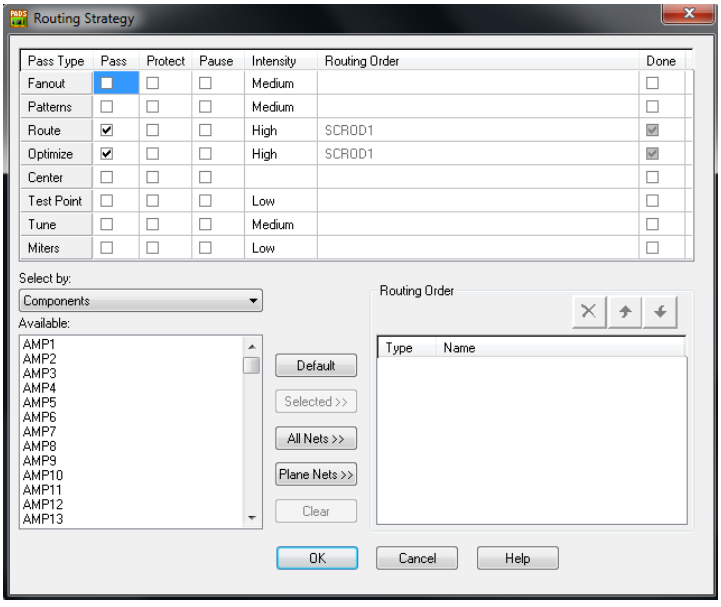


FIGURE 28. PADS routing strategy options.

In this design, the two most important types of actions are routing and optimizing signal lines. Designer can choose the routing in either by component, net, or length. When choosing routing by component or net, the designer can choose which nets or components have the highest priority.

Having a software doing most of the work sounded easy at first, but once again a several issues were discovered. After the first routing attempts, 14 -18 signal lines were always left unrouted, with absolutely no room to route them by hand. The auto router module was also overwhelmed by the number of signal lines and crashing constantly. The attempt to fix this was to let the auto router optimize the signal several times and route only the signal lines that were left on the first run. But when the router module managed to connect one signal line, it deleted another one.

The second strategy was to route the signal lines by component, in this case one ASIC board output connector at a time, then optimize those signals and route next ASIC board. This was many times slower, and routing all the ASIC board took between 6 - 7 hours. Still the results were only slightly better, with at least dozen signal lines left untouched. Third strategy was to route the ASIC boards in groups of four, lower and upper side at different time, and divide the routing to different layers. When this also failed, routing the whole board by hand was seriously considered, but found even more time consuming.

Finally, the routing was accomplished by routing the signals in small groups and forcing the router module to use specific paths and layers by adding keepouts with PADS layout. A keepout is an area which designer has locked, and auto router cannot use that area. After routing of a small group of signals, typically 15 – 20 at the time, the signal lines were optimized and new keepouts were added using PADS layout. This meant bouncing the design back and forth between two software's. The digital signal routing which was supposed to be 8 hour work, turned out to be over two weeks. Since the auto router was also very unstable, a backup copy was made after each attempt. The design that passed the PADS layout connectivity test, was routing design number 48. (STURM-based x-ray Monitor Meeting page)

8.6 Finalized board

Figure 29 shows all the main components of the motherboard, and Figure 30 shows the manufactured board.

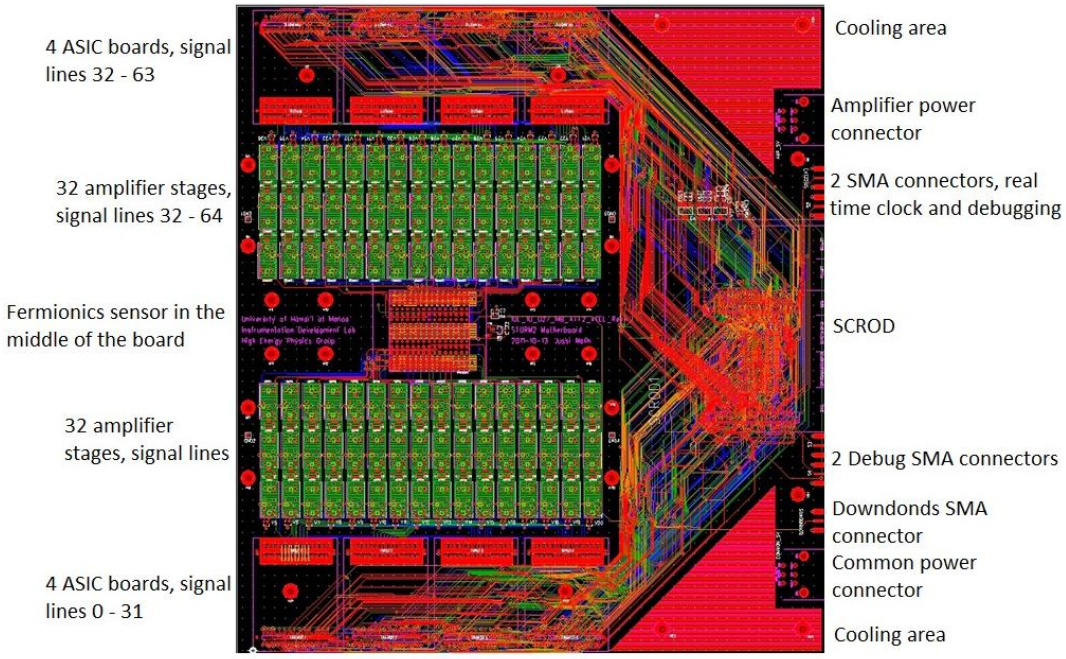


FIGURE 29. STURM2 motherboard main components.

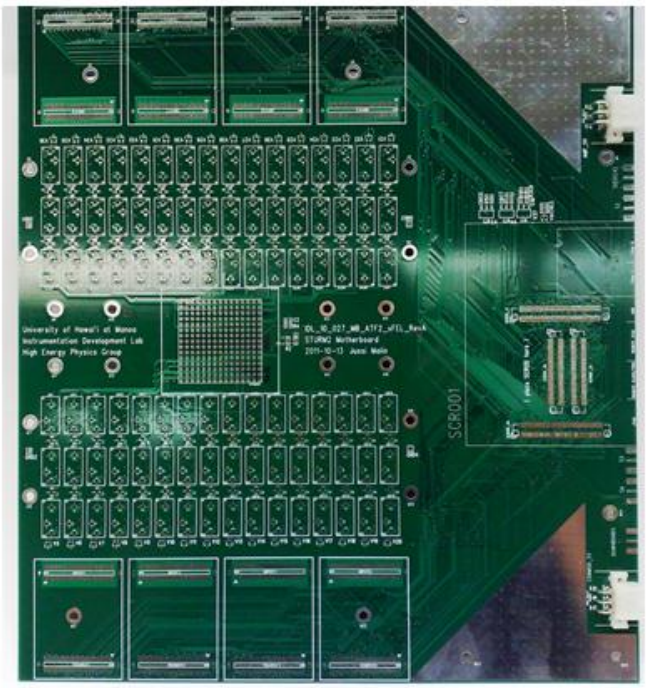


FIGURE 30. STURM2 motherboard.

9 Hardware testing and verification criteria

Hardware testing at IBLab includes testing of the fermionics sensor, motherboard, and amplifier and daughter boards. The test has two phases:

9.1 Testing phase 1

The fermionics sensor, motherboard and amplifier boards are tested by using an infrared beam. Sensor and amplifier boards are plugged into the motherboard, and a high intensity infrared pulse is fired at the fermionics sensor. It takes 3.6 electron volts to release one electron-hole pair from the sensor This signal from the sensor is then fed through a three stages of amplifiers, each having a 20 dB amplification.

When the intensity of the infrared beam is known, it is possible to calculate that the amplifier stage reaches the desired 60 dB amplification. This test is not very accurate since the infrared beam used in the testing cannot reach energy levels high enough. This test is used to verify that all the connections and bonding wires are intact before moving onto a more high scale testing.

9.2 Testing phase 2

A second phase is to test the same configuration with a more powerful beam source. A FEL (Free electron laser) is used for this test. A microwave pulse is fired, and the beam is bent with infrared laser and optical storage cavity, and guided into the beam dump. When a microwave pulse is bent, it emits X-rays. This is the same principal as how the device is going to be used at KEKB collider. The X-ray beam is focused with a collimator, and its intensity is measured. After this the X-ray beams hit the fermionics sensor located at the STURM2 motherboard.

Now it is possibly the compare the results from the beam intensity monitor and STURM2 to make sure the hardware works as designed. Figure 31 illustrates the testing set up.

After this it is possible to move on to firmware testing, and start to take readouts of X-ray beam profile, which is the main function of the device. (STURM-based x-ray Monitor Meeting page)

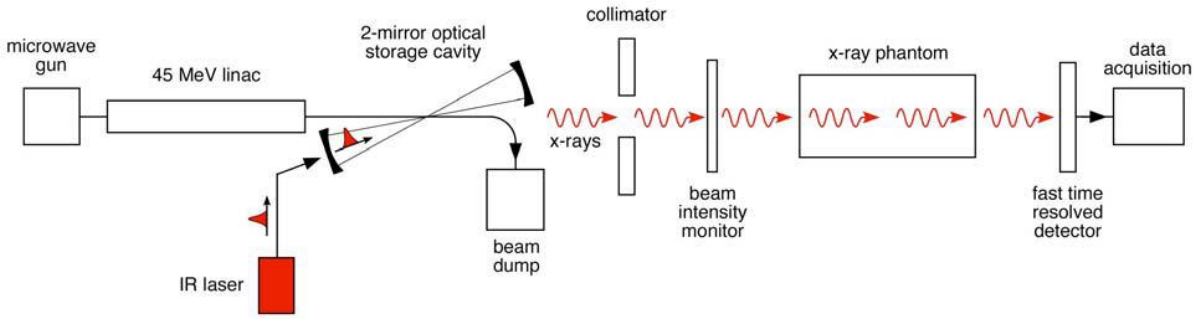


FIGURE 31. STURM2 hardware test set up.

10 Conclusions

This thesis reached all of its goals concerning the motherboard design, which was the main focus. Revision A of the motherboard was designed and manufactured, and is currently in a testing phase. In parallel to the motherboard design this thesis included amplifier board design and testing, component selection and purchasing and managing bill of materials of all the components in the design. The main focus in the component selection was to choose components that can be easily soldered since the first prototype will be assembled by hand. Components needed to have casing that is physically large enough, as well as enough lead spacing. The PADS design software can produce the BOM in Microsoft excel format with all the necessary components listed. Managing the BOM included finding suppliers that can provide all the components, eliminating the need for placing several orders.

The thesis also included a lot of circuit board assembly, and consulting with various companies concerning component purchase, circuit board manufacturing and assembly. Also in parallel with the motherboard design, a revision B of the ASIC board which fixed numerous issues in revision A was designed.

The firmware testing was not so successful for the reasons explained in Chapter 6. The time and effort that was put to the attempts to get the testing software working proved very frustrating for all the people involved.

Working in the instrumentation development laboratory is very self–reliant, and with so many different projects going on at the same time it takes some time to get fully adjusted working in a place like this. This kind of independent work method is very helpful in gaining more professional expertise. When assigned to a certain project and design, each person gets lots of responsibility and freedom to work on their design as they see fit. As long it follows the project rules and criteria of course. But during the first couple of weeks, a new worker finds himself in a maze of abbreviations and new devices. There really is no tutoring or introduction phase, and it is everybody’s own responsibility to catch up with the rest of the people.

11 Lessons learnt

Being able to do a thesis in an international work group, as well as to take part in a design processes as the STURM2 is a once in a lifetime opportunity. Skills in different languages as well as professional skills have massively improved during the exchange period. Skills learnt include mastering design, layout, printed circuit board manufacturing, board assembly, integrated module testing, parts procurement, PADS CAD tools, especially the auto router module, as well as understanding how to select parts and optimize component selection.

The experience from long term projects is also extremely valuable for the future career. The experiences vary from those that make project handling easier and more effective to those work methods that should never be used. Weekly meetings and coordinating of the ongoing project with other people involved via video conferences, as well as weekly deadlines and common design criteria are those methods that proved very effective.

On the other hand, many points of improvement were found. It is vital that in one project all the people involved use the same or at least a compatible design environment. As explained in Chapter 6, when one person decides to do things in his own way instead of keeping into the criteria that are outlined in the project start, the entire organization can come to a stop. In the worst case, this kind of work needs to be redone by someone else, causing a lot of lost time and money.

12 Further development

Further development of the monitoring system will be a 128-channel device, which will double the amount of measurement channels. The focus on the next generation measuring device will be to achieve faster measurement with more samples from each electron bunch, along with faster and more accurate AD conversion.

The device created in this thesis will serve as a part of Super KEKB collider and BELLE2 experiment, and also a design and research platform for next generation devices. The desired monitoring accuracy and speed along with other design criteria will be decided based on the experience and performance of the 64-channel device. The progress of the STURM2 project can be followed from STURM-based x-ray monitor meeting page from address http://www.phys.hawaii.edu/~idlab/

13 Symbols, terms and abbreviations

STURM2	Sampler of Transients for the Uniformly Redundant Mask
BELLE2	General purpose spectrometer for the next-generation *B*-factory experiment at KEK. The Belle2 efficiently collects data of e^+-e^- collisions made by the Super KEKB accelerator
Mils	A unit of measurement used in electronics. One mill equals one thousands of an inch.
PADS	PCB design software created by Mentor Graphics.
SCROD	FPGA firmware + PC software to control and readout waveform sampling ASICs for instrumenting sub detectors in high-energy physics experiments. Designed in instrumentation development laboratory at university of Hawaii.

References

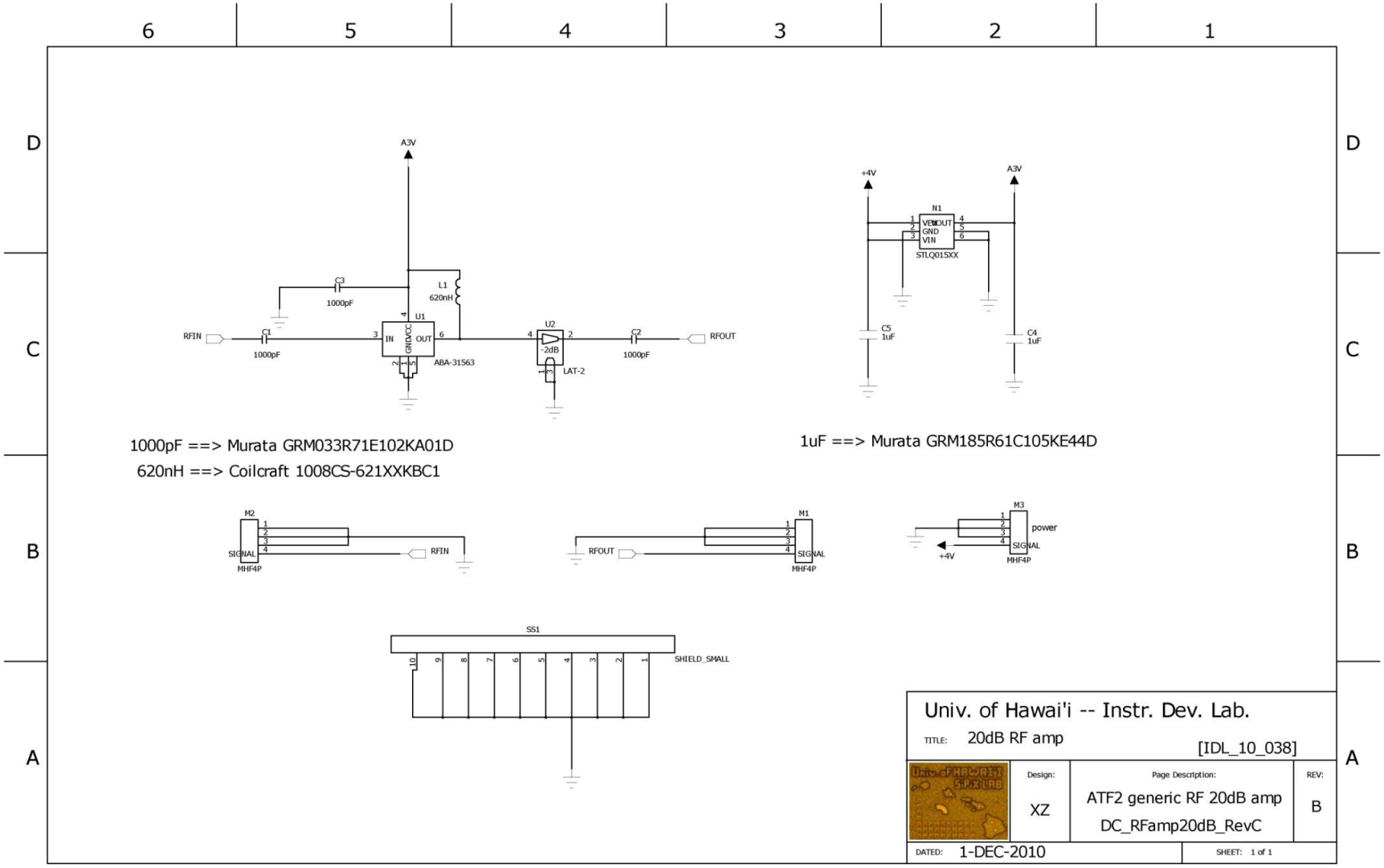
BELLE2 collaboration. [Web Page] accessed January 2012. http://belle2.kek.jp/detector.html

STURM2 design review, Dr. Gary S. Varner 2009. [Web Page] accessed January 2012. http://www.phys.hawaii.edu/~idlab/

High Energy Accelerator Research Organization, (KEK). [Web Page] accessed January 2012. http://accl.kek.jp/eng/acclmap_e.html

PADS PCB Design Tools. [Web Page] accessed January 2012. http://www.mentor.com/products/pcb-system-design/design-flows/pads/

STURM-based x-ray Monitor Meeting page. [Web Page] accessed January 2012. http://www.phys.hawaii.edu/~idlab/


6
5
4
3
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A3V
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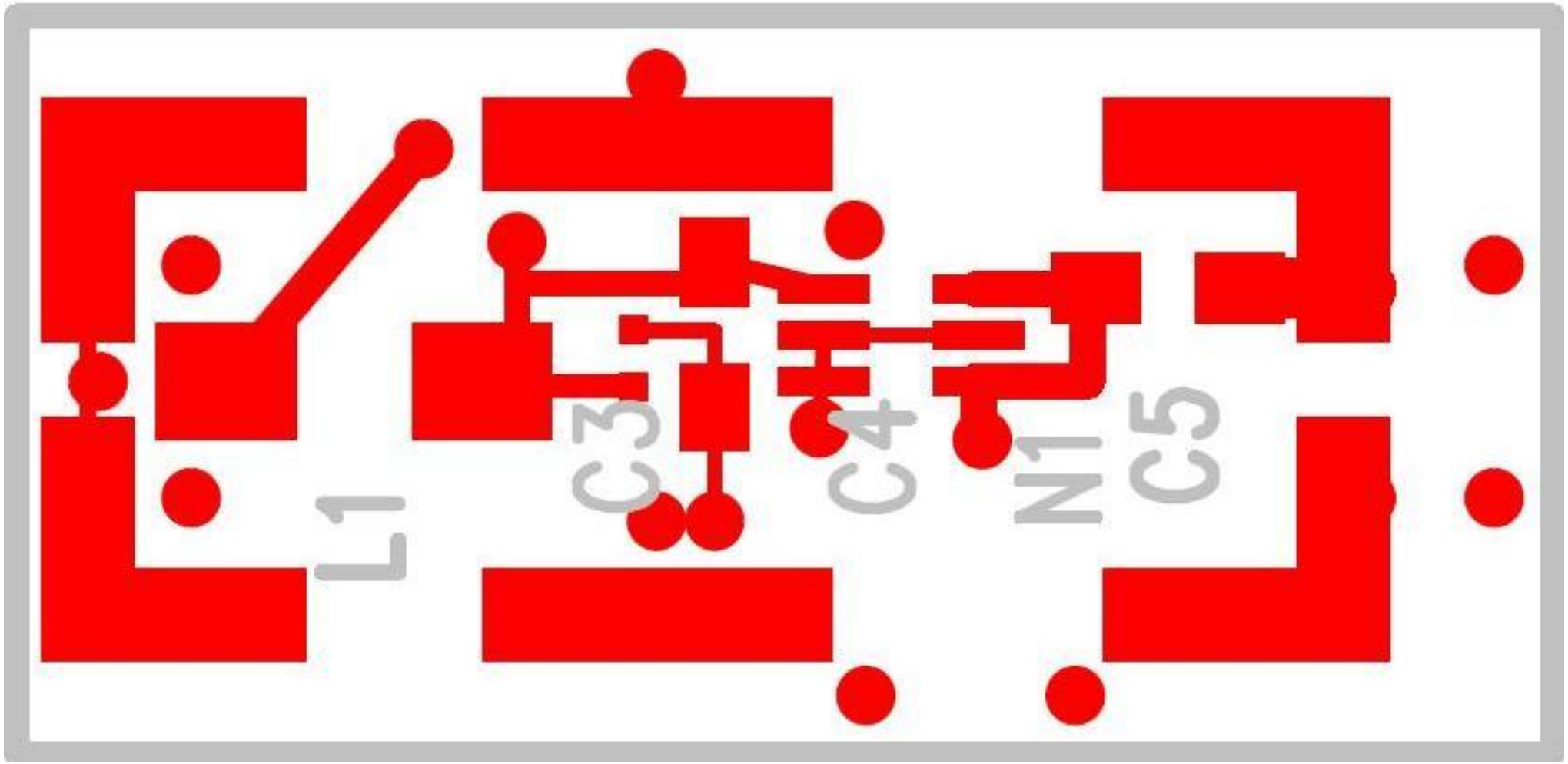
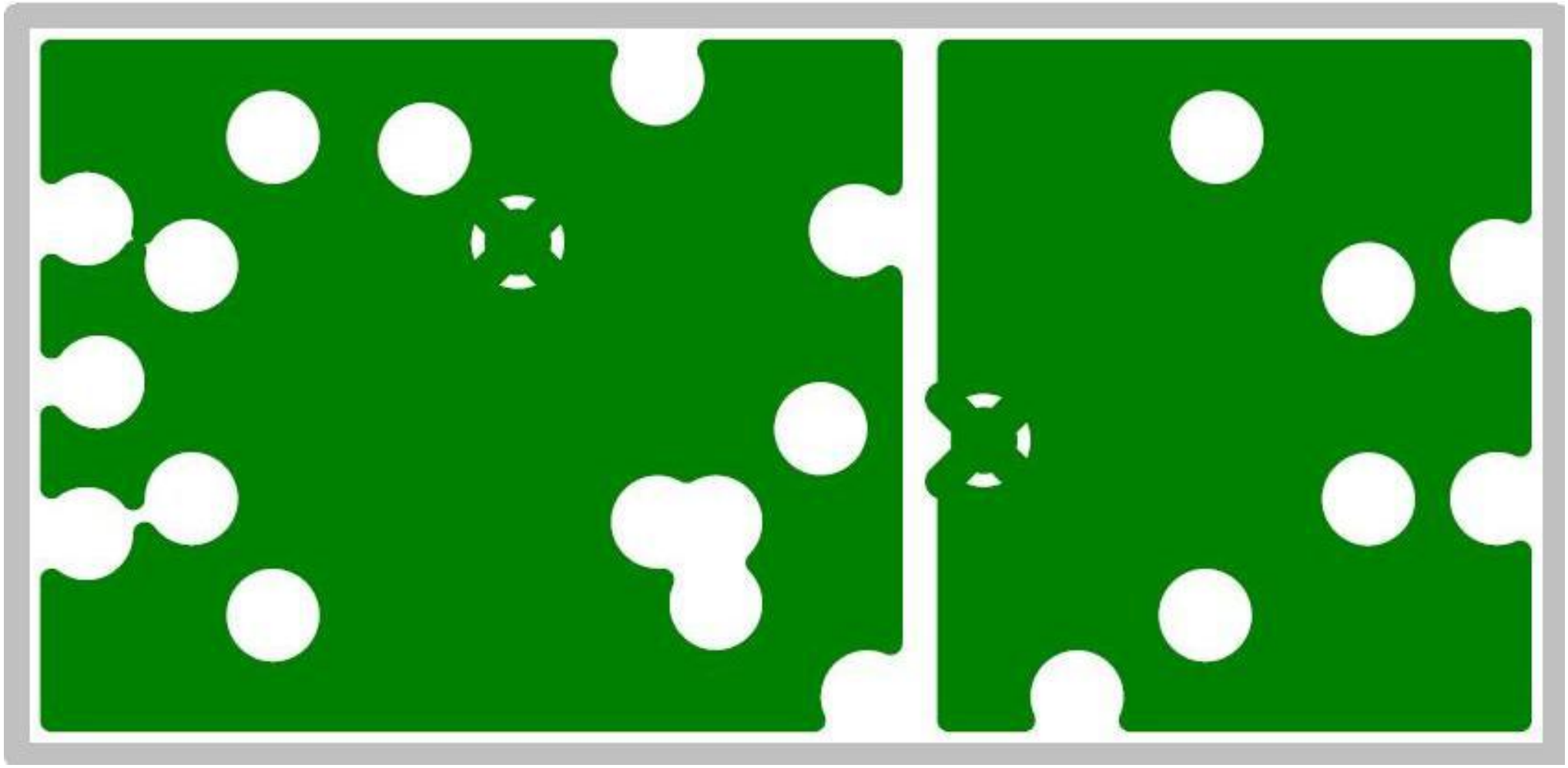
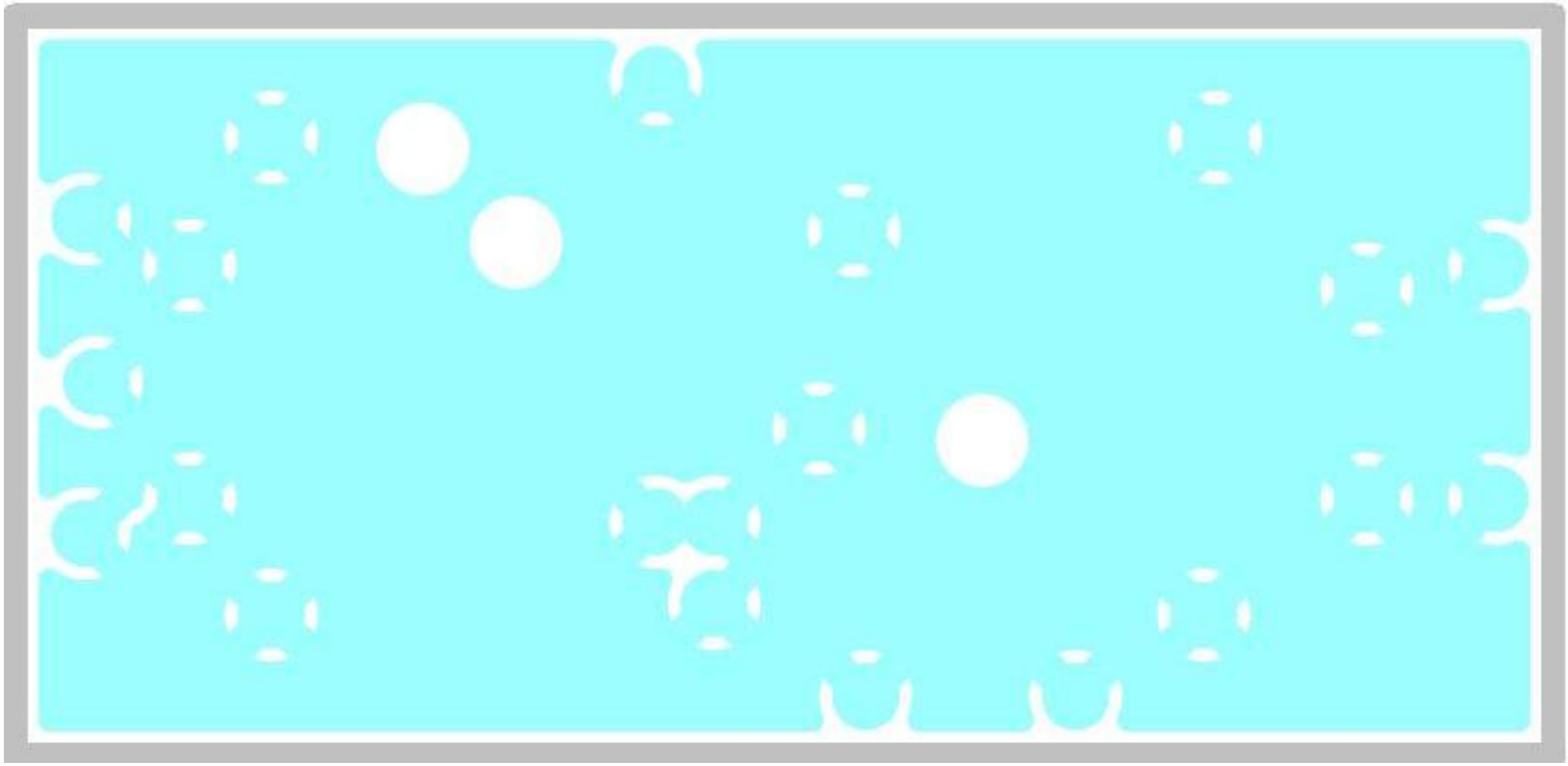
1000pF
L1
620nH
RFIN
C1
1000pF
U1
IN
GND
VCC
OUT
ABA-31563
U2
-2dB
LAT-2
C2
1000pF
RFOUT
+4V
A3V
N1
VEN
GND
VIN
VOUT
STLQ015XX
C5
1uF
C4
1uF
1000pF ==> Murata GRM033R71E102KA01D
620nH ==> Coilcraft 1008CS-621XXKBC1
1uF ==> Murata GRM185R61C105KE44D
M2
SIGNAL
RFIN
MHF4P
M1
RFOUT
SIGNAL
MHF4P
M3
power
SIGNAL
+4V
MHF4P
SS1
SHIELD_SMALL
Univ. of Hawai'i -- Instr. Dev. Lab.
TITLE: 20dB RF amp
[IDL_10_038]
Design:
XZ
Page Description:
ATF2 generic RF 20dB amp
DC_RFamp20dB_RevC
REV:
B
DATED: 1-DEC-2010
SHEET: 1 of 1



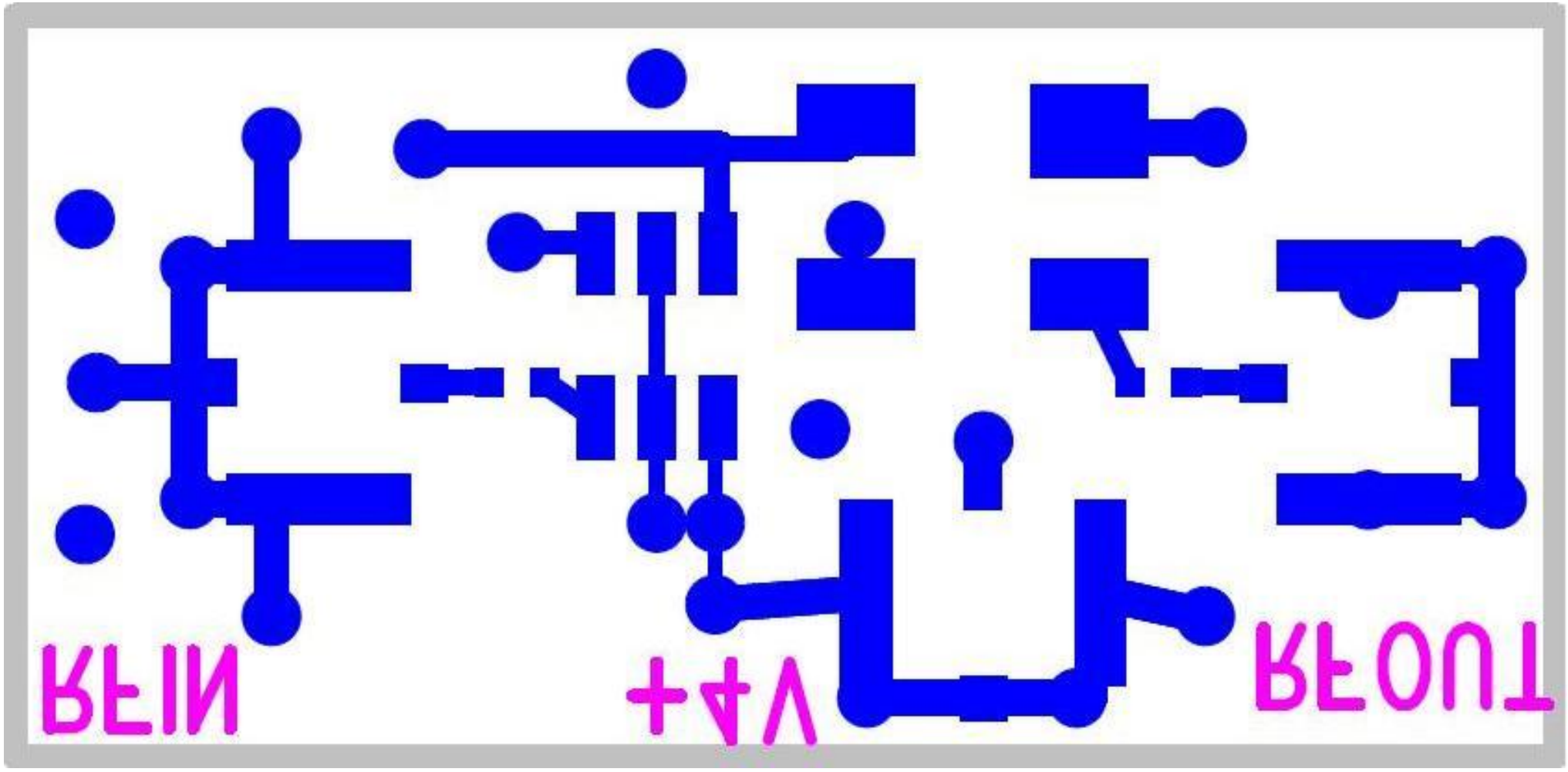
STURM2 amplifier board top layer, primary components



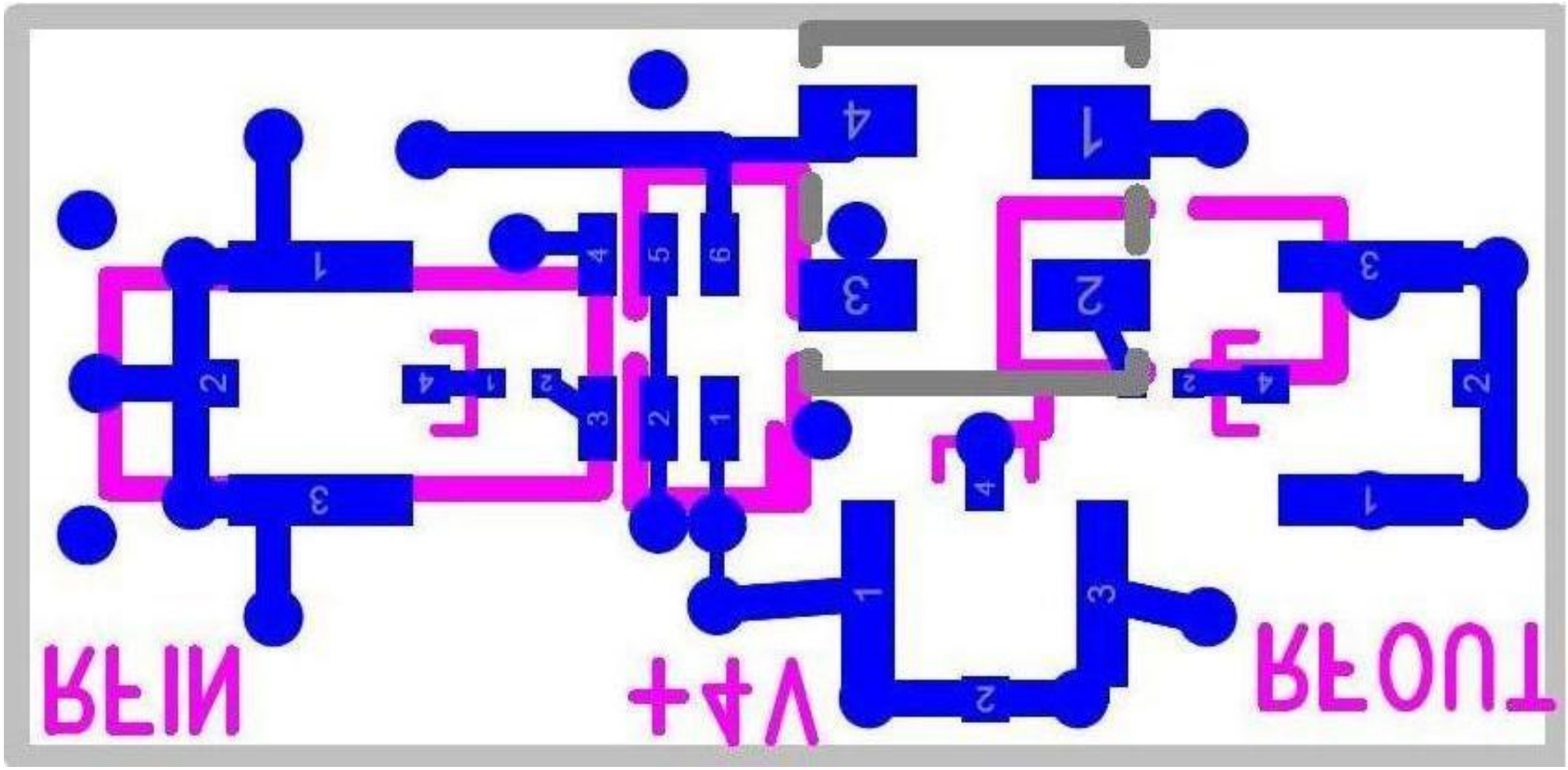
STURM2 amplifier board inner layer 1, power



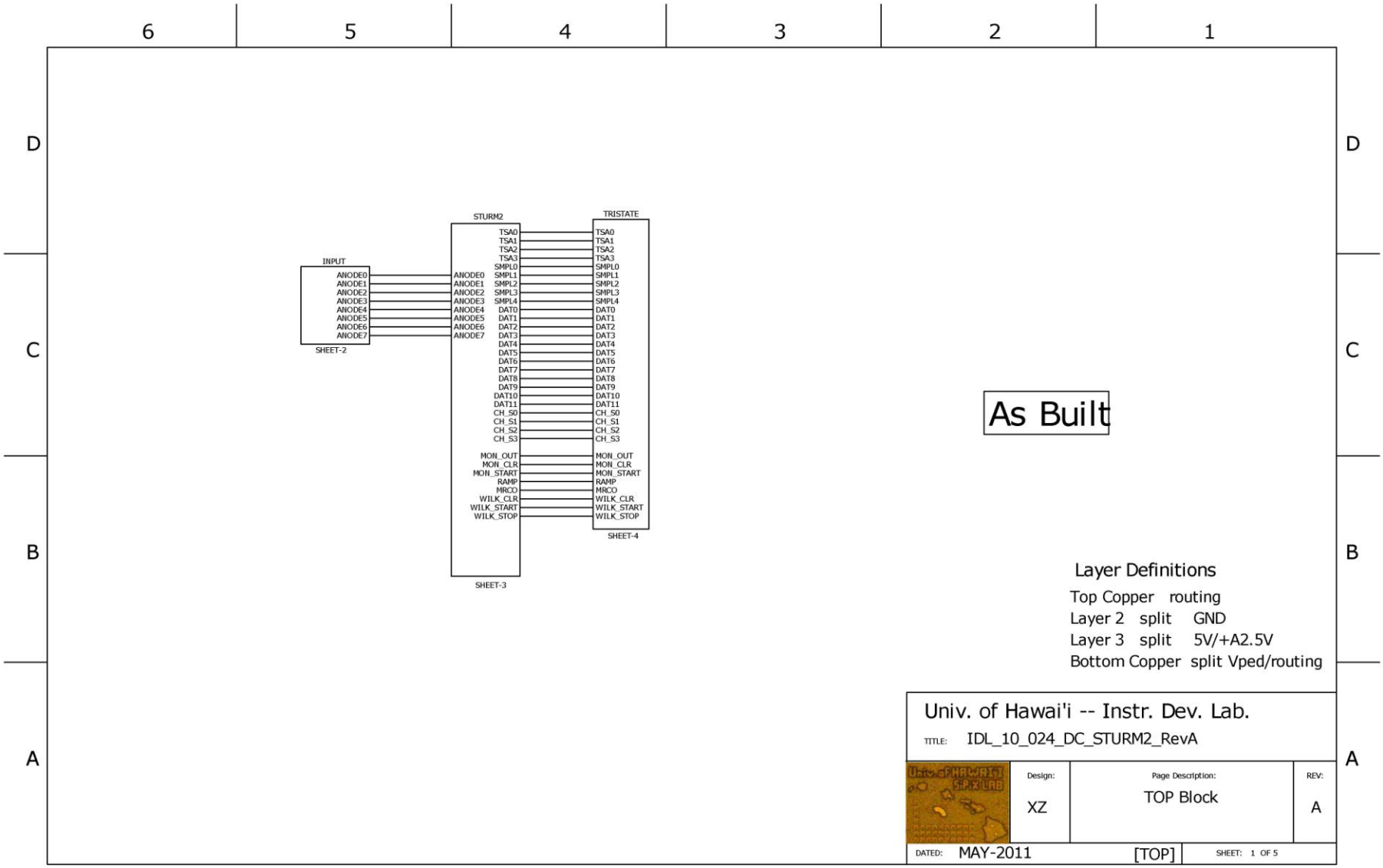
STURM2 amplifier board inner layer 2, GND

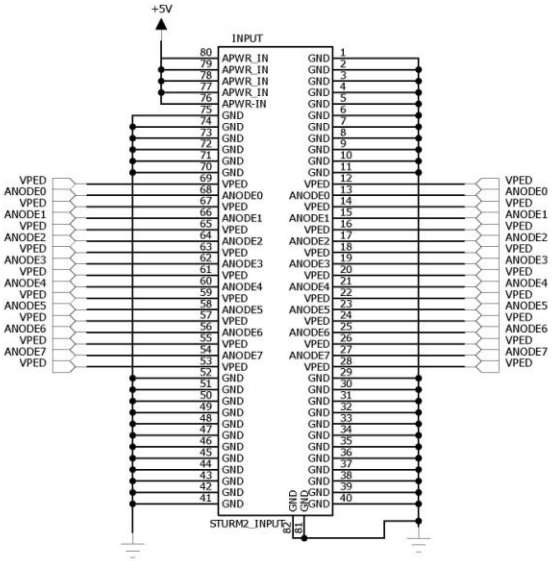


STURM2 amplifier board bottom layer, RF components



STURM2 amplifier board composite


6
5
4
3
2
1
D
C
B
A
INPUT
ANODE0
ANODE1
ANODE2
ANODE3
ANODE4
ANODE5
ANODE6
ANODE7
SHEET-2
STURM2
ANODE0
ANODE1
ANODE2
ANODE3
ANODE4
ANODE5
ANODE6
ANODE7
TSA0
TSA1
TSA2
TSA3
SMPL0
SMPL1
SMPL2
SMPL3
SMPL4
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
DAT8
DAT9
DAT10
DAT11
CH_S0
CH_S1
CH_S2
CH_S3
MON_OUT
MON_CLR
MON_START
RAMP
MRCO
WILK_CLR
WILK_START
WILK_STOP
SHEET-3
TRISTATE
TSA0
TSA1
TSA2
TSA3
SMPL0
SMPL1
SMPL2
SMPL3
SMPL4
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
DAT8
DAT9
DAT10
DAT11
CH_S0
CH_S1
CH_S2
CH_S3
MON_OUT
MON_CLR
MON_START
RAMP
MRCO
WILK_CLR
WILK_START
WILK_STOP
SHEET-4
As Built
Layer Definitions
Top Copper routing
Layer 2 split GND
Layer 3 split 5V/+A2.5V
Bottom Copper split Vped/routing
Univ. of Hawai'i -- Instr. Dev. Lab.
TITLE: IDL_10_024_DC_STURM2_RevA
Design:
XZ
Page Description:
TOP Block
REV:
A
DATED: MAY-2011
[TOP]
SHEET: 1 OF 5



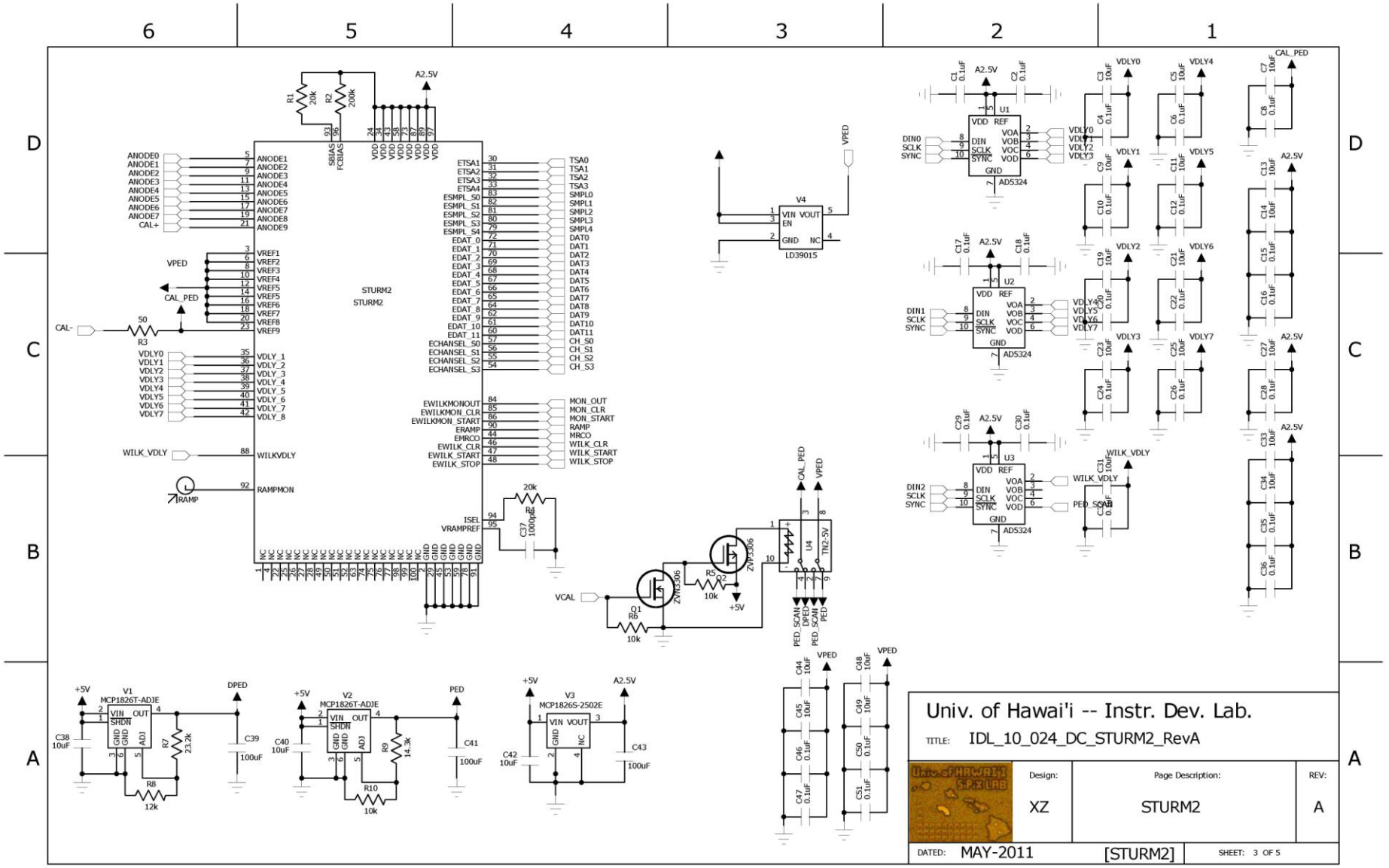
DAT7

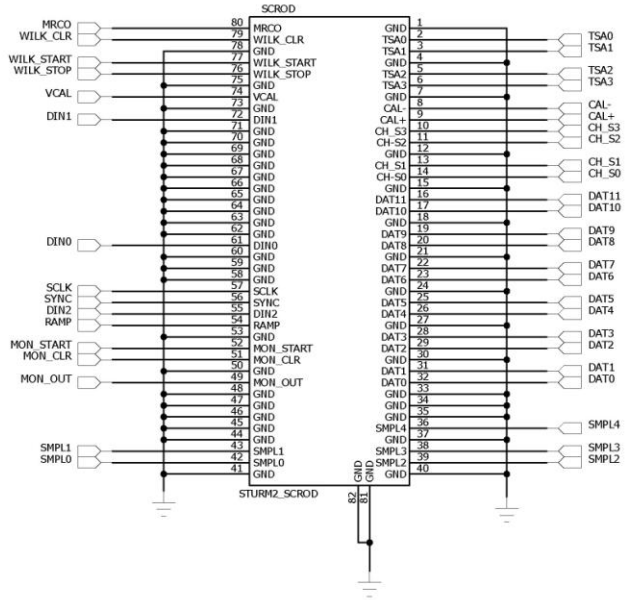
Univ. of Hawai'i -- Instr. Dev. Lab.

TITLE: IDL_10_024_DC_STURM2_RevA

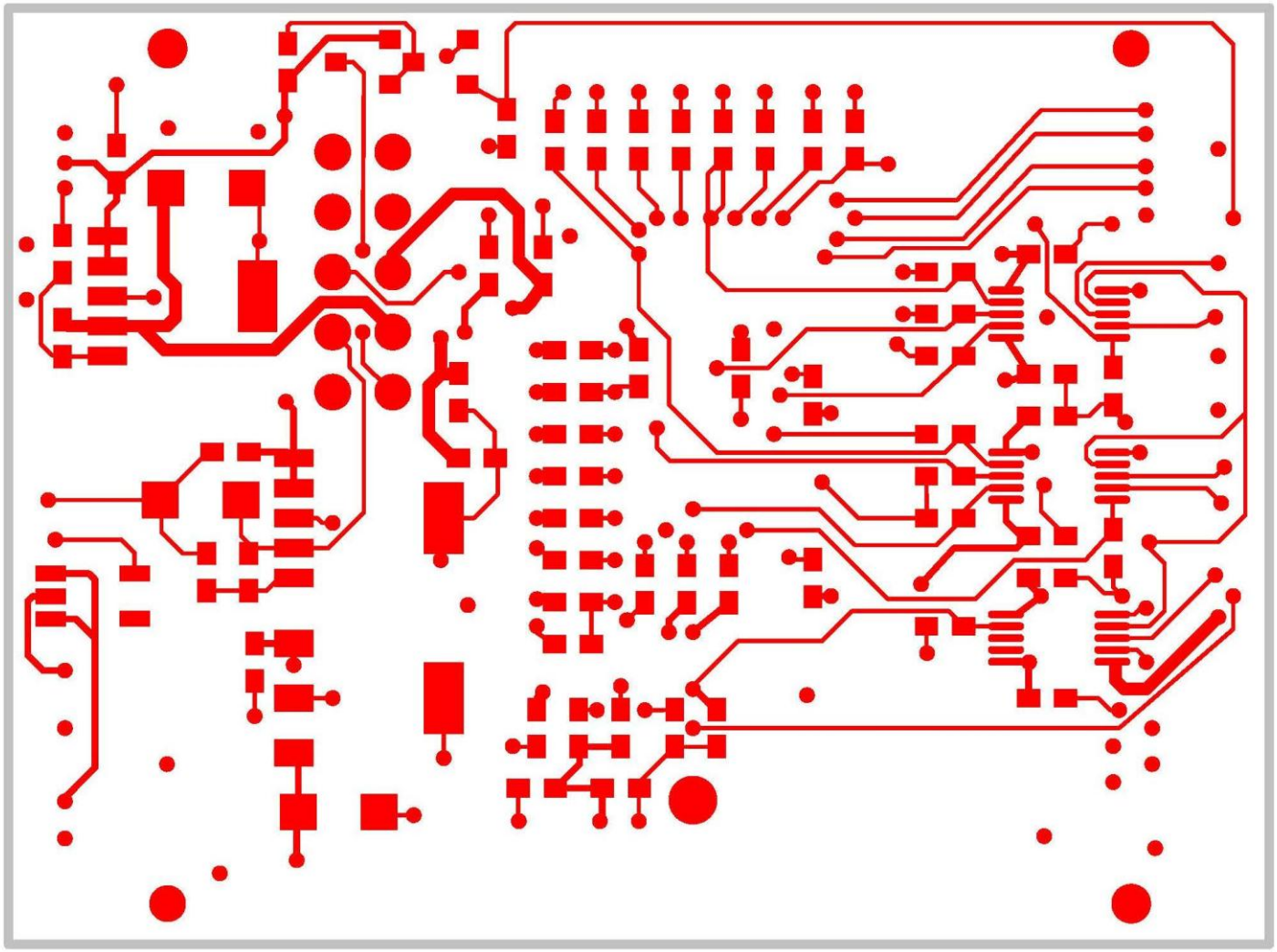
Design:	Page Description:	REV:
XZ	Input Block	A

DATED: MAY2011 [INPUT] SHEET: 2 OF 5

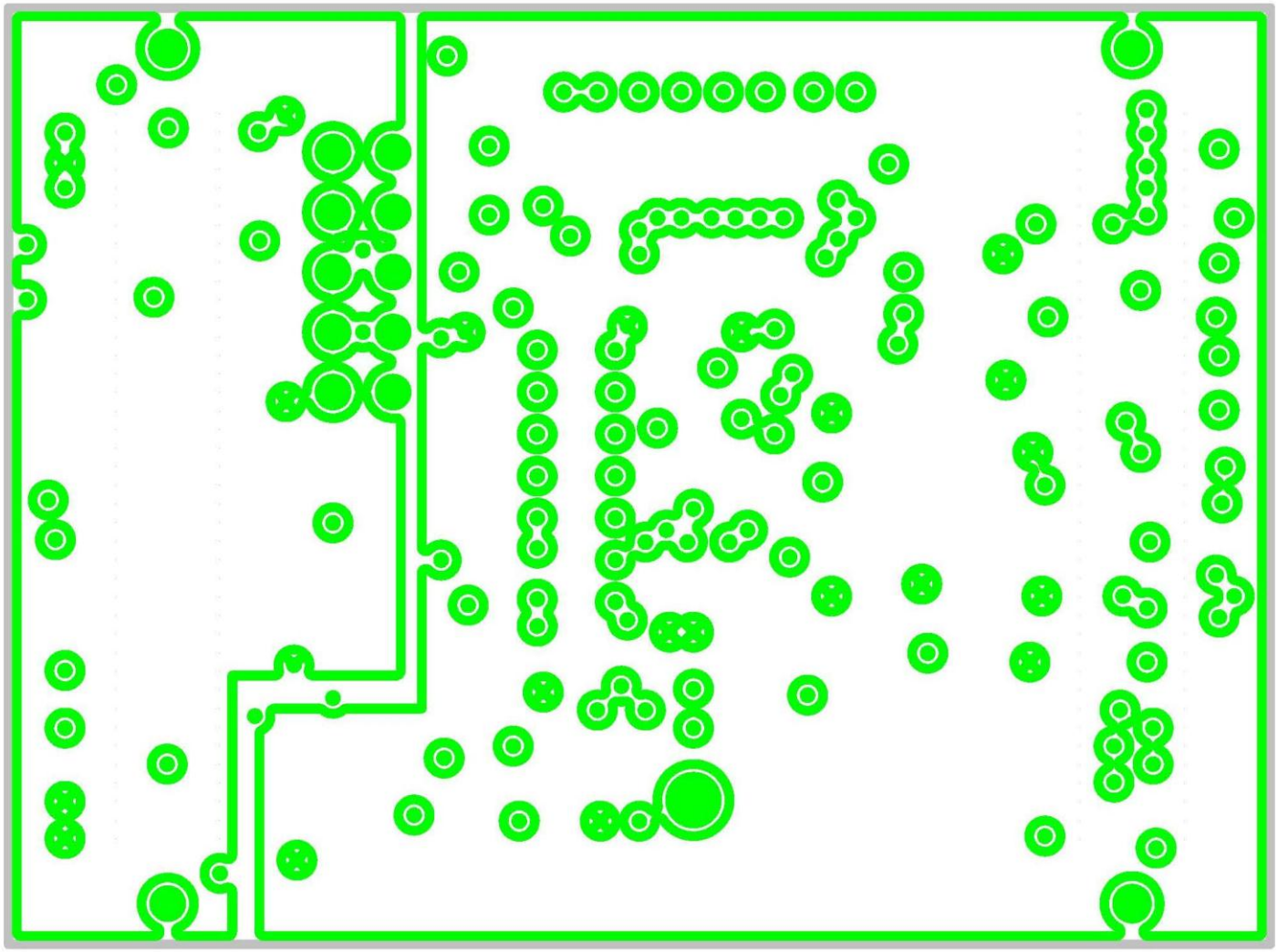

STURM2
STURM2
A2.5V
VPED
CAL_PED
CAL-
WILK_VDLY
RAMP
VCAL
+5V
DPED
PED
Univ. of Hawai'i -- Instr. Dev. Lab.
TITLE: IDL_10_024_DC_STURM2_RevA
Design: XZ
Page Description: STURM2
REV: A
DATED: MAY-2011
[STURM2]
SHEET: 3 OF 5



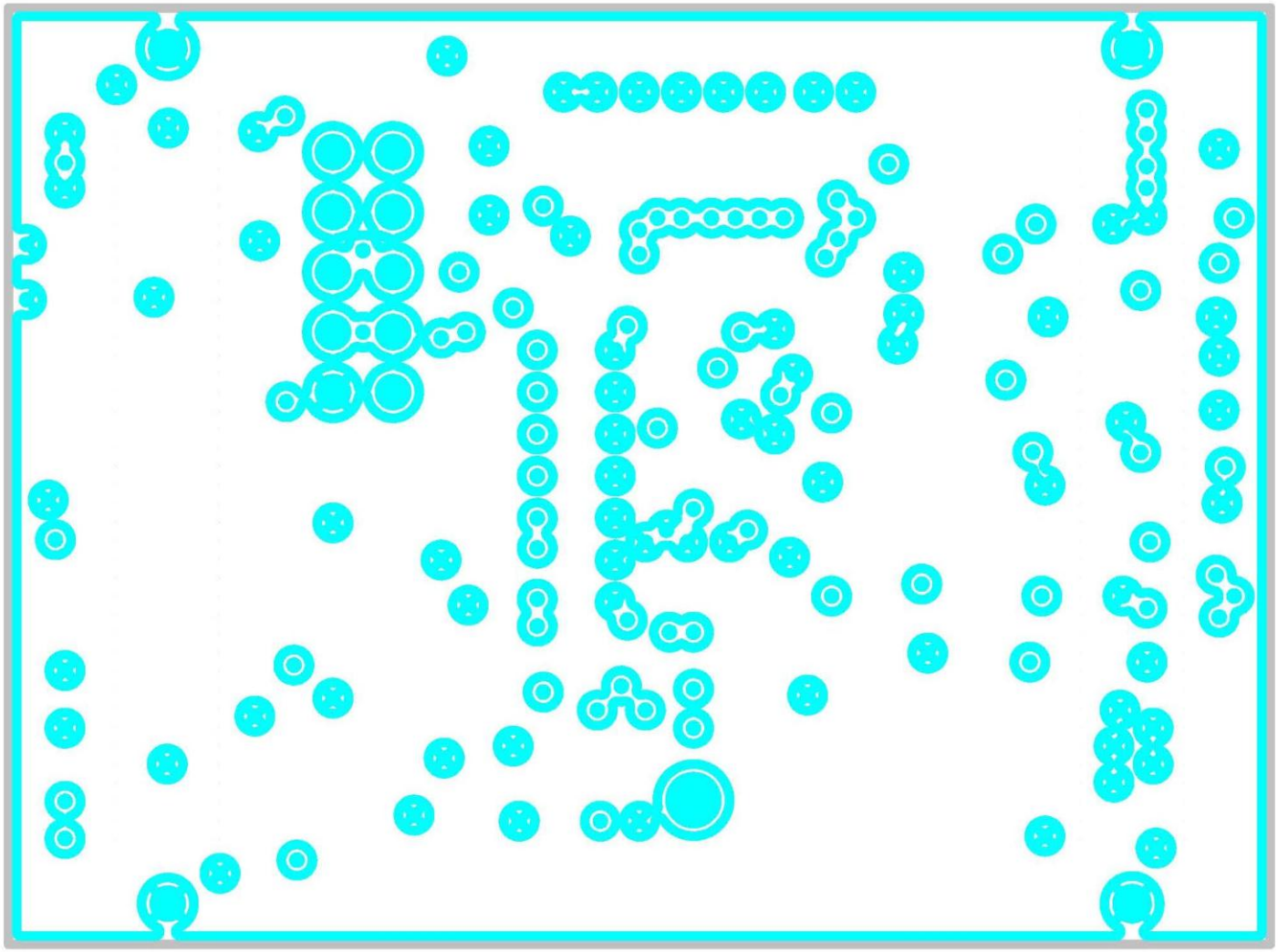
Univ. of Hawai'i -- Instr. Dev. Lab.			
TITLE: IDL_10_024_DC_STURM2_RevA			
	Design: XZ	Page Description: Tristate Output Data Select	REV: A
DATED: MAY-2011	[TRISTATE]	SHEET: 5 OF 5	



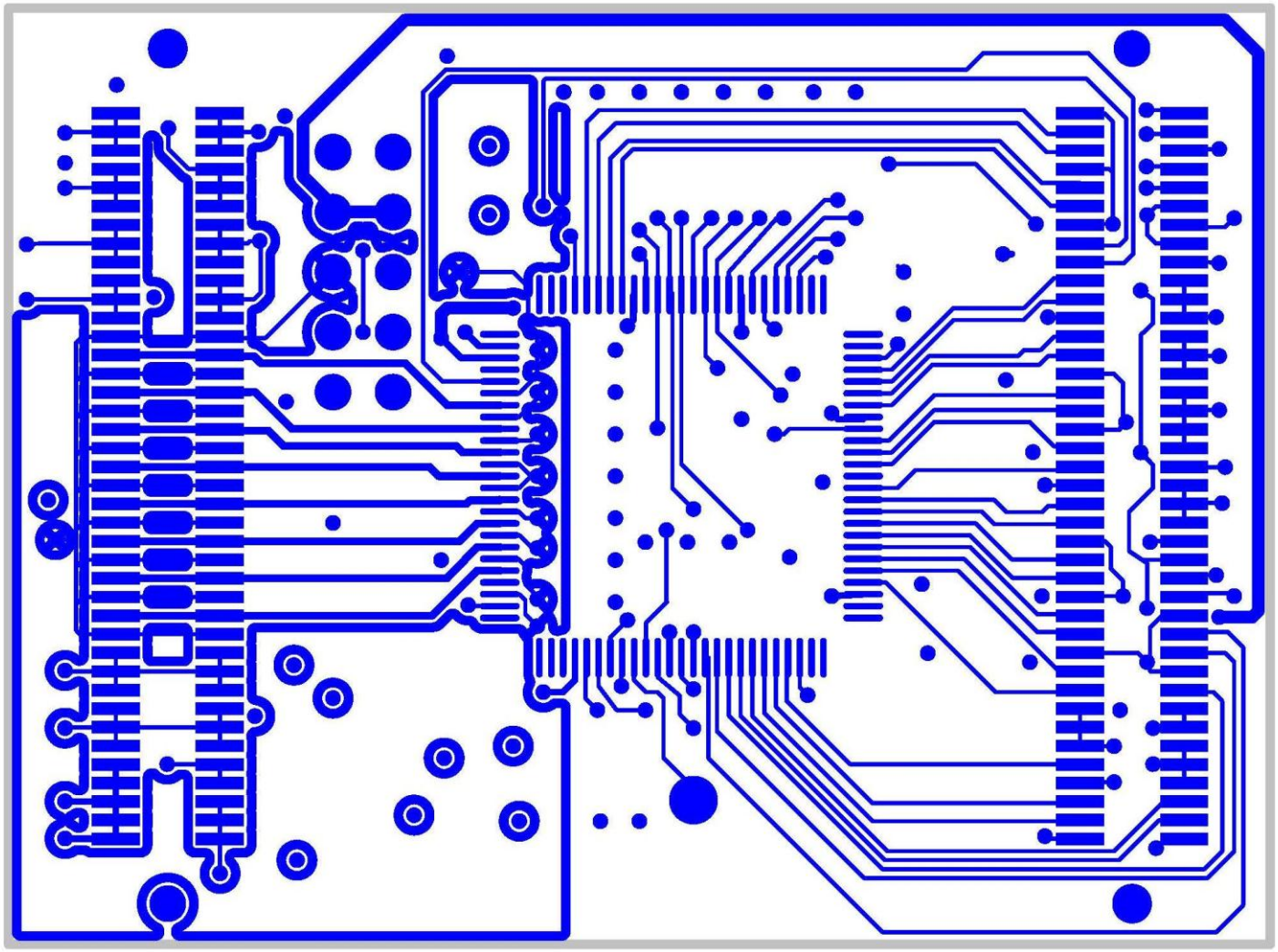
STURM2 ASIC board top layer



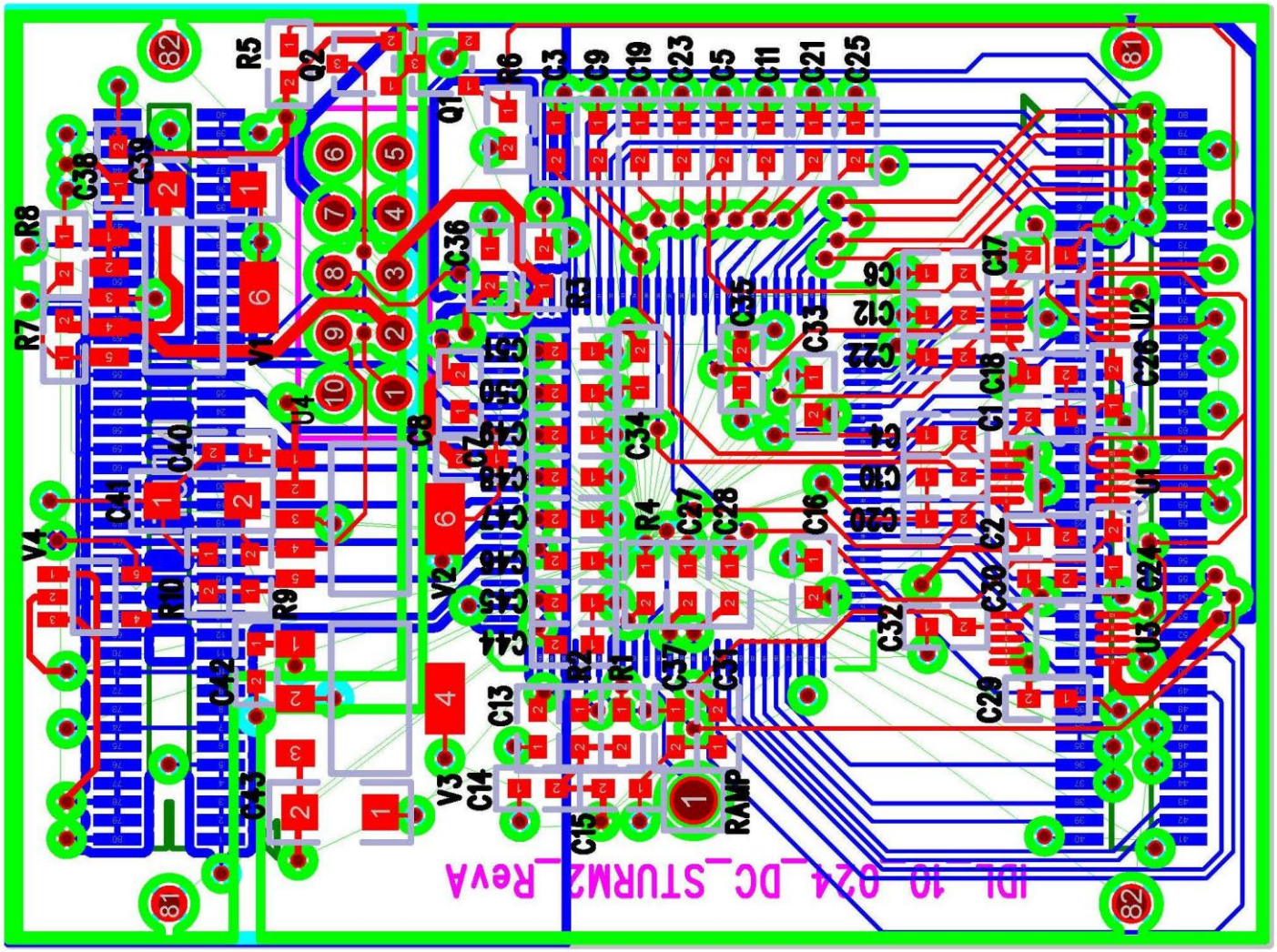
STURM2 ASIC board inner layer 1, power



STURM2 ASIC board inner layer 2, GND



STURM2 ASIC board bottom layer



STURM2 ASIC board composite

STURM2 Motherboard

Layer Definitions

Top Layer no plane routing / components

Layer 2 mixed plane split VPED / downbonds / routing

Layer 3 mixed plane amplifier regulator power

Layer 4 mixed plane amplifier power / routing

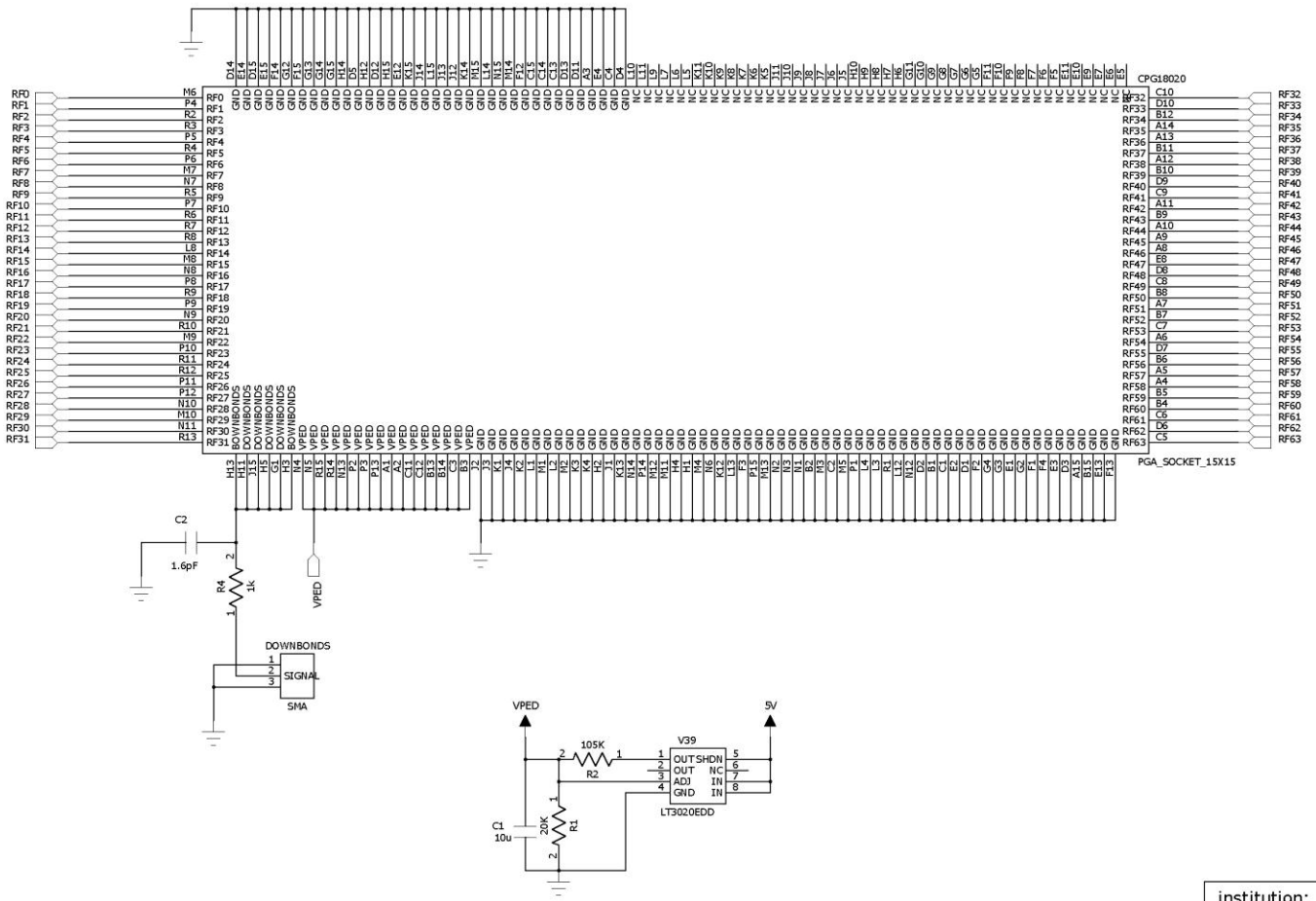
Layer 5 mixed plane ground plane 1 / routing

Layer 6 mixed plane common 5 volt power

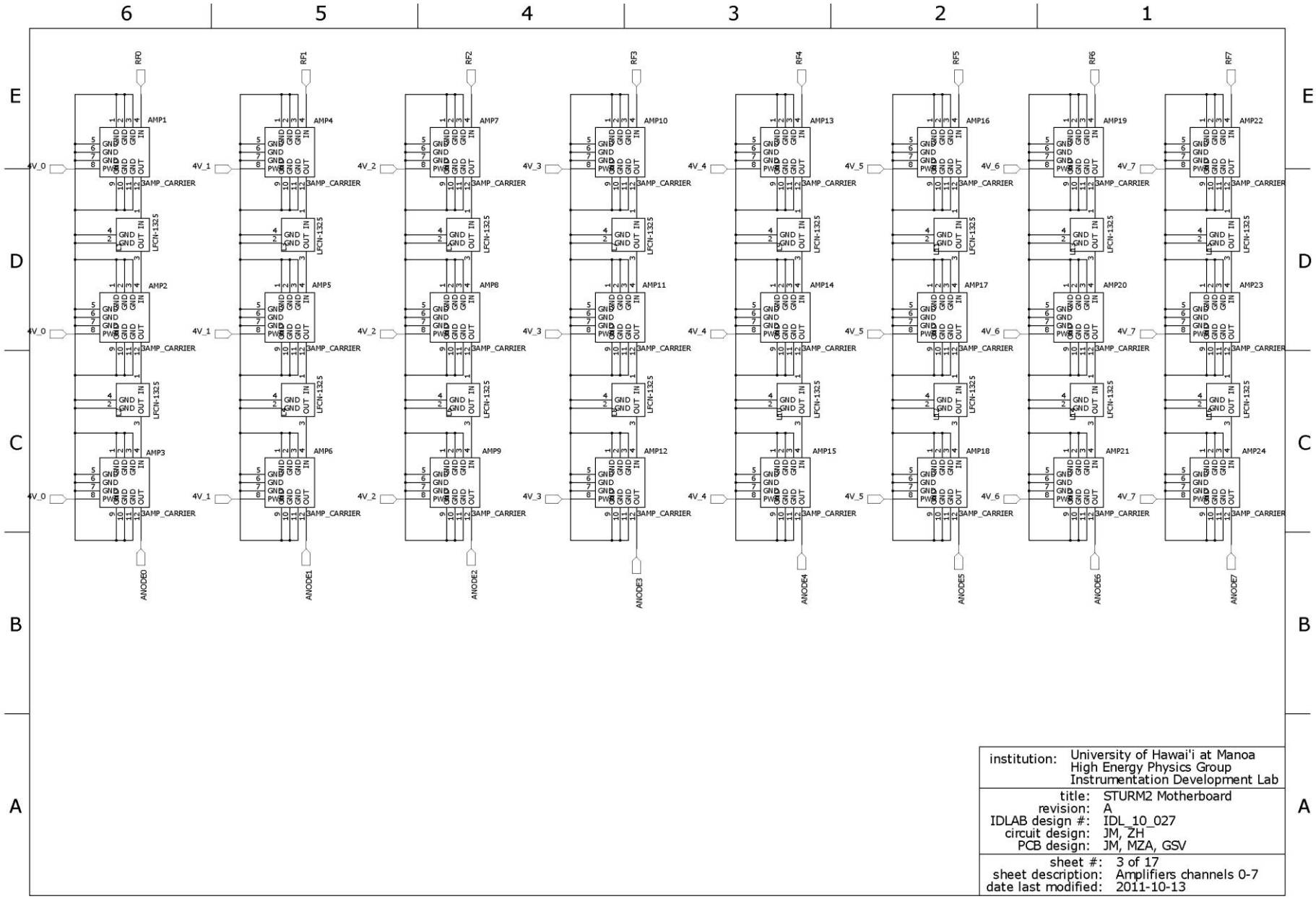
Layer 7 mixed plane ground plane 2

Bottom Layer no plane routing / components

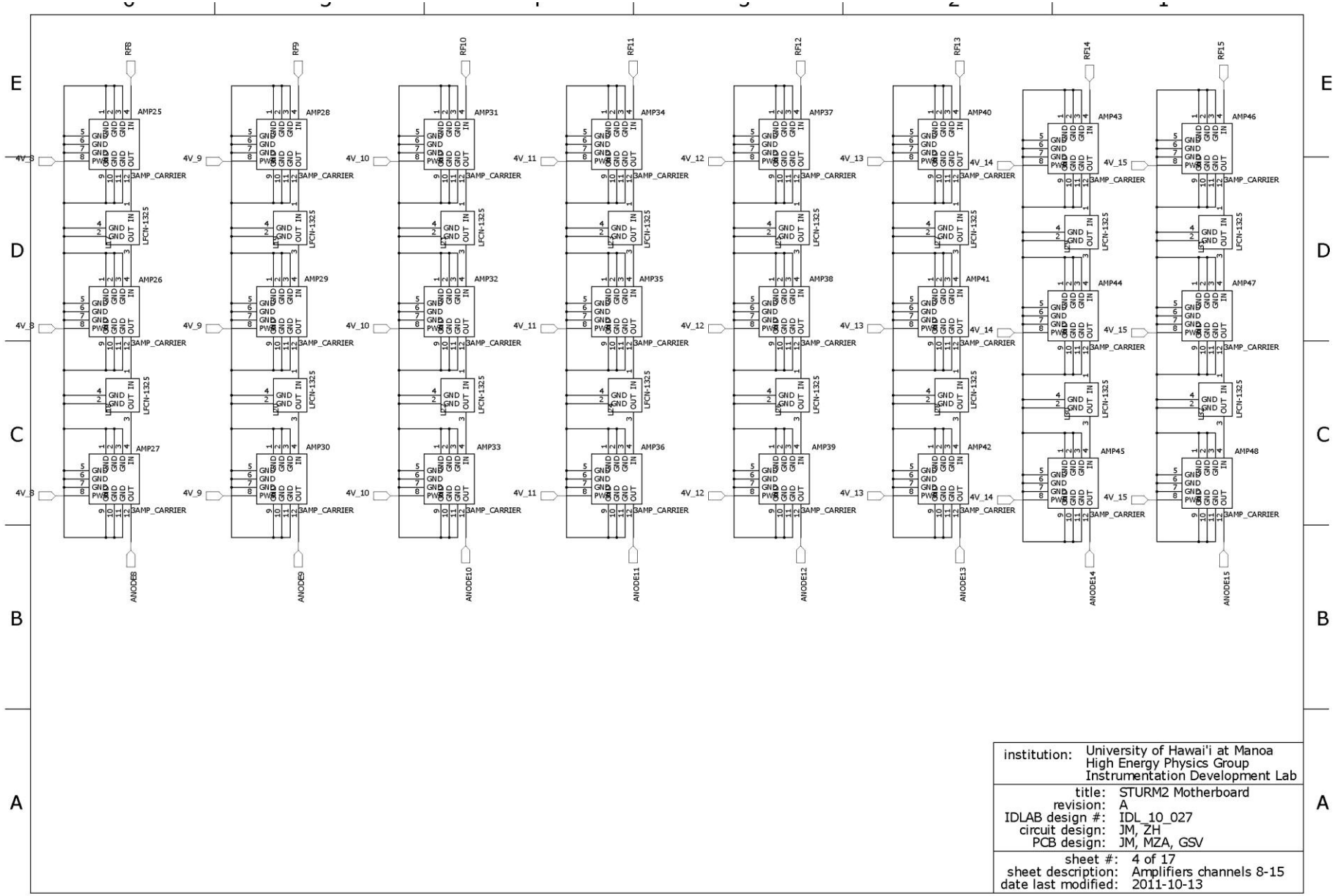
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	1 of 17
sheet description:	TOP Block
date last modified:	2011-10-13



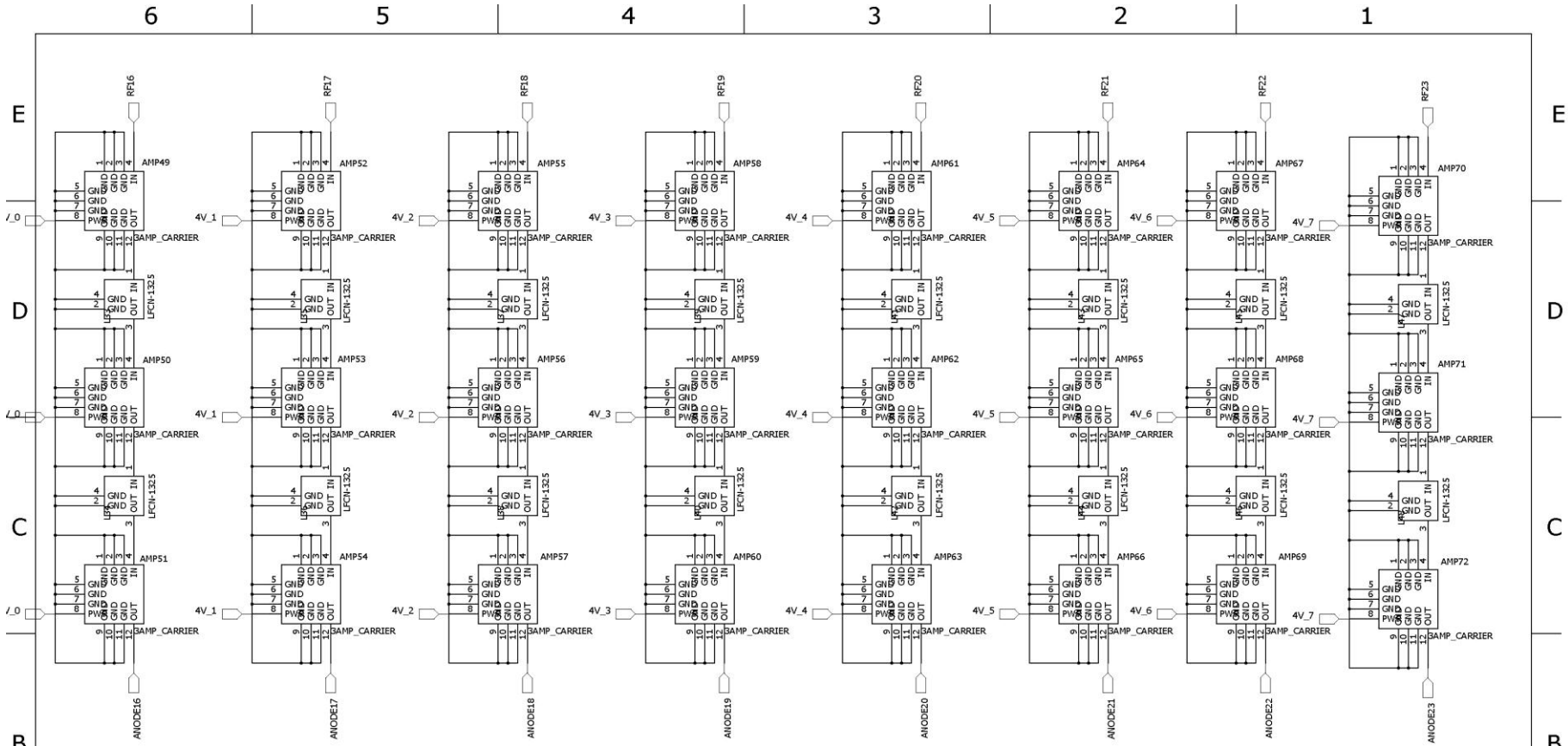
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	2 of 17
sheet description:	Fermionics sensor
date last modified:	2011-10-13



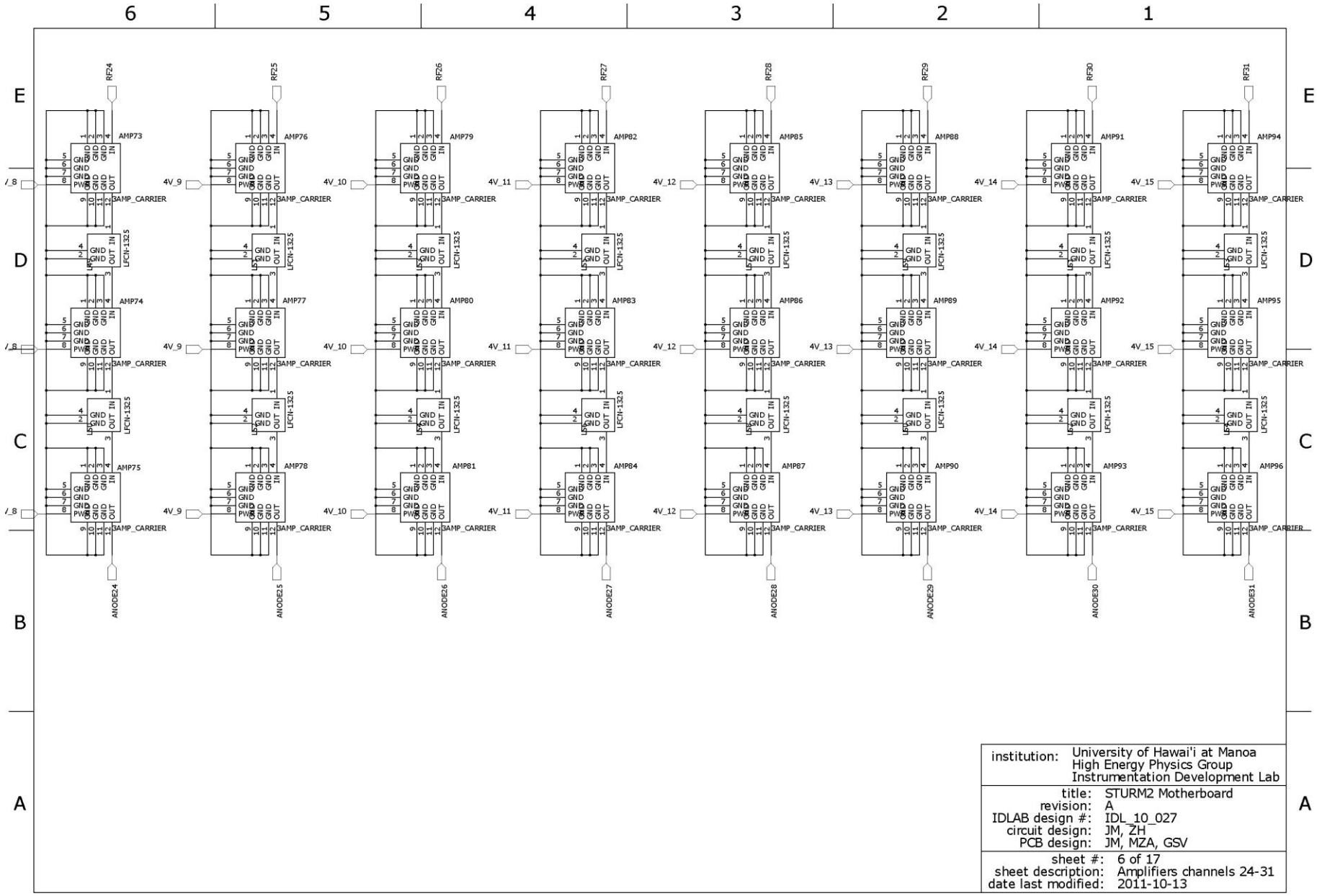
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	3 of 17
sheet description:	Amplifiers channels 0-7
date last modified:	2011-10-13



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	4 of 17
sheet description:	Amplifiers channels 8-15
date last modified:	2011-10-13



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	5 of 17
sheet description:	Amplifiers channels 16-23
date last modified:	2011-10-13


6
5
4
3
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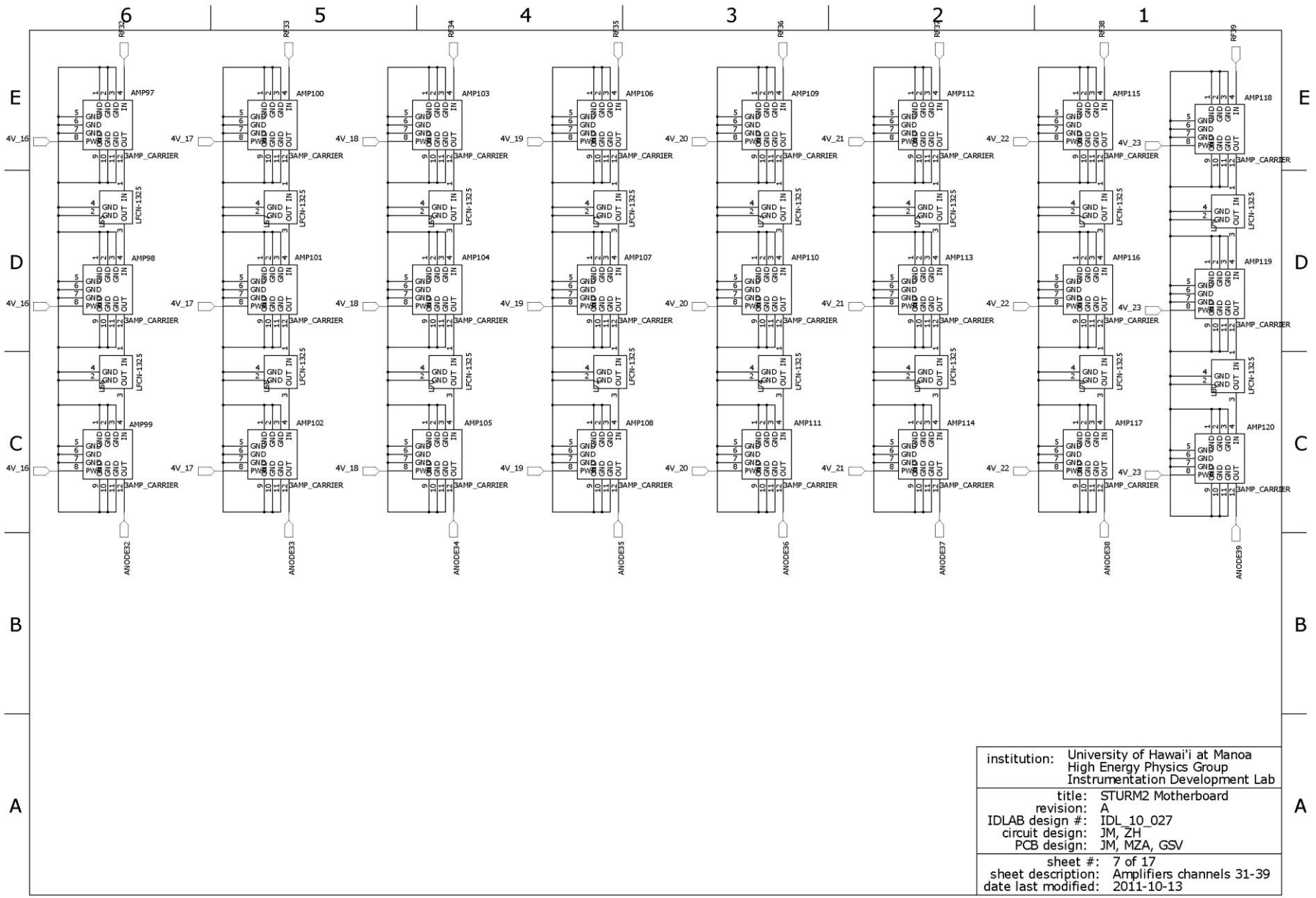
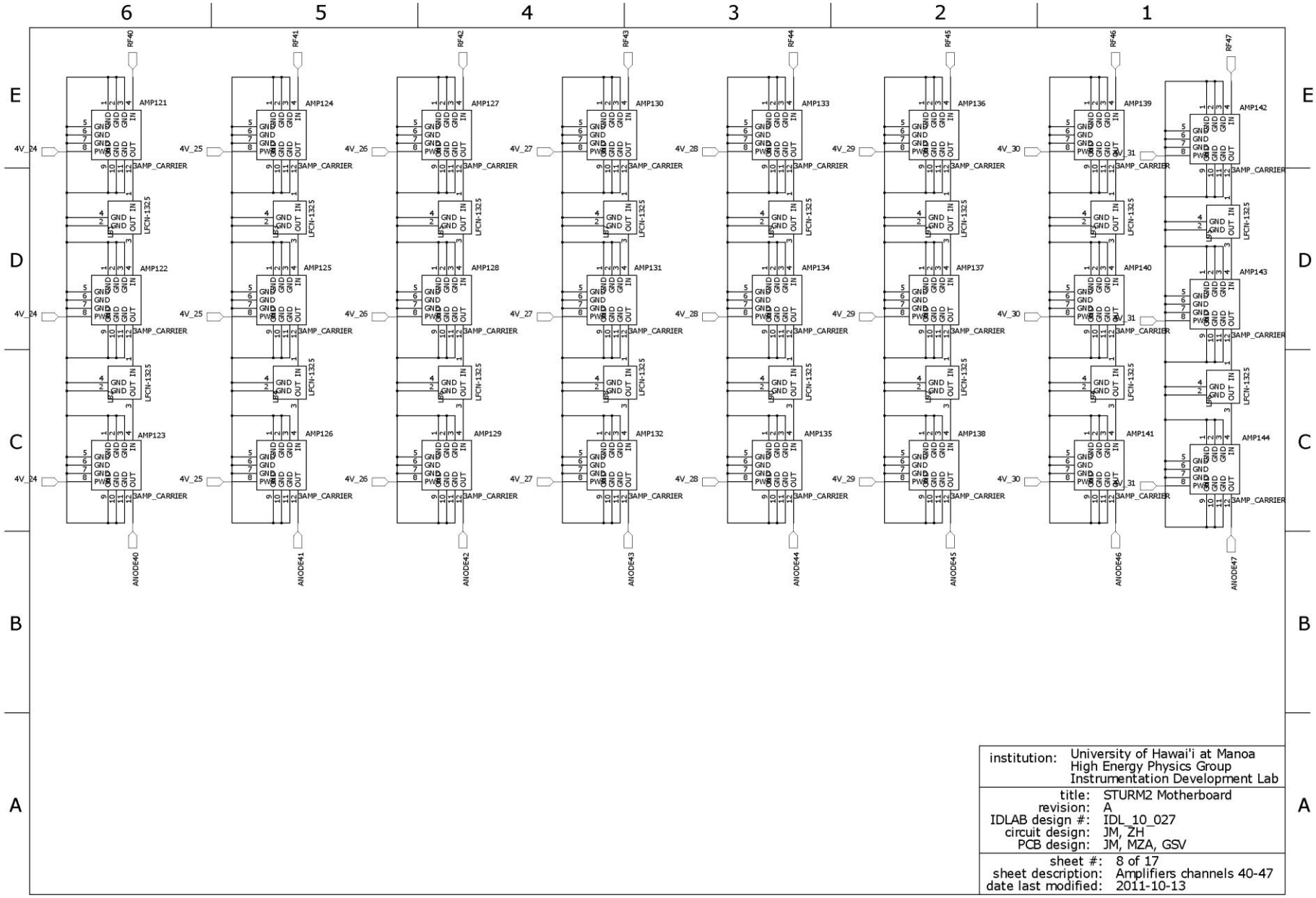
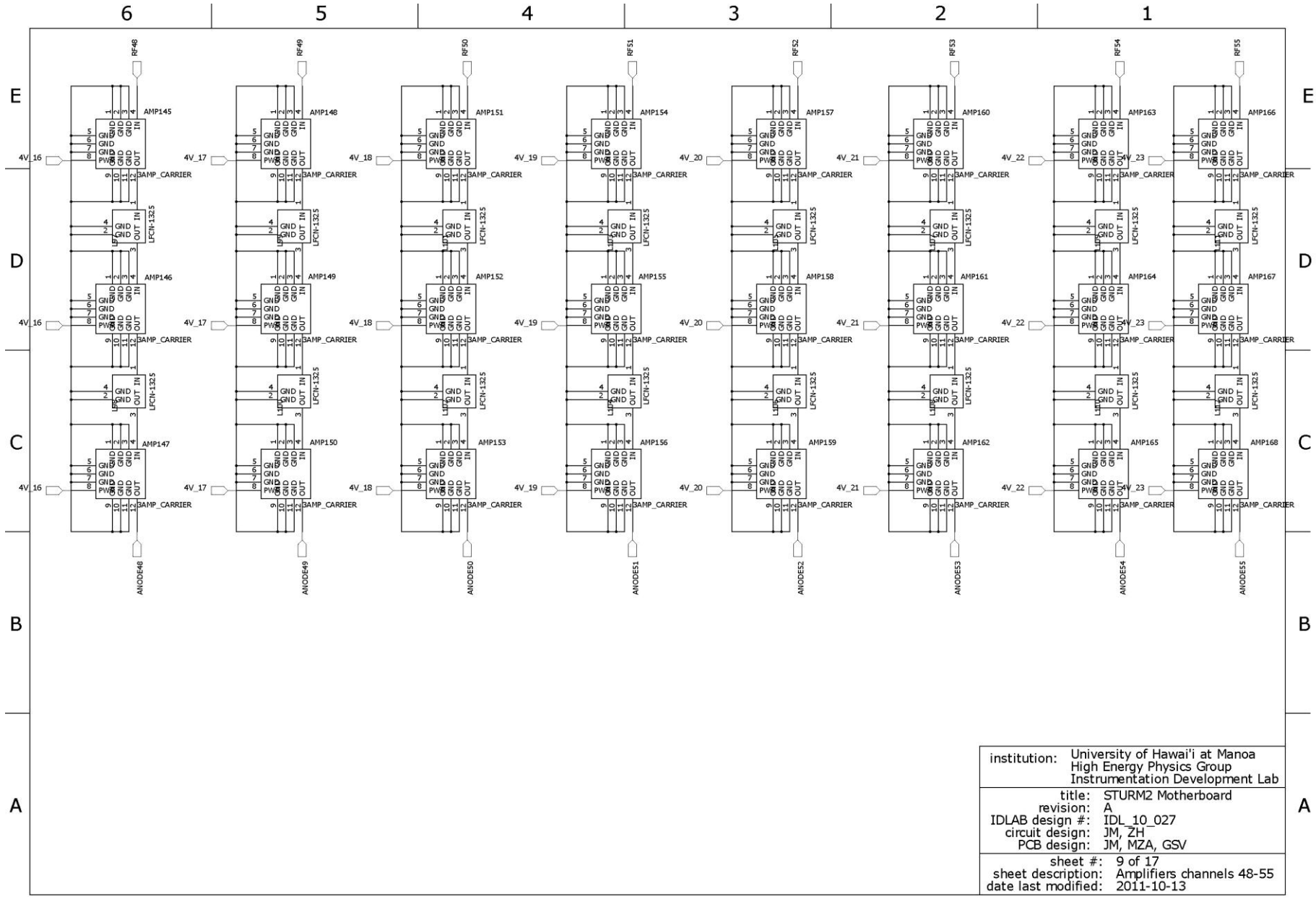
RF24
RF25
RF26
RF27
RF28
RF29
RF30
RF31
AMP73
AMP74
AMP75
AMP76
AMP77
AMP78
AMP79
AMP80
AMP81
AMP82
AMP83
AMP84
AMP85
AMP86
AMP87
AMP88
AMP89
AMP90
AMP91
AMP92
AMP93
AMP94
AMP95
AMP96
3AMP_CARRIER
LFCN-1325
4V_9
4V_10
4V_11
4V_12
4V_13
4V_14
4V_15
ANODE24
ANODE25
ANODE26
ANODE27
ANODE28
ANODE29
ANODE30
ANODE31
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 6 of 17
sheet description: Amplifiers channels 24-31
date last modified: 2011-10-13



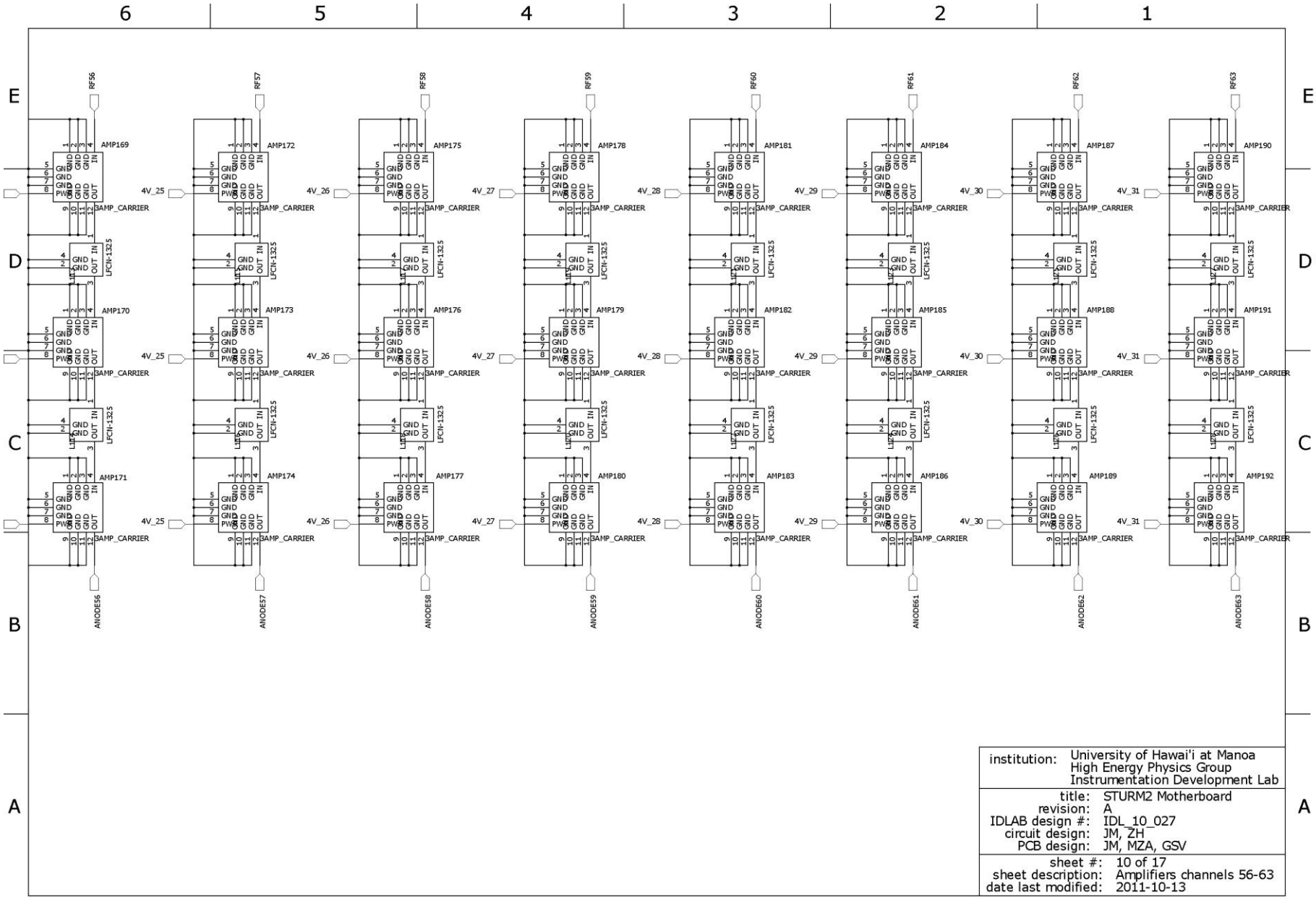
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	7 of 17
sheet description:	Amplifiers channels 31-39
date last modified:	2011-10-13

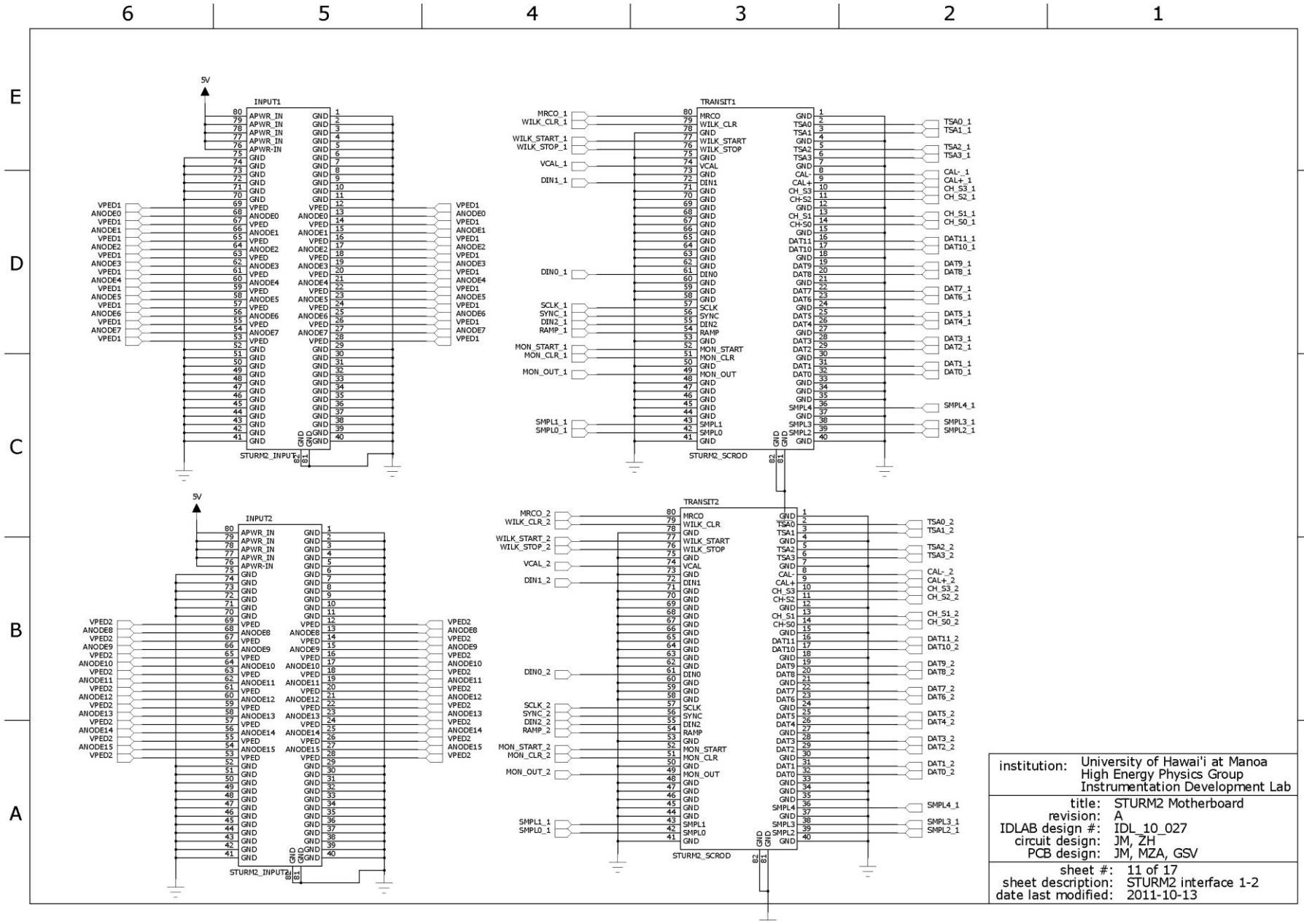


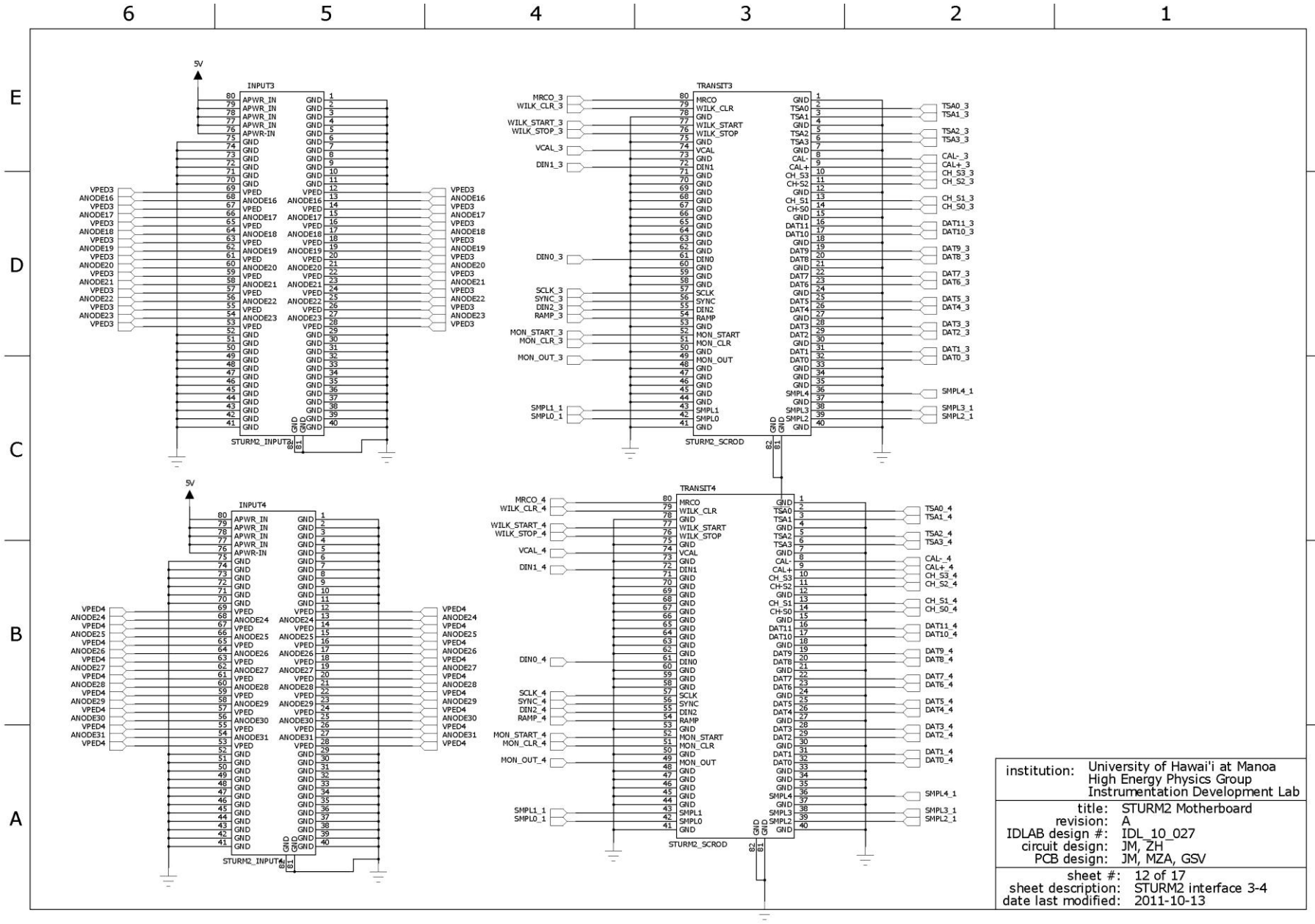
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	8 of 17
sheet description:	Amplifiers channels 40-47
date last modified:	2011-10-13

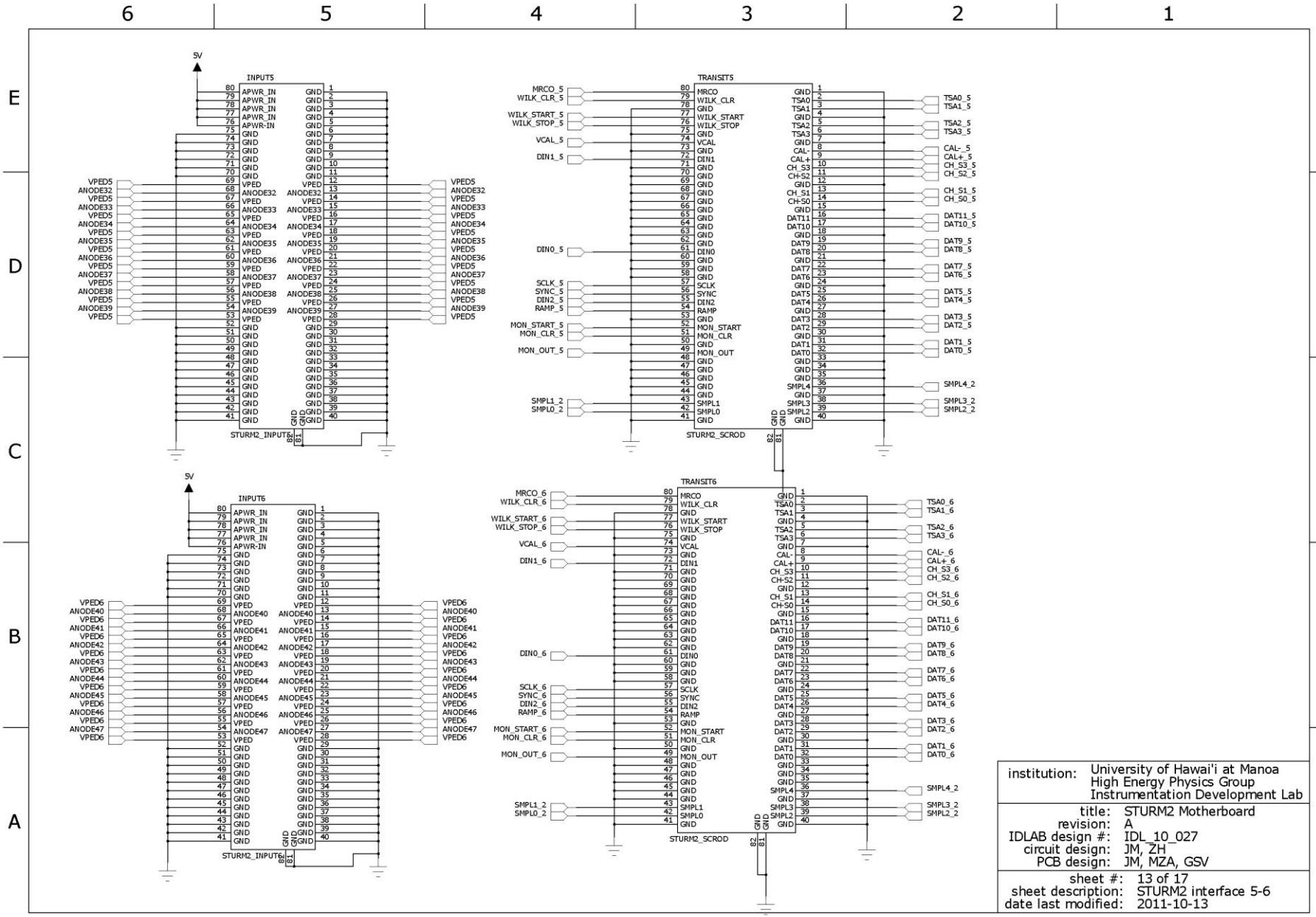


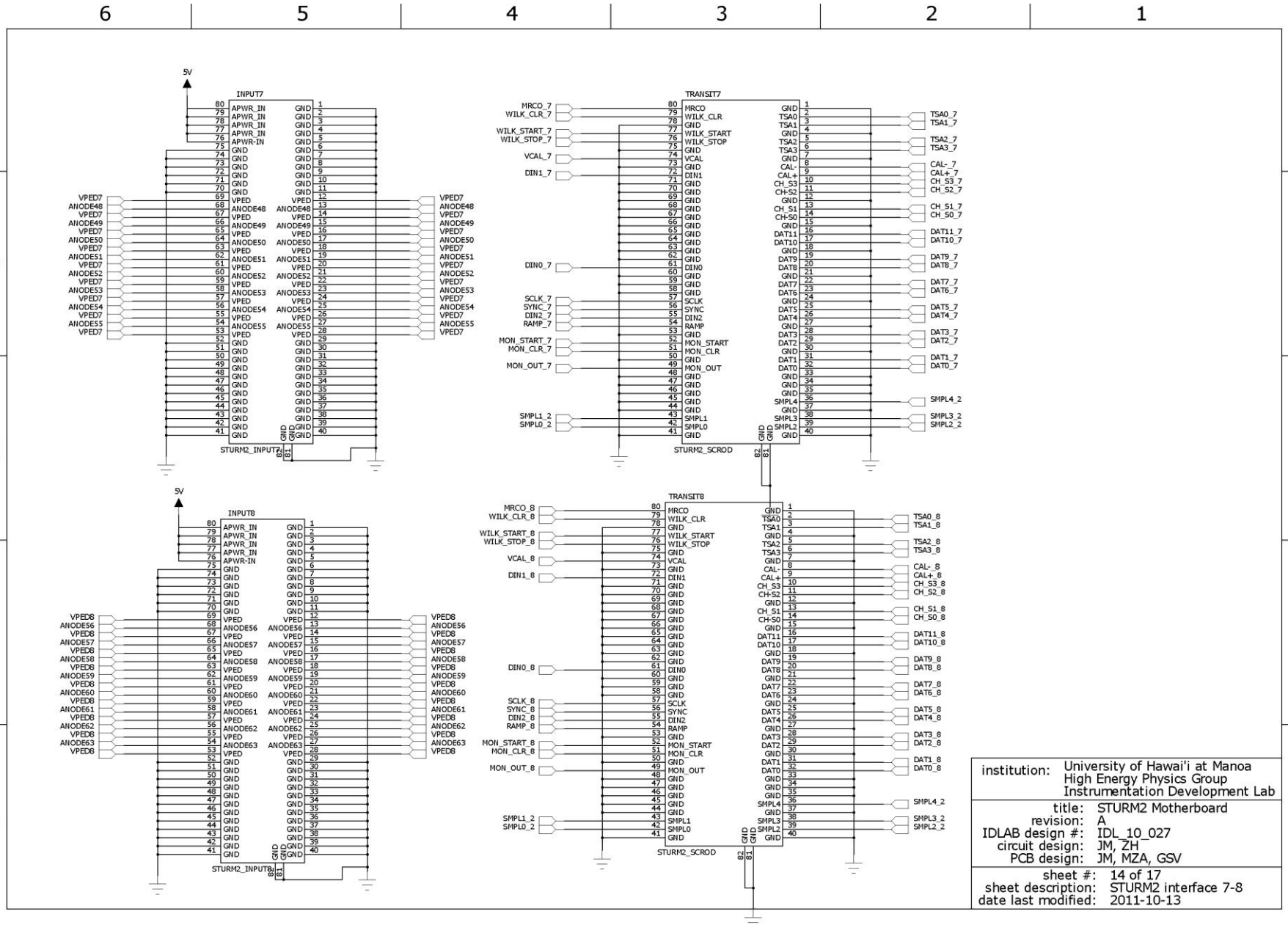
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	9 of 17
sheet description:	Amplifiers channels 48-55
date last modified:	2011-10-13

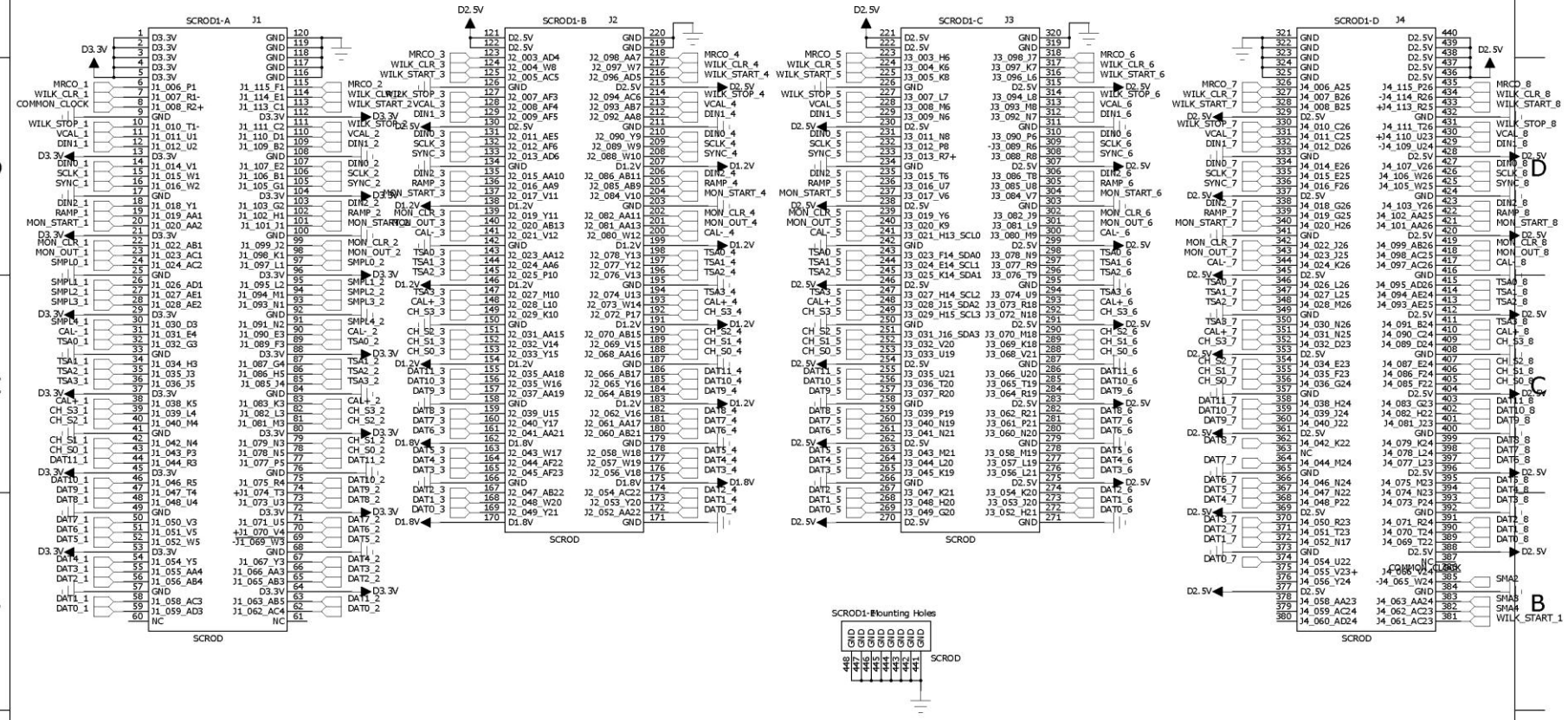

6
5
4
3
2
1
E
D
C
B
A
RF56
RF57
RF58
RF59
RF60
RF61
RF62
RF63
AMP169
AMP170
AMP171
AMP172
AMP173
AMP174
AMP175
AMP176
AMP177
AMP178
AMP179
AMP180
AMP181
AMP182
AMP183
AMP184
AMP185
AMP186
AMP187
AMP188
AMP189
AMP190
AMP191
AMP192
4V_25
4V_26
4V_27
4V_28
4V_29
4V_30
4V_31
3AMP_CARRIER
LFCN-1325
ANODE56
ANODE57
ANODE58
ANODE59
ANODE60
ANODE61
ANODE62
ANODE63
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 10 of 17
sheet description: Amplifiers channels 56-63
date last modified: 2011-10-13


6
5
4
3
2
1
E
D
C
B
A
5V
INPUT1
STURM2_INPUT
INPUT2
STURM2_INPUT
TRANSIT1
STURM2_SCROD
TRANSIT2
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 11 of 17
sheet description: STURM2 interface 1-2
date last modified: 2011-10-13

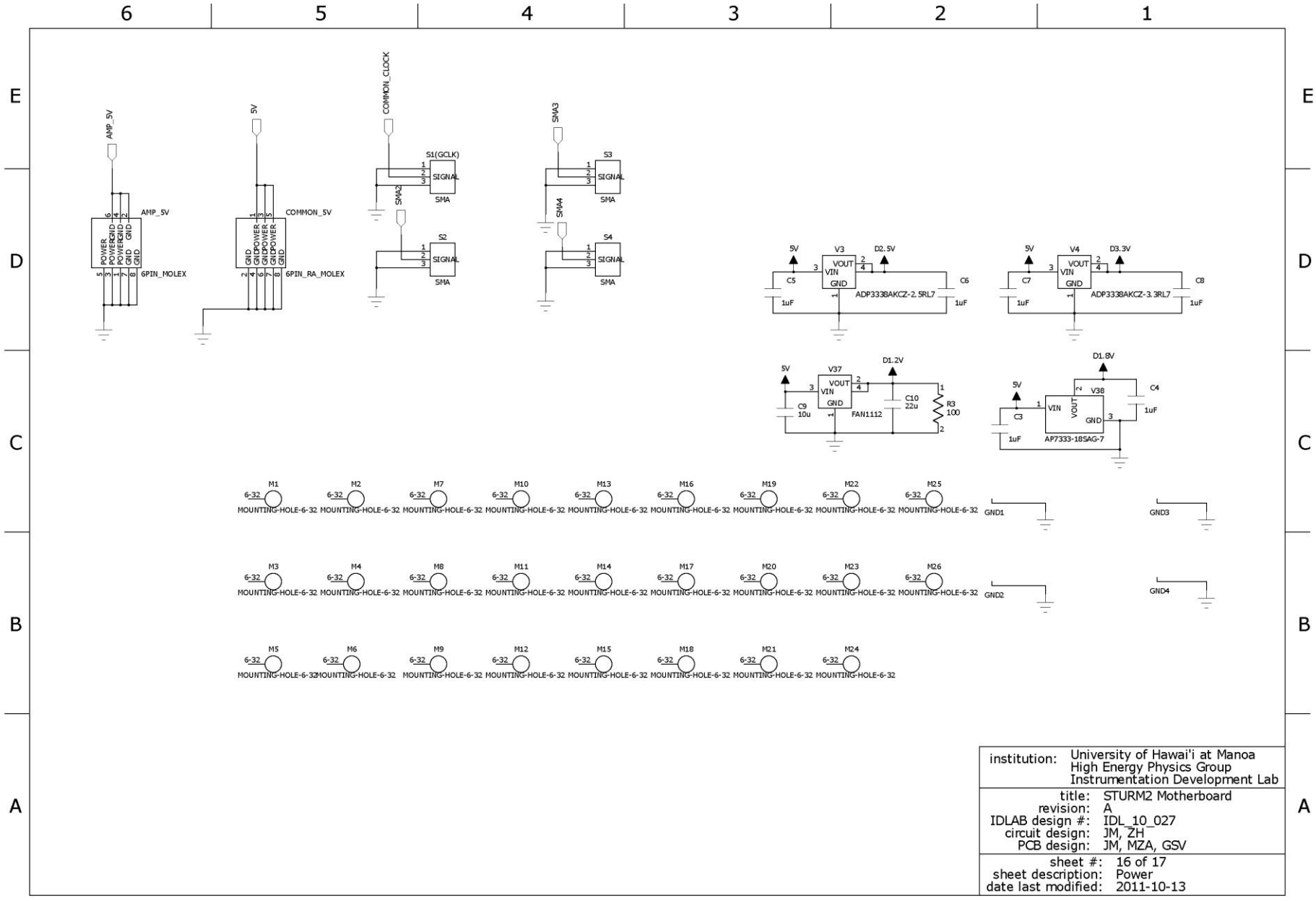

6
5
4
3
2
1
E
D
C
B
A
5V
INPUT3
STURM2_INPUT3
TRANSIT3
STURM2_SCROD
5V
INPUT4
STURM2_INPUT4
TRANSIT4
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 12 of 17
sheet description: STURM2 interface 3-4
date last modified: 2011-10-13

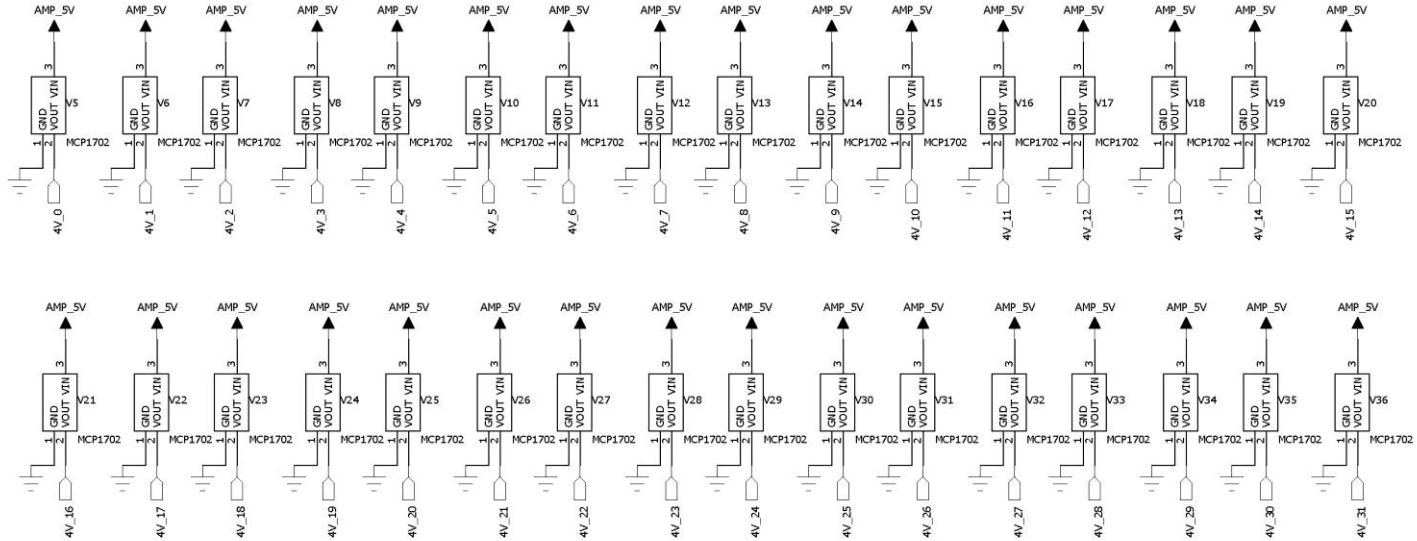

6
5
4
3
2
1
E
D
C
B
A
5V
INPUT5
STURM2_INPUT5
TRANSIT5
STURM2_SCROD
INPUT6
STURM2_INPUT6
TRANSIT6
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 13 of 17
sheet description: STURM2 interface 5-6
date last modified: 2011-10-13


6
5
4
3
2
1
E
D
C
B
A
5V
INPUT7
STURM2_INPUT7
TRANSIT7
STURM2_SCROD
INPUT8
STURM2_INPUT8
TRANSIT8
STURM2_SCROD
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 14 of 17
sheet description: STURM2 interface 7-8
date last modified: 2011-10-13



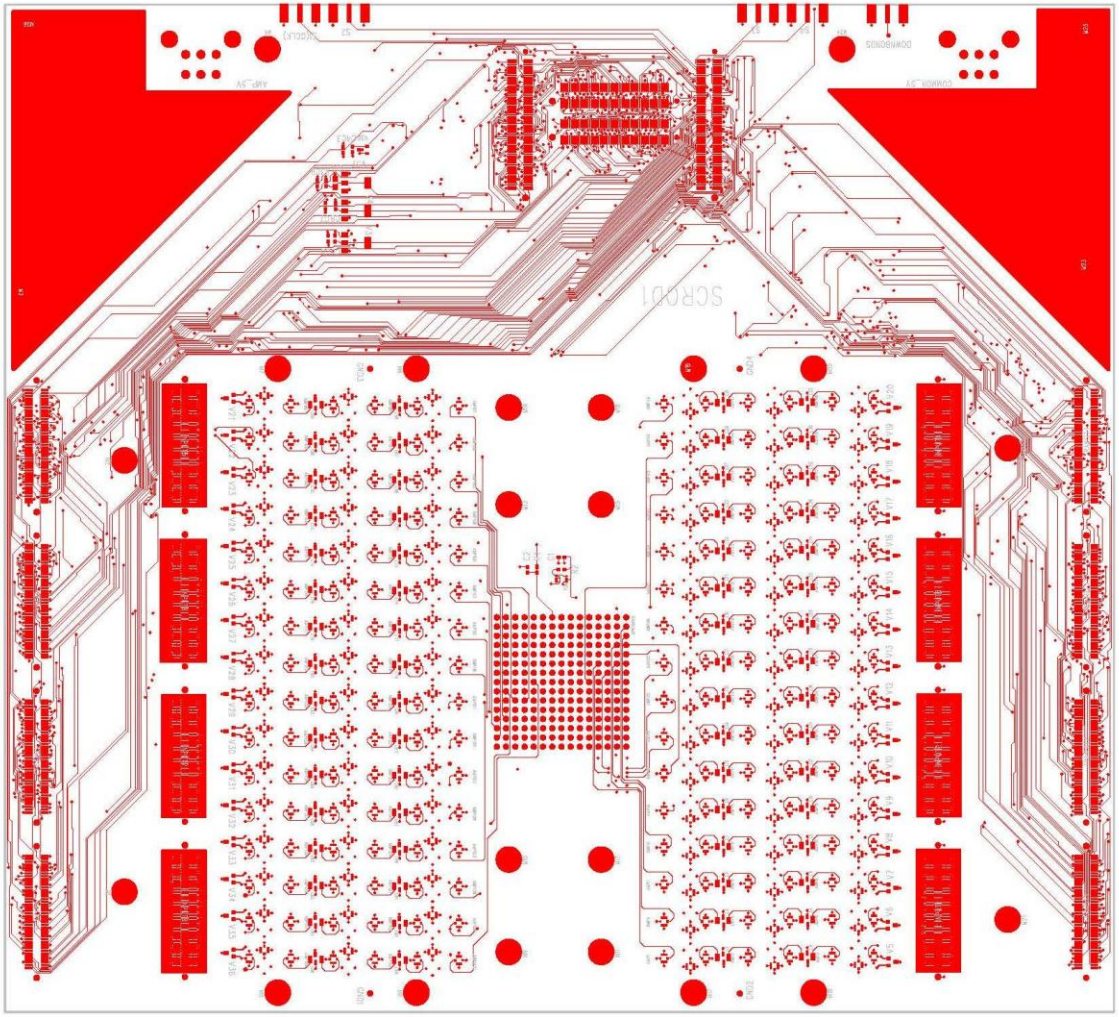
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	15 of 17
sheet description:	SCROD interface
date last modified:	2011-10-13


6
5
4
3
2
1
E
D
C
B
A
AMP_5V
AMP_5V
POWER
POWERGND
POWER
GND
GND
GND
6PIN_MOLEX
5V
COMMON_5V
GND
GNDPOWER
GNDPOWER
GNDPOWER
GND
6PIN_RA_MOLEX
COMMON_CLOCK
S1(GCLK)
SIGNAL
SMA
SMA2
S2
SIGNAL
SMA
SMA3
S3
SIGNAL
SMA
SMA4
S4
SIGNAL
SMA
5V
V3
VOUT
VIN
GND
D2.5V
C5
1uF
ADP3338AKCZ-2.5RL7
C6
1uF
5V
V4
VOUT
VIN
GND
D3.3V
C7
1uF
ADP3338AKCZ-3.3RL7
C8
1uF
5V
V37
VOUT
VIN
GND
D1.2V
C9
10u
FAN1112
C10
22u
R3
100
5V
V38
VOUT
VIN
GND
D1.8V
C3
1uF
AP7333-18SAG-7
C4
1uF
M1
M2
M7
M10
M13
M16
M19
M22
M25
M3
M4
M8
M11
M14
M17
M20
M23
M26
M5
M6
M9
M12
M15
M18
M21
M24
6-32
MOUNTING-HOLE-6-32
GND1
GND2
GND3
GND4
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: STURM2 Motherboard
revision: A
IDLAB design #: IDL_10_027
circuit design: JM, ZH
PCB design: JM, MZA, GSV
sheet #: 16 of 17
sheet description: Power
date last modified: 2011-10-13

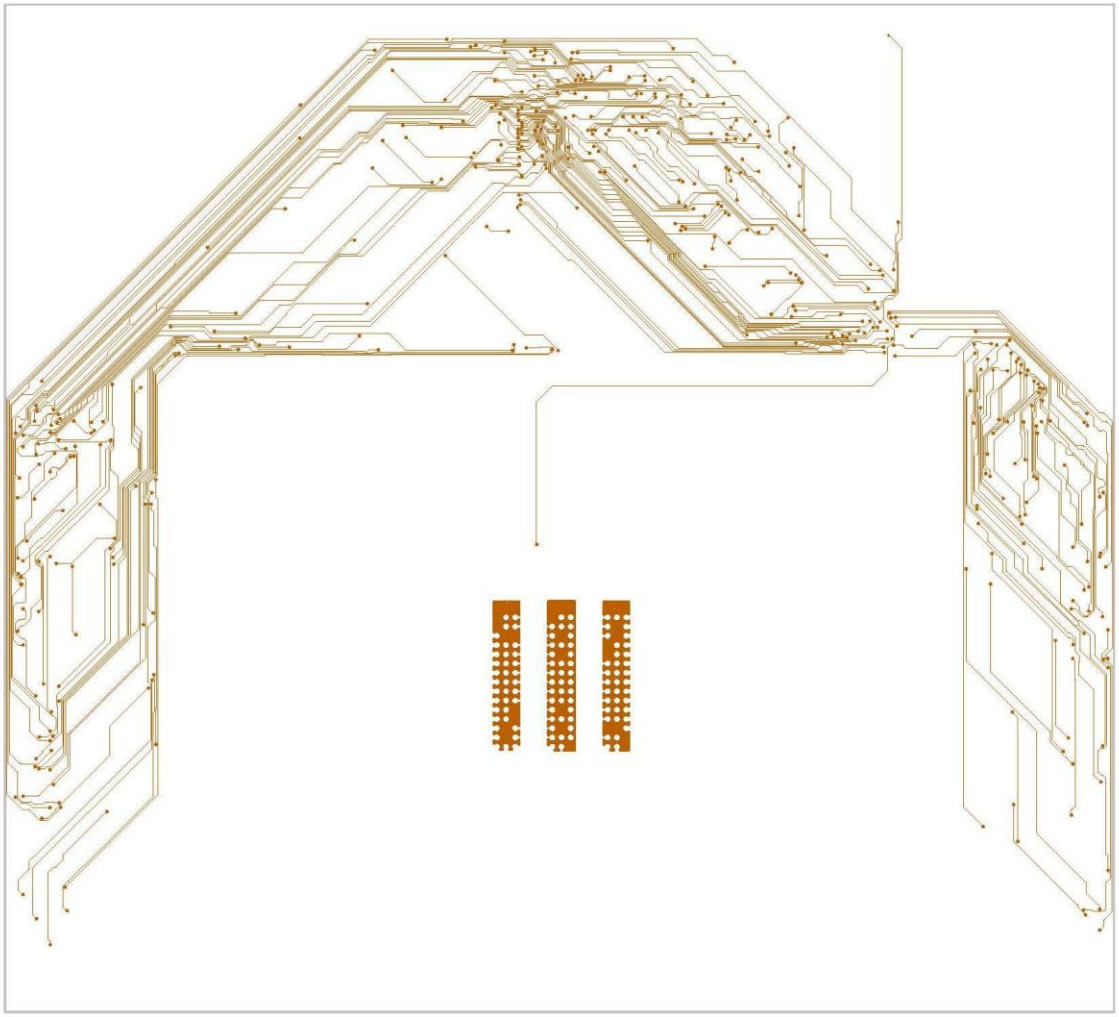


1 regulator for 2 channels

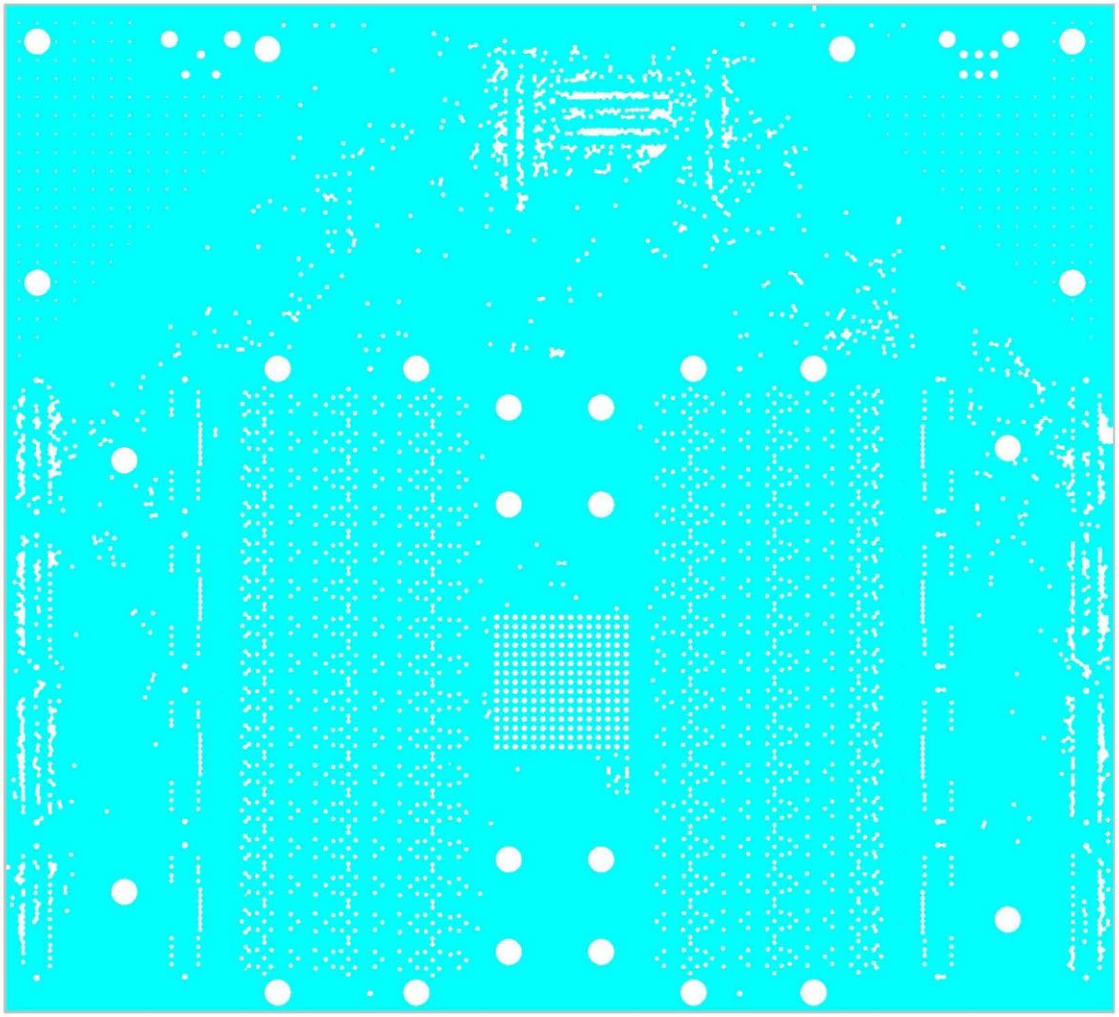
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	STURM2 Motherboard
revision:	A
IDLAB design #:	IDL_10_027
circuit design:	JM, ZH
PCB design:	JM, MZA, GSV
sheet #:	17 of 17
sheet description:	Amplifier power
date last modified:	2011-10-13



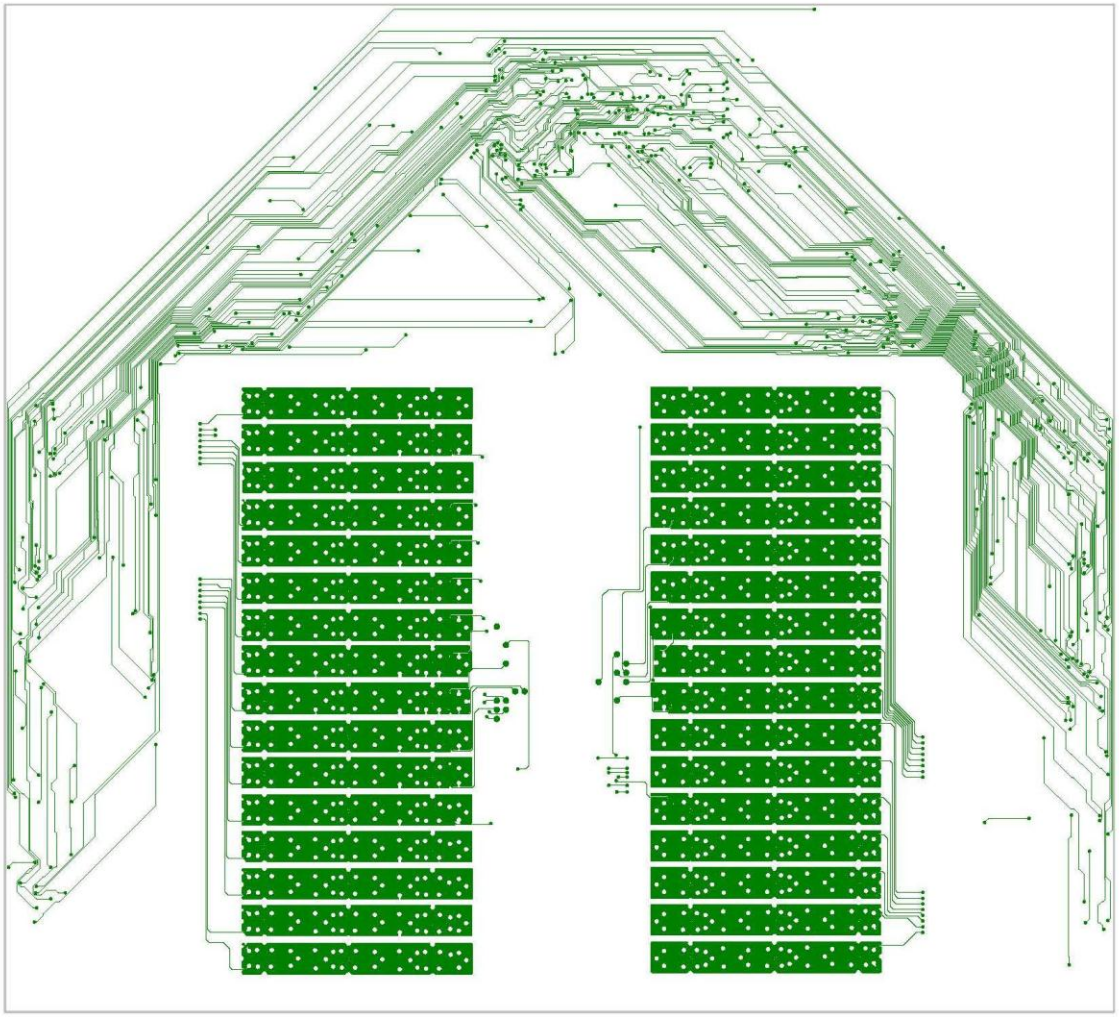
STURM2 motherboard top layer



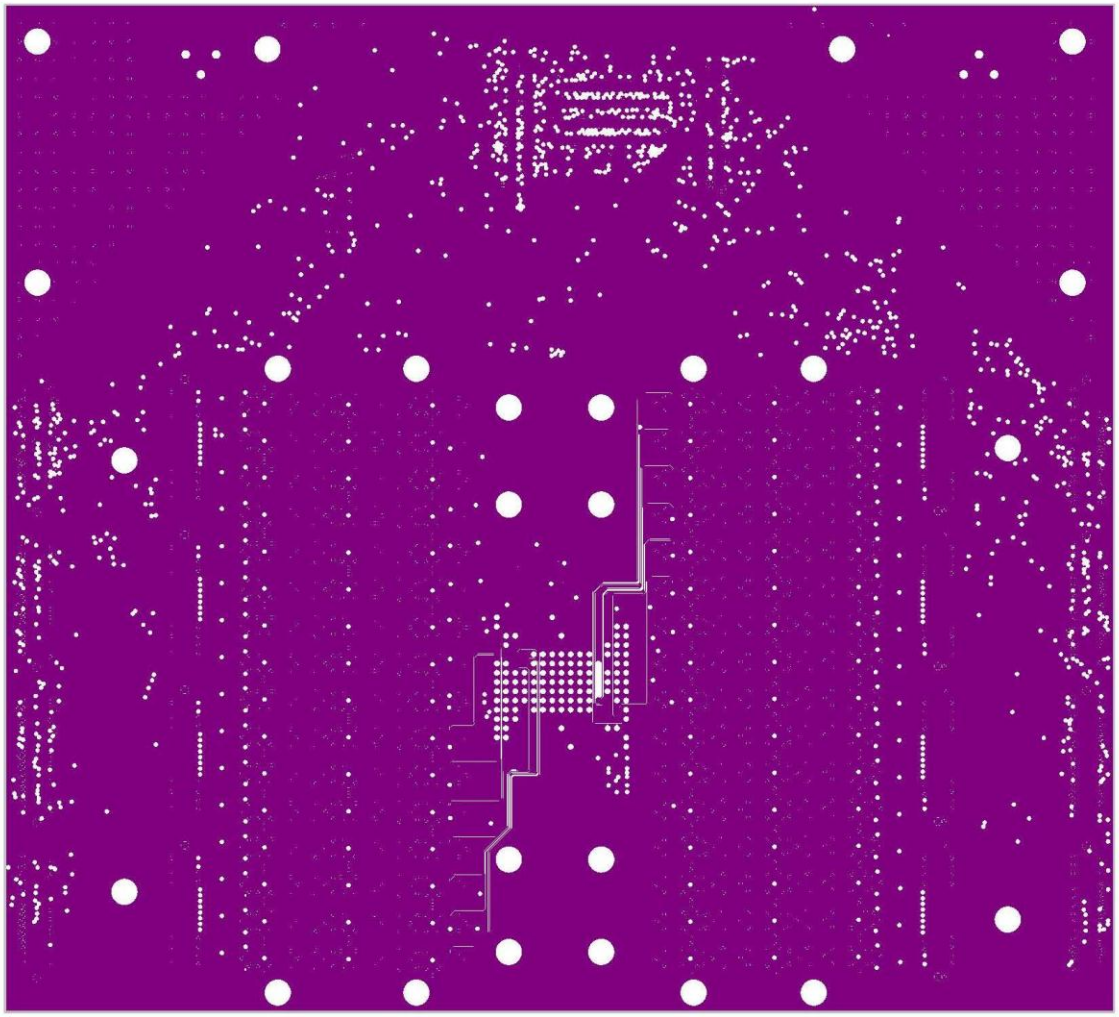
STURM2 motherboard inner layer 1, MISC.



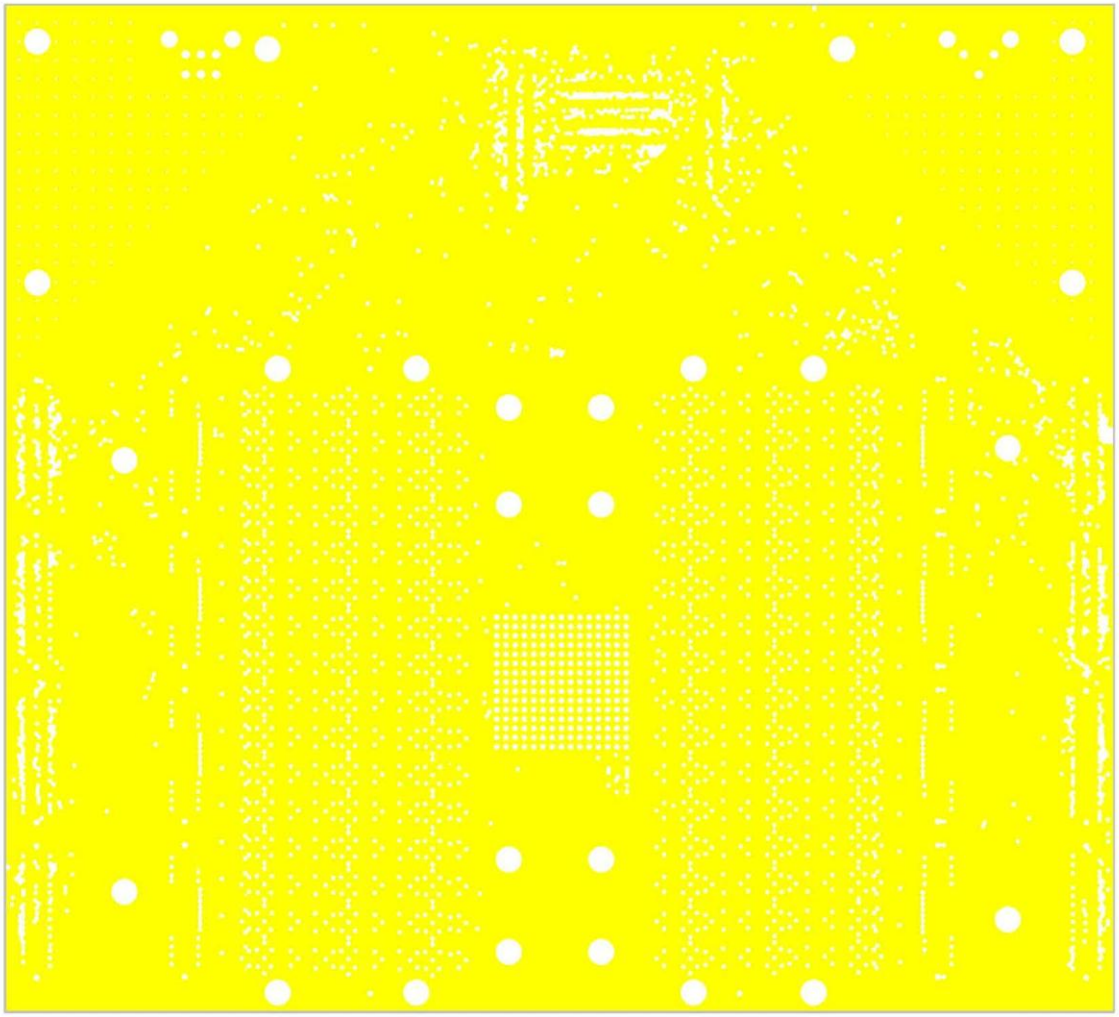
STURM2 motherboard inner layer 2, power plane 1.



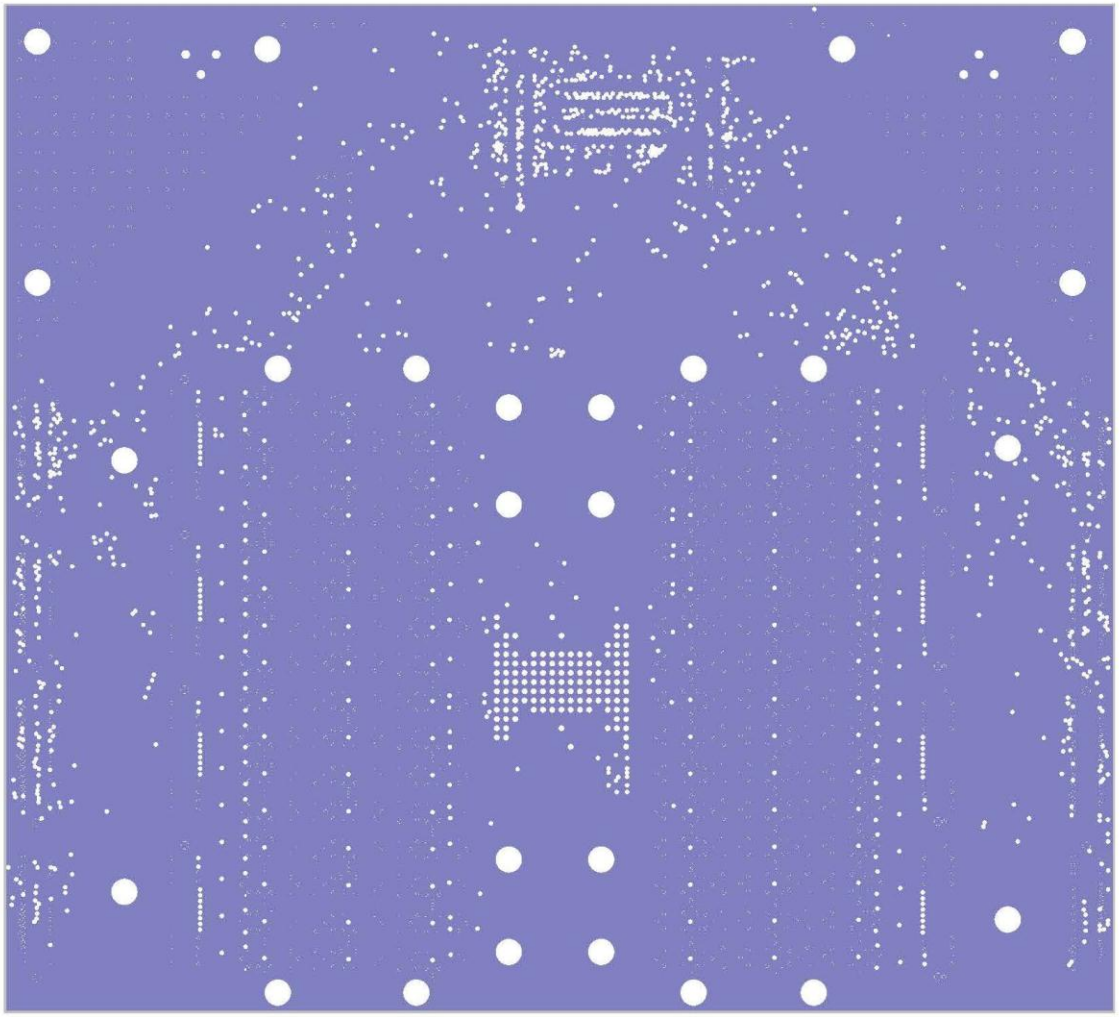
STURM2 motherboard inner layer 3, amplifier power.



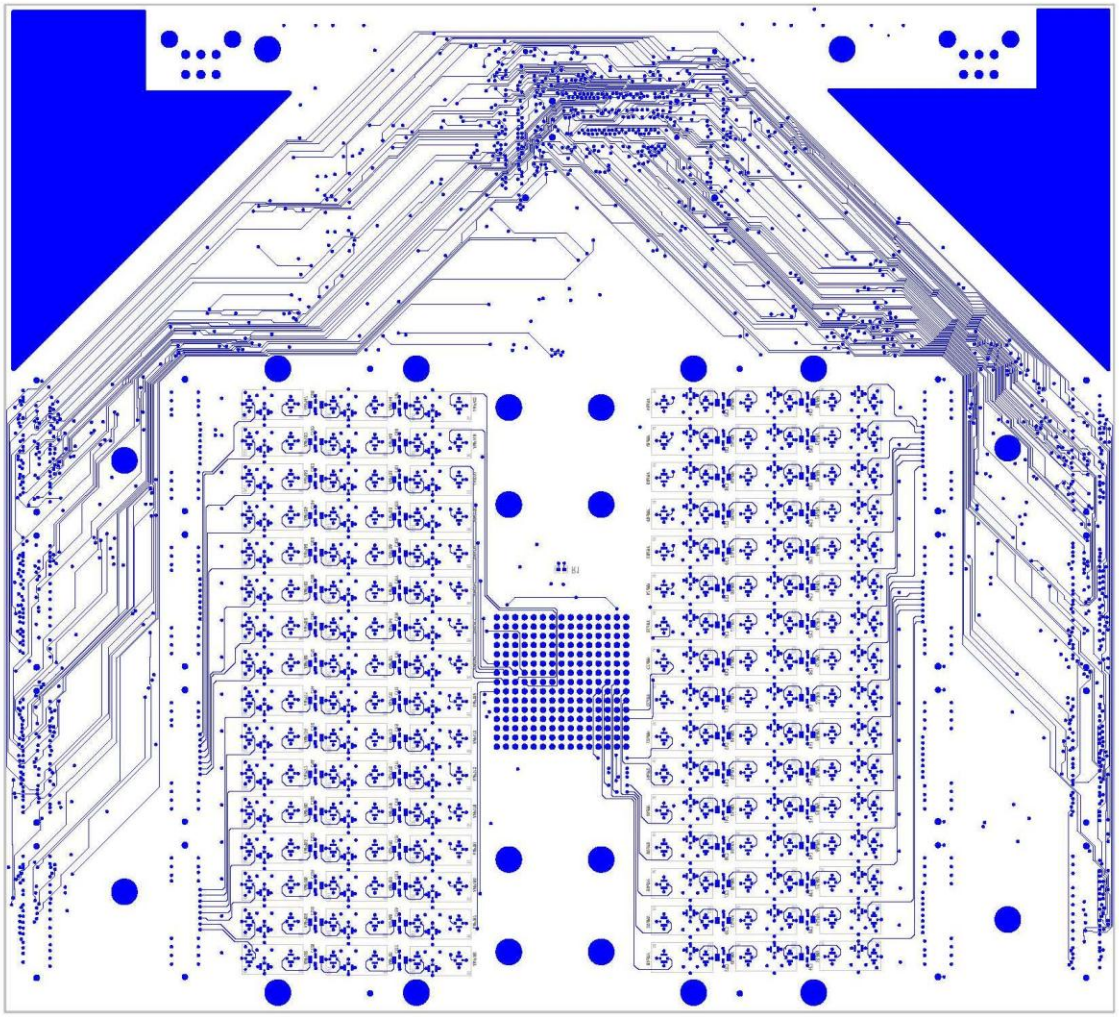
STURM2 motherboard inner layer 4, GND plane 1



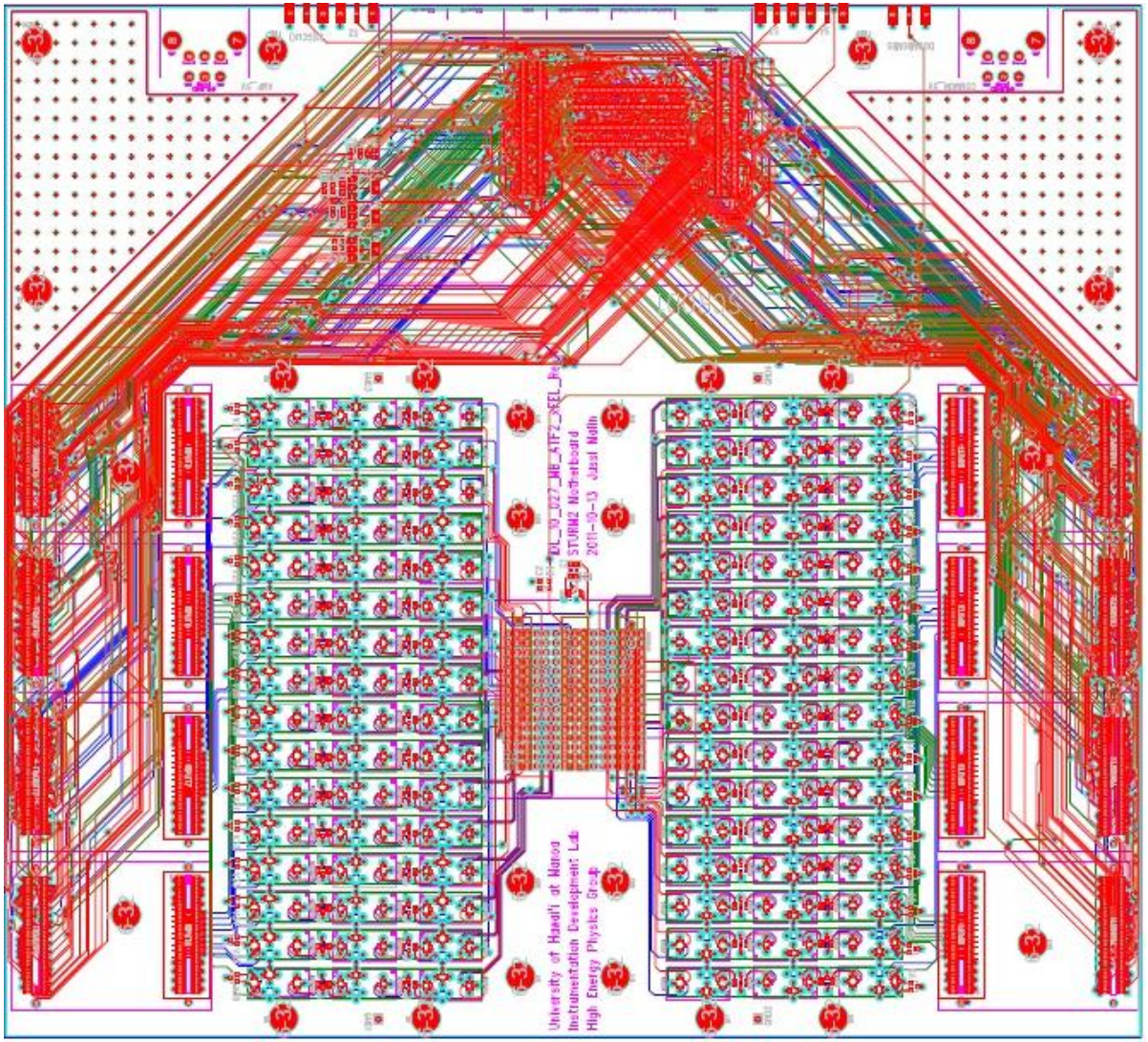
STURM2 motherboard inner layer 5, power 2.



STURM2 motherboard inner layer 6, GND plane 2.

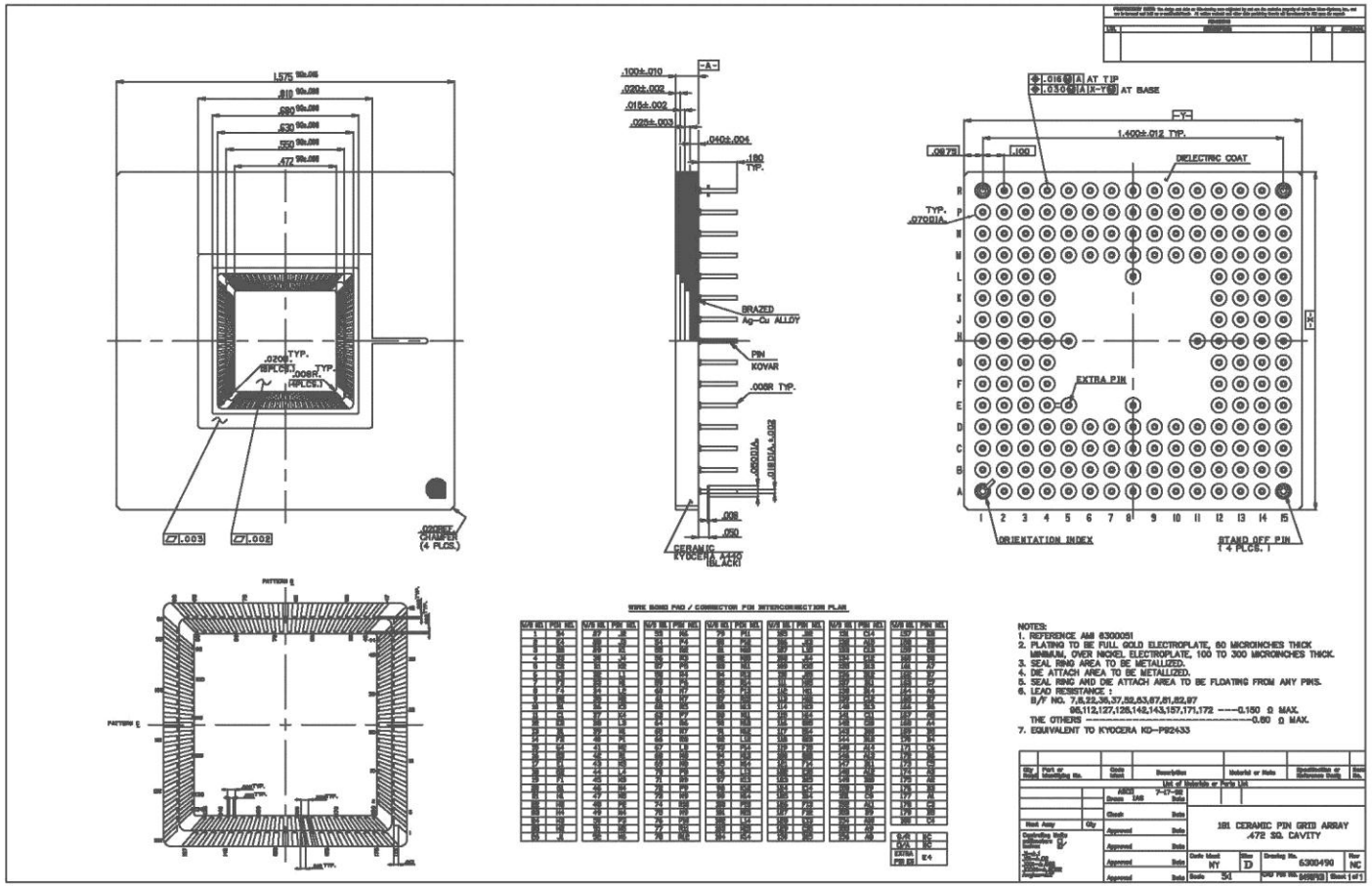


STURM2 motherboard bottom layer.



STURM2 motherboard composite

SSM P/N CPG18020



SPECTRUM SEMICONDUCTOR MATERIALS, INC.

Ph: 408.435.5555 email: ssm_sales@spectrum-semi.com

Motherboard bill of materials

Item	Qty	Reference	Part Name	Description	Part Nro	Distributor	In stock	Needed	Ordered
1	192	AMP1-192	3AMP_CARRIER	RF AMP 20 dB				384	384
2	16	CONNECTOR	BLAB3A_DC	CONN RCPT 80POS .8MM FH 5H 8AU	A99191CT-ND	Digi-Key		32	32
3	128	L1-128	LFCN-1325	LOW PASS FLTR / SURF MT / RoHS	LFCN-1325+	Mini Circuits		256	256
4	1	SENSOR	PGA_SOCKET_15X15					2	2
5	1	SCROD1	SCROD					2	2
6	576		MHF 4 SMT RECEPTACLE	ULTRA SMALL COAXIAL CONNECTOR	20449-001E	I-PEX	900	1152	252
7	2	V1,V2	6PIN_RA_MOLEX	6 PIN POWER CONNECTOR				4	4
8	1	V3	ADP3338AKCZ-2.5RL7	IC REG LDO 1A PREC 2.5V SOT-223	ADP3338AKCZ-2.5RL7CT-ND	Digi-Key		2	2
9	1	V4	ADP3338AKCZ-3.3RL7	IC REG LDO 1A PREC 3.3V SOT-223	ADP3338AKCZ-3.3RL7CT-ND	Digi-Key		2	2
10	32	V5-36	MCP1702	IC REG LDO 4V 250MA SOT89-3	MCP1702T-4002E/MBCT-ND	Digi-Key		64	64
11	1	V37	FAN1112	IC REG LDO 1A 1.2V TO-252	FAN1112DXTR-ND	Digi-Key		2	2
12	1	V38	AP7333-18SAG-7	IC REG LDO 1.8V 0.3A SOT23	AP7333-18SAG-7DICT-ND	Digi-Key		2	2
13	1	V39	LT3020EDD	IC REG LDO ADJ 100MA LV 8-DFN	LT3020EDD#PBF-ND	Digi-Key		2	2
14	3	C1,C9	CAP0603,10uF	CAP CER 10UF 6.3V 10% X5R 0603	445-7492-1-ND	Digi-Key		6	6
15	6	C3-8	CAP0603,1uF	CAP CER 1000PF 50V 10% X7R 0603	490-1494-1-ND	Digi-Key		12	12
16	1	C10	CAP0805,22uf	CAP TANT 22UF 6.3V 10% 0805	478-4188-1-ND	Digi-Key		2	2
17	1	C2	CAP0603,1.6pF	CAP CER 1.6PF 50V C0G 0603	490-1377-1-ND	Digi-Key		2	2
18	1	R3	RES0603,100	RES 100 OHM 1/10W 5% 0603 SMD	RMCF0603JT100RCT-ND	Digi-Key		2	2
19	1	R2	RES0603,105K	RES 105K OHM 1/10W 1% 0603 SMD	RMCF0603FT105KCT-ND	Digi-Key		2	2
20	1	R1	RES0603,20K	RES 20K OHM 1/10W 5% 0603 SMD	RMCF0603JT20K0CT-ND	Digi-Key		2	2
21	1	R4	RES0603,	RES 1K OHM 1/10W 5% 0603 SMD	RMCF0603JT1K00CT-ND	Digi-Key		2	2
22	5	S1-5	SMA	CONN JACK SMA 50 OHM EDGE MOUNT	WM5534-ND	Digi-Key	0	10	10
23	4	TP1-4	TH_TESTPT	GROUND TEST POINT					

STURM2 ASIC board bill of materials

Item	Qty	Reference	Part Name	Value	Description	Part Nro	Distributor	In stock	Needed	Ordered
1	3	U1-3	AD5324		IC DAC 12BIT QUAD VOUT 10-MSOP	AD5324BRMZ-ND	Digi-Key		48	48
2	2	C1-2	BLAB3A_DC		CONN PLUG 80POS .8MM FH 5H GOLD	A99197CT-ND	Digi-Key		32	32
3	25	C1-2 C4 C6 C8 C10 (	CAP0603	0.1uF	CAP CER .10UF 25V X7R 10% 0603	445-1316-1-ND	Digi-Key		400	400
4	1	C37	CAP0603	1000pF	CAP CER 1000PF 50V 10% X7R 0603	490-1494-1-ND	Digi-Key		16	16
5	22	C3 C5 C7 C9 C11 C1	CAP0603	10uF	CAP CER 10UF 6.3V 10% X5R 0603	445-7492-1-ND	Digi-Key		352	352
6	3	C39 C41 C43	CAP1206	100uF	CAP CER 100UF 6.3V Y5V 1206	490-4512-1-ND	Digi-Key		48	48
7	1	V3	MCP1826S-2502E		IC LDO REG 1A 2.5V SOT223-3	MCP1826S-2502E/DB-ND	Digi-Key		16	16
8	2	V1-2	MCP1826T-ADJE		IC LDO REG 1A ADJ-V SOT223-5	MCP1826T-ADJE/DCCT-ND	Digi-Key		32	32
9	3	R5-6 R10	RES0603	10k	RES 10K OHM 1/10W 5% 0603 SMD	RMCF0603JT10K0CT-ND	Digi-Key		48	48
10	1	R8	RES0603	12k	RES 12K OHM 1/10W 5% 0603 SMD	RMCF0603JT12K0CT-ND	Digi-Key		16	16
11	1	R9	RES0603	14.3k	RES 14.3K OHM 1/10W 1% 0603 SMD	RMCF0603FT14K3CT-ND	Digi-Key		16	16
12	1	R2	RES0603	200k	RES 200K OHM 1/10W 5% 0603 SMD	RMCF0603JT200KCT-ND	Digi-Key		16	16
13	2	R1 R4	RES0603	20k	RES 20K OHM 1/10W 5% 0603 SMD	RMCF0603JT20K0CT-ND	Digi-Key		32	32
14	1	R7	RES0603	23.2k	RES TF 23.2K OHM 1% 0.1W 0603	RMCF0603FT23K2CT-ND	Digi-Key		16	16
15	1	R3	RES0603	50	RES 50 OHM 125MW +/-5% 0603 SMD	FC0603E50R0JST1-ND	Digi-Key		16	16
16	1	STURM2	STURM2						16	16
17	1	RAMP	TH_TESTPT						16	16
18	1	U4	TN2-5V		RELAY SLIM VERT 1A 5VDC PC MNT	255-1022-5-ND	Digi-Key		16	16
19	1	Q1	ZVN3306		MOSFET N-CH 60V 150MA SOT23-3	ZVN3306FCT-ND	Digi-Key		16	16
20	1	Q2	ZVP3306F		MOSFET P-CH 60V 90MA SOT23-3	ZVP3306FCT-ND	Digi-Key		16	16
14	1	V39	LT3020EDD		IC REG LDO ADJ 100MA LV 8-DFN	LT3020EDD#PBF-ND	Digi-Key		16	16

Amplifier board bill of materials

Item	Qty	Reference	Part Name	Value	Description	Part Nro	Distributor	In stock	Needed	Ordered
1	1	U1	ABA-31563		IC AMP RFIC 3.5GHZ 3V SOT-363	516-1490-1-ND	Digi-Key		384	384
2	3	C1-3	C0201	1000pF	CAP CER 1000PF 25V X7R 0201	490-3184-1-ND	Digi-Key		1152	1152
3	2	C4-5	CAP0603	1uF	CAP CER 1000PF 50V 10% X7R 0603	490-1494-1-ND	Digi-Key		768	768
4	1	L1	IND-MOLDED	620nH	MOLDED INDUCTOR 0.5" PIN SPACING	535-10549-1-ND	Digi-Key		384	384
5	1	SS1	SHIELD_SMALL						384	384
6	1	N1	STLQ015XX		IC REG LDO 3V 0.15A SOT666	497-10547-1-ND	Digi-Key	200	384	184
7	1	U2	LAT-2		FXD ATTEN / SURF MT / RoHS	LAT-2+	Mini Circuits		384	384
8	3	M1-3	MHF 4 SMT PLUG		ULTRA SMALL COAXIAL CONNECTOR	20462-001E	I-PEX	900	1152	252


SAVONIA