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# Phase Locked Loop (PLL)

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The main purpose of this project was to design a PLL circuit which can be locked at 1GHZ with four factors of frequency division (10, 20, 40 and 80). Phase Locked Loops (PLLs) are feedback systems that generate phase-locked signals in response to external input signals. PLLs are used to generate an output signal with a programmable frequency., rational multiple of a fixed input frequency. In other words, PLLs are used to lock or track input signals in frequency and phase. When the phase and frequency of the input signals are synchronized, the PLL is said to be in the locked condition. The phase difference between the output signal and the reference is a known value when the loop is locked.

To perform the PLL circuit a PCB was designed using PADS, and printed using the milling machine in the university laboratory.
The main component of the PLL circuit are Prescaler, Active Loop Filter, Mixer, Power splitter, variable resistor and A voltage-controlled oscillator (VCO). The Prescaler, mixer, power splitter and VCO are surface mount component (SMD).

The goal of this thesis to achieve a locked state of PLL system was not achieved successfully. After checking and testing the board the results shows that the only thing that not working is the prescaler because the output of it was giving wrong signals to the mixer. Also when changing the division factors they were not affecting in the output.

| | |
|---|---|
| Keywords | PLL, Loop filter, PCB, VCO, SMD |

## Contents

List of Abbreviations

List of Figures
List of Tables

1 Introduction 1

1.1 Introduction to Phase Locked Loop 2

2 Terms in PLL 3

2.1 Lock Scale 3
2.2 Capture Range 3
2.3 Pull in Time 4
2.4 Bandwidth of PLL 4
2.5 Noise in PLL 4
2.5.1 Phase Noise 4
2.5.2 Jitter 5
2.5.3 Spur 5
2.5.4 Charge Pump Leakage Current 6

3 PLL Types 6

3.1 Analog Phase-Locked Loop (APLL). 6
3.2 Linear Phase-Locked Loop (LPLL). 7
3.3 Digital Phase-Locked Loop (DPLL). 8
3.4 All Digital Phase-Locked Loop (ADPLL). 9
3.5 Software phase-locked loop (SPLL). 10

4 Uses of PLL 10

4.1 Frequency Synthesizer 10
4.2 Clock Generation 11
4.3 Skew Reduction 11
4.4 Carrier Recovery (Clock Recovery) 11
4.5 Jitter and Noise Reduction 12

5 Building Blocks of a PLL 12

5.1 Mixer (Phase Detector) 12
Mixer type: SYM-11LH+ (SMD) 1-2000 Mhz. **Error! Bookmark not defined.**
5.2 Loop Filter 13
5.3 VCO 15
5.4 Prescaler 19
6 Operating Principle of a PLL 20
7 Design and Measurement 21
7.1 Two Additional Tasks 26
8 Discussion and Conclusion 29
9 References 30
Appendices
Appendix 1. Measurement setup and the 1GHz output.

## List of Abbreviations

| | |
|---|---|
| AC | Alternating Current |
| ADPLL | All Digital Phase-Locked Loop |
| APLL | Analog Phase-Locked Loop |
| CP | Charge Pump |
| dB | Decibels |
| DC | Direct Current |
| DCO | Digitally Controlled Oscillator |
| DPLL | Digital Phase-Locked Loop |
| GHz | Gigahertz |
| LPLL | Linear Phase-Locked Loop |
| LO | Local Oscillator |
| PFD | Phase Frequency Detector |
| PLL | Phase Locked Loop |
| RF | Radio Frequency |
| SMD | Surface Mount Device |
| SPLL | Software Phase-Locked Loop |
| VCO | Voltage Controlled Oscillator |

## List of figures


Figure 1. PLL Block diagram of the project. 2

Figure 2. Illustration of lock and capture range. 3

Figure 3. Output current pulses from charge pump in the lock state. 5

Figure 4. Block diagram of the Analog phase-locked loop. 6

Figure 5. LPLL Block diagram. 7

Figure 6. The various ranges of interest for a linear PLL. 7

Figure 7. DPLL Block Diagram. 9

Figure 8. All digital phase-locked loop Block Diagram. 10

Figure 9. CP Out of the case of frequency lock and phase lock. 13

Figure 10. Schematic of single-pole single-zero active loop filter. 14

Figure 11. Active loop filter set with resistance and capacitance value. 15

Figure 12. Transfer Function of VCO. 16

Figure 13. Tuning voltage in line graph. 18

Figure 14. Schematic for PLL circuit. 21

Figure 15. PCB layout for the Final PLL circuit. 23

Figure 16. PCB layout for the smallest size of PLL circuit. 23

Figure 17. 1GHz wires width. 24

Figure 18. Final PCB board. 25

Figure 19. Bottom layer of the final PCB board. 26

Figure 20. PLL schematic without the prescaler, regulator and switches. 27

Figure 21. PLL layout without the prescaler, regulator and switches. 27

Figure 22. PLL schematic without the prescaler and loop filter. 28

Figure 23. PLL layout without the prescaler and loop filter. 28

## List of Tables

Table 1. Performance Data & Curves of the VCO. 17

Table 2. JTOS-1300+VCO Tuning sensitivity table from 900MHz to 1100MHz. 18

Table 3. Control signal states and their corresponding division factors. 19

# 1 Introduction

The aim of proposed thesis is to design a PLL PCB with SMD components along with locked at 1GHz. PLL (Phase Locked Loop) can be interpreted as a common circuit block in wireless applications and radio frequency. It is beneficial for many operations in radio, wireless, and from Cell phones to Transmitting radios and TV to Wi-Fi routers. PPL has wide range of applicability in walkie-talkie radios and state-of-the-art professional communications systems encapsulating many other related latest communication platforms.

PPL operations relies majorly on the difference of output signal and reference signal that is also considered as vital factor for PPL flow of operations. The reference signal (Input) comes from the oscillator and the output signal which come from the Voltage Controlled Oscillator (VCO). It has ability to detect both of it and in case of error detection, phase processes this information to monitor the frequency of the specified loop. Phase and phase difference belongs to two different conceptual frameworks. They can be viewed as two distinguished waveforms conventionally considered as sine waves additionally visible on oscilloscope. If both signals are subjected to fire through trigger, both signals will be shown at different locations at the screen.

Fundamental aspect of PPL is to drive a VCO in order to produce a specified signal of high and stable frequency. Critical point to consider is that the phase locked output oscillator is actually output of respective VCO that is operational through the PLL. While considering this aspect, merely utilizing a VCO instead of PPL might considered as same, PPL assists VCO for creating more stable and precise frequency. The output of an individual operating VCO is not contemplate as stable. Various external factors i.e. noise and temperature poses affects on the output of VCO. Furthermore, it also results in making the unstable output signal with respect to frequency. In order to generate signals with stable and precise frequency, a PPL can be effectively utilized with a local or reference oscillator. It also provides assurance that the VCO is capable of oscillating at a stable frequency. Sometimes, internal or external factors causes change in the frequency of VCO, in such cases the PPL synchronizes accordingly in order to balance the output.

## 1.1 Introduction to Phase Locked Loop

PLL basically relies on the difference of phases among the feedback clock signal and input clock signal related to controlled oscillator. It can viewed as a closed-loop frequency-control system as well [1]. In other words, PLL can be designated as an electronic feedback system that is operational with the assistance of consecutively changing a voltage or current-driven oscillator. This behavior helps in matching with the input signal phase along with frequency particularly. To attain the desired output signal, addition, multiplication and division/mixing various frequencies can be achieved through PLL. PLLs are composed of the below mentioned components and various types:

Components

- Voltage Controlled Oscillator (VCO)
- Error comparator/detector
- Loop filter
- Prescaler feedback counter
- Power splitter

Types

- Analog phase-locked loop (APLL)
- Linear phase-locked loop (LPLL)
- Digital phase-locked loop (DPLL)
- All digital phase-locked loop (ADPLL)
- software phase-locked loop (SPLL)

Above mentioned components that forms a PLL are illustrated in figure 1.

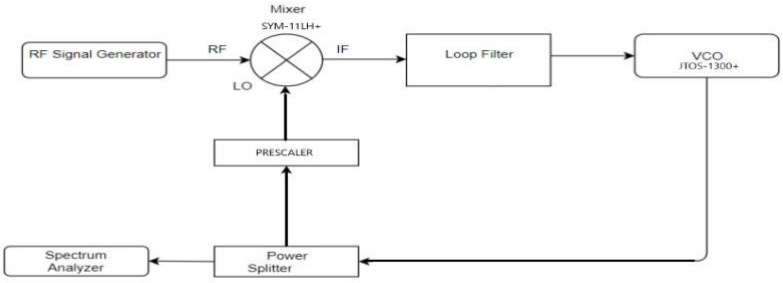


Figure 1. PLL Block diagram of the project.

# 2 Terms in PLL

There are five terms that describe the operations in the PLL.

## 2.1 Lock Scale

Scale of input signal frequencies through which the loop stays locked when it has caught the input signal. This factor can be limited either through the phase detector or through VCO frequency range. When the lock is departed in the PLL circuit, the VCO starts performing its operation at the free-running frequency the free-running frequency is between the $fmin$ and

$fmax$. Also, the lock range is always wider than the capture range.

## 2.2 Capture Range

Capture Range can be defined as a frequency range that can inhibits PLL lock even if it is not in Lock beforehand. This character is also known as acquisition range. On the other hand, loop filter bandwidth improvises the rate of rejection of the out of band signals. Meanwhile, the capture range falls and pull in the targeted time to become enormous. On the other hand, phase margin becomes decremented. These starting and ending points of lock and capture range are depicted in figure 2.

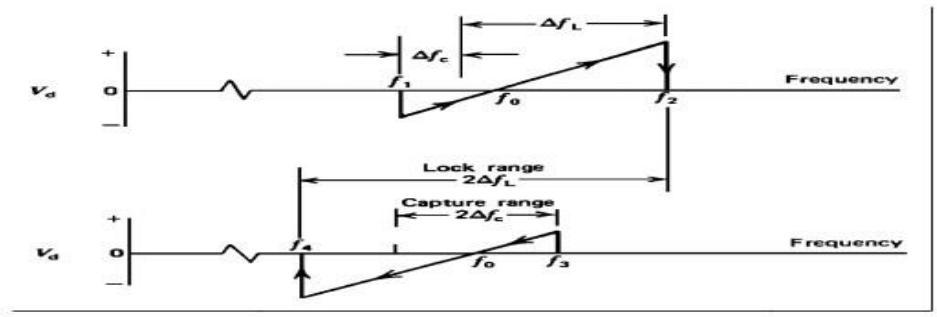


Figure 2. Illustration of lock and capture range.

## 2.3 Pull in Time

The amount of time held by the PLL to catch the specified signal (or to create the lock) is known as Pull in Time. It is also named as PLL Acquisition Time.

## 2.4 Bandwidth of PLL

Rate of frequency at which the PLL start to drop the lock with reference is known as Bandwidth. The advantages of high-bandwidth includes provision of a rapid lock time with tracking of jitter corresponding to reference clock source. Moreover, it is capable of tracking a broad spread-spectrum clock through utilizing high-bandwidth setting. The primary effect related to low-bandwidth is the reaction of PLL that keeps on changing slowly by its input clock along with taking prolonged time duration to get down towards lower frequency.

## 2.5 Noise in PLL

Noise in PLL can be explained as phenomenon through which the practical system's output diverges from the expected response. Noise might originates due to existence of flawed parameters present in the system. The noise occurrences additionally influence the PLL system's output.

Four types of noises are described as given:

### 2.5.1 Phase Noise

When random frequency transition of a signal gives rise to phase fluctuations, it is known as Phase noise. On a majority basis, it is affected by oscillator’s frequency stability. The primary sources that are present in PLL are frequency divider circuit, oscillator noise and PFD. whereas, there are two principal components related to phase noise i.e. flicker and thermal noise.

### 2.5.2 Jitter

Short-lived transitions of a signal corresponding to its expected position with respect to specific time is know as jitter. Jitter affects the rate of data transmission quality negatively. Phase and Jitter noise are approximately correlated to each other and can be evaluated from each another. There are two factors that can cause deviation from the expected position i.e. either by leading edge or through trailing edge of respective signal. In few cases, Jitter might be instigated by a clock signal with various different sources and lack of uniformity throughout entire frequencies also exist. In parallel, excessive jitter results in increased Bit Error Rate (BER) of the communication signal. Contraventions related to time margins and improper conduct of circuits are other significant consequences of Jitter among digital systems [8].

### 2.5.3 Spur

Undesirable frequency that is irrelevant to the frequency of oscillation and related harmonics is known as “Spur”. Classification of spur is based on two things i.e. reference spur and fractional spur. Fractional spur contributes significantly for fractional PLL while on the other hand, reference spur is functional for integer PLL. During lock state of PLL, PFD are fundamentally equal provided that there must be lack of error output from the PFD. Although, it can generate issues if the PFD originates through locked state in a way that the ongoing pulses corresponding to CP is subjected to have a very small width as demonstrated in the Figure 3. Input control voltage factor of the VCO is also regulated and therefore generates “Reference Spur”.

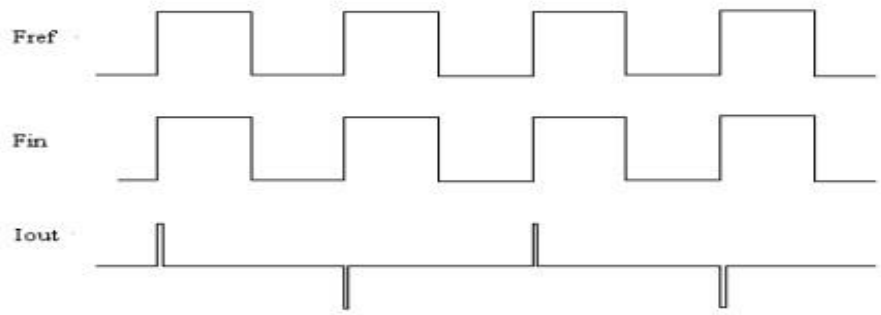


Figure 3. Output current pulses from charge pump in the lock state [8].

### 2.5.4 Charge Pump Leakage Current

There are two factors. Firstly, when there is no flow of current and CP output from the synthesizer is scheduled with the high resistance state. Secondly, when current circulates in the circuit in practical terms. In both mentioned cases, it is known as “charge pump leakage current”.

## 3 PLL Types

PLL have many associated types. Few of the known terms are analog phase locked loop (APLL) also referred to as a linear phase-locked loop (LPLL), digital phase locked loop (DPLL), all digital phase-locked loop (ADPLL), and software phase-locked loop (SPLL) [2].

### 3.1 Analog Phase-Locked Loop (APLL).

The APLL is first given the signal to lock on to, called the reference signal, then a DC voltage is manually tuned to set the VCO to nearly the right frequency. When the frequency of the output is close to the input, the startup circuit will disconnect the user-supplied DC voltage and connect the output to the VCO. A pin is provided for a reset voltage. If the oscillator’s tuning voltage goes below this voltage, the chip will be placed back into startup conditions. In simulation with parasitic, the APLL worked from average 4 MHz to 10 MHz it operates with three voltage rails: -2.5 v, 0 v, and +2.5 v [3]. The Block diagram of the Analog phase-locked loop is depicted in figure 4.

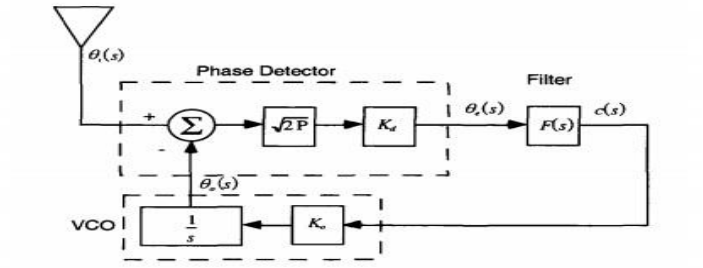


Figure 4. Block diagram of the Analog phase-locked loop.

## 3.2 Linear Phase-Locked Loop (LPLL).

It has the same basic as the PLL but the only difference is the Phase detector it uses analog multiplier instead of the mixer as shown in figure 5.

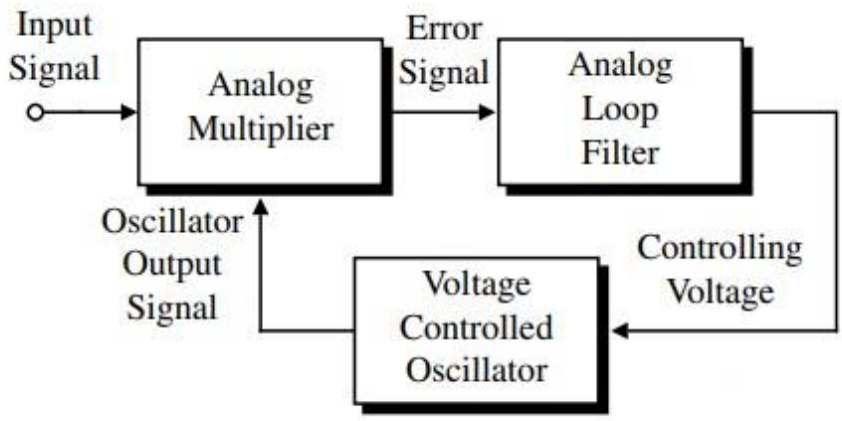


Figure 5. LPLL Block diagram.

The LPLL is comprised of four integral stability regions. These regions are described as specific deviations within frequency from the passive frequency of the VCO. Reference frequency transition with respect to their speed is shown in figure 6.

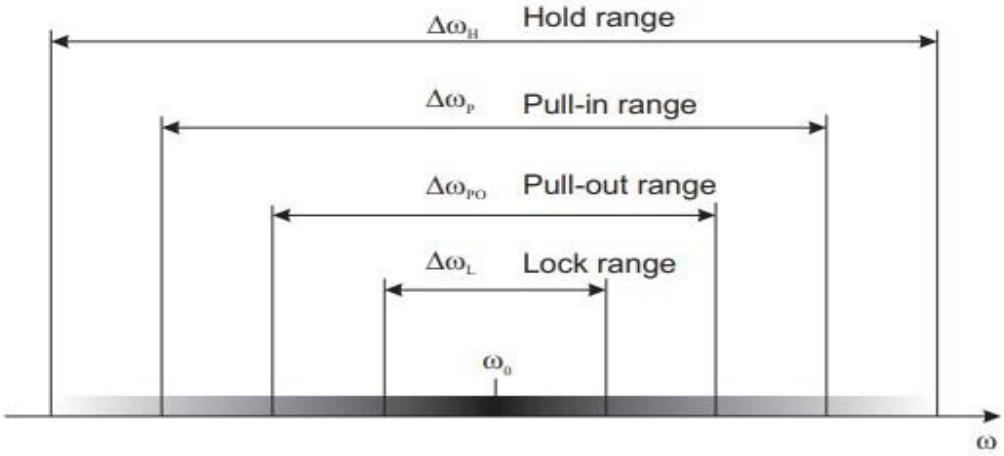


Figure 6. The various ranges of interest for a linear PLL [11].

1. $\Delta\omega H$ is the hold range from where the PLL maintains phase tracking statically. If the reference frequency diverges from the expected passive frequency then LPLL will be shifted to unlock resultantly phase error will turn into infinity state. This character is independent of the frequency speed change.

2. $\Delta\omega\rho$ is pull-in range within which an LPLL is set to lock if unlocked. This range would be infinite provided the correct filter is utilized.

3. $\Delta\omega\rho o$ is the pull-out range: This range stands for dynamic limit for secure operation of a PLL. When tracking is dropped within specified range, an LPLL usually revert to lock again. It is a slow process if related to pull-in operation. It also describes the extent of a frequency step that can be taken by LPLL without unlocking.

4. $\Delta\omega L$ is the lock range which is frequency range within which a PLL locks inside a single-beat note among output frequency and reference frequency. This character is independent of the speed during the phase change provided the case it should not go beyond the range.

### 3.3 Digital Phase-Locked Loop (DPLL).

Digital PLLs are classification of PLL that is used for synchronizing digital signals. Input and Output is set to be digital in DPLLs that indicates they possesses internal functions highly based on analog signals. DPLL is comprised of four integral elements i.e.

- Phase Detector
- Loop Filter
- Voltage Controlled Oscillator (VCO)
- Divider

The divider is designed to perform for the output signal with a frequency of the phase expected output. This component is missing in DPLLs that are specifically invented to possess an input frequency similar to the output frequency.

Figure 7 illustrates signal flow through various components.

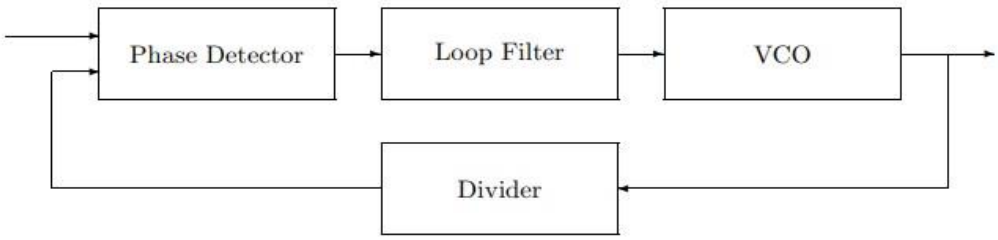


Figure 7. DPLL Block Diagram.

### 3.4 All Digital Phase-Locked Loop (ADPLL).

ADPLL is comprised of various components that relies in a digital format. ADPLL components are analogous with respect to analog PLL. Mainly, the phase detector set to be substitute by time to digital convertor or digital phase frequency detector. Concurrently, phase error is related to digital representation. In some cases, digital filter is utilized rather then analog filter provided the frequency control through a control word. The voltage-controlled oscillator (VCO) is substituted by digitally controlled oscillator (DCO) [4]. Figure 8 depicts General block diagram of ADPLL.

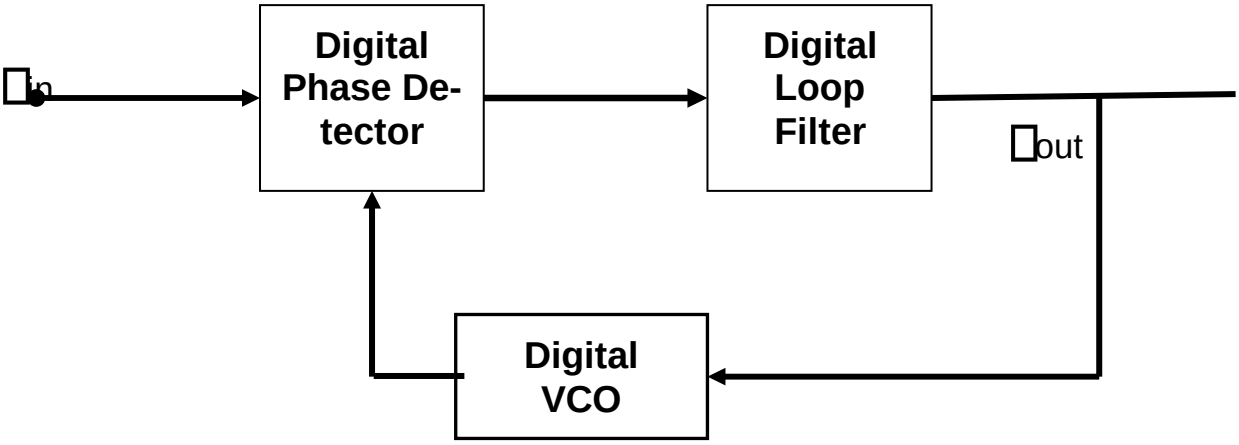


Figure 8. All digital phase locked loop block diagram.

### 3.5 Software phase-locked loop (SPLL).

A software PLL can be describe as a developed software in which the blocks are established with respect to software instead of actual hardware.

## 4 Uses of PLL

The demand of the PLL has witnessed significant rise due to its broader applications in the scope of electronics, instrumentation and transmission. The modern applications related to the PLL circuits i.e. microprocessors, memories, RF, hard disk drive electronics, and wireless transceivers, clock recovery circuits on microcontroller boards and optical fiber receivers. Below mentioned are PLL applications as follows.

### 4.1 Frequency Synthesizer

A *frequency synthesizer* permits the designer to produce wide variety of output frequencies in terms of multiples of a single corresponding reference frequency. The primary application is related to generating local oscillator (LO) signals for the high and low conversions of RF signals.

The synthesizer is functional corresponding to phase-locked loop (PLL). A phase/frequency detector (PFD) usually compares a provided frequency with a divided-down type of the reference frequency also shown in Figure 1. The PFD's output relevant signals are subjected to filtration and integration of generated voltage. These voltage operates an external voltage-controlled oscillator (VCO) to enhance or drop the output frequency in order to drive the PFD's mean output in relation to zero.

## 4.2 Clock Generation

Plenty of electronic systems comprised of processors with different types that are operational at hundreds of megahertz. Conventionally, the incorporated clocks came from these processors and from clock generator PLLs. In order to multiply a lesser-frequency reference clock (usually 50 or 100 MHz) ranging from operating frequency of the processor. The multiplication factor can be analyzed as considerably large in cases where the operational frequency is multiple GHz along with reference crystal being at just tens or hundreds of megahertz [11].

## 4.3 Skew Reduction

Skew Reduction is significant and advanced use of PLL. This factor assist in synchronous pair of data along with clock lines that enters through a large digital chip. It usually drives a considerable number of transistors, that's why it is better incorporated to the large buffer. Furthermore, the distribution on chip can also suffer from substantial skew corresponding to data.

## 4.4 Carrier Recovery (Clock Recovery)

Few of the data streams, particularly high-speed continuous data streams i.e. raw stream of data along with magnetic head of a disk drive are designated without an assisted clock. The receiver is set to produce a clock from an average frequency reference. When Phase aligns for transformation in the data stream with a PLL, this flow is mentioned as clock recovery frequency reference, and

then phase-aligns to the transitions in the data stream with a PLL. This process is referred to as clock recovery.

### 4.5 Jitter and Noise Reduction

The beneficial aspect related to all PLLs is their ability to bring clock edges forward into the close proximity. The associated average difference in relation with time among the stages of the two respective signals during which PLL has attained lock is known as the static phase offset. The discrepancy present between these phases is designated as tracking jitter. In majority of the cases, it shall be zero, and on the other hand tracking jitter shall be low and easily achievable [11].

## 5 Building Blocks of a PLL

This chapter explains the types of each component of the PLL circuit and how it was built.

### 5.1 Mixer (Phase Detector)

Functionality of a PLL relies within the phase difference of respective two signals, the first signal is the reference signal with frequency $Fmin$ which come from the signal generator and the second one is the feedback $Fout$ and it come from the VCO. An error voltage that is directly proportional with the variance between phases of the two signals is initiated by the phase detector. This respective error generated voltage can effectively utilized to synchronize the related frequency of the PLL. Appropriately given two signals is subjected to be closely related to each other. The occurrences of phase variation among signals is supposed to be null or negligible. Furthermore, the charge pump controls from respective loop filter and it is dependent on the condition of the signal that is been fed by the connected PFD. While considering the signals that are generated by the PFD are of two types i.e. high and low signals. The condition of these signals relies on the phase (leading/lagging) for the associated feedback signal. The operation of VCO are set for higher frequency if the condition of control signal is ‘up’

and contra wise. The charge pump operates the current for the loop filter in case if it gets an ‘up’ signal. Otherwise, it withdraws the current through loop filter if it gets a ‘down’ signal [1].

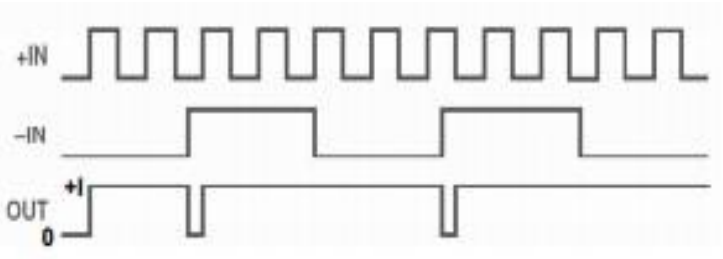


Figure 9. CP Out of the case of frequency lock and phase lock [5].

Figure 9, illustrates the system when it is out of lock and the provided frequency at -IN is below the frequency at +IN. The expected output of CP is usually at the high state more often. The initial rising side on +IN forms it as high state of output until the first rising side on -IN depicts. In other words, output is considered as the input of the VCO that constructs the frequency higher at -IN. When the frequency on -IN is bit higher in comparison with the frequency on +IN, then output associated with CP would be in the low state for most of its time. This also makes VCO input lower and frequency at - IN should be in close proximity with +IN in order to make the locked condition possible.

## 5.2 Loop Filter

Based on the succeeded filter of MyoungJun Kwak [10] thesis which was the single-pole single-zero active loop filter. And it is because it does not have a spurious signal. It is composite of an op-amp, capacitor and three resistors. Figure 10 depicts Electrical schematic in detail.

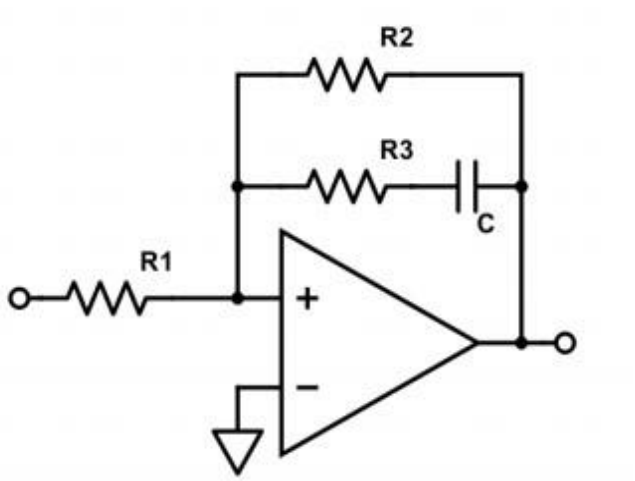


Figure 10. Schematic of single-pole single-zero active loop filter.

The transfer function associated with loop filter is identify as an equation 1 and 2 [6].

$$F(s) = -K_a \frac{1+s\tau_2}{1+(\tau 1+\tau 2)} \quad (1)$$

$$\tau_1 = R_2 C \rightarrow \tau_2 = R_3 C \rightarrow K_a = R_2/R_1 \quad (2)$$

When DC polarity of a mixer is negative then it indicates that the mixer is going to generate negative current. Secondly, positive signal current is needed to operate VCO in terms of turning buffer which is executed for passive loop filter. Moreover, active loop filter are not designed to use a polarity inversion due to the transfer function of equation 1 that possesses negative polarity. As per Table 1 description, VCO produces 1GHz frequency with an input voltage locality of 6.62V. Although, there are restrictions for DC current that mixer is capable of generating per given time. Conventionally, It is incapable of generating a DC voltage equals to 6.62V. Due to this factor, bias voltage of VCO is subjected to be set by additional level shifter. This can also be attained with the help of potentiometer and with DC voltage.

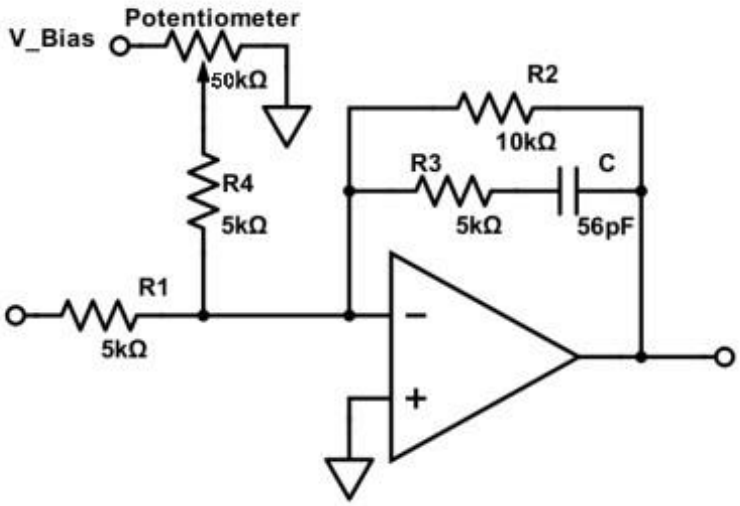


Figure 11. Active loop filter set with resistance and capacitance value.

Figure 11 shows a given set of active loop filter along with level shifter. As discussed earlier, the active loop filter and inverting buffer are not needed, because the loop filter is capable of polarity inversion itself. Although, the negative voltage is needed for its application, but resistance of potentiometer i.e. R1, R4 values needed to be the same due to the fact that set act like a voltage summer.

## 5.3 VCO

VCO considered as the key of PLL circuit. The VCO converts a voltage to frequency so, basically electronic circuit can generates the frequency signal in relation to required input voltage. While considering the fact that it keeps on changing in the course of same sense, it starts raising the frequency in relation to increased voltage. When a change occurs, few cases act normal in response to a result of false resonances. It can also result in the loop to make it unstable.

The output of the VCO is of two kinds i.e. a sine waved signal and squared wave signal. It is dependent upon the requirements of the relation that exist within applied voltage

and output signal. Usually, elongated voltage input moves towards the VCO to increase the frequency output that results in overall frequency increase as illustrated in figure 12.

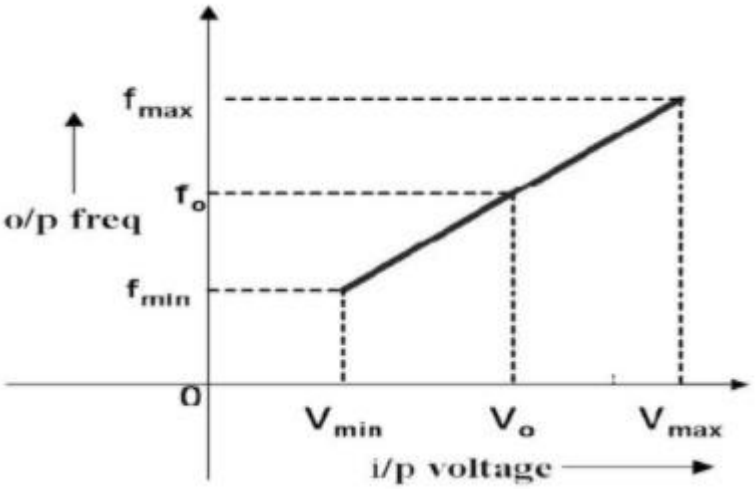


Figure 12. Transfer Function of VCO [7].

The output frequency of the VCO can be formulize as:

$$\omega_{out} = \omega_O + K_{VCO}.V_{invco}\ {}^{rad}/_{sec} \quad (3)$$

Where

$V_{invco}$ is set as input voltage to the VCO, $\omega_o$, and it considered as free running frequency, KVCO is the added by the VCO and is given by

$$K_{VCO} = 2_{\pi}.\frac{f_{\max - f_{min}}}{V_{\max - V_{min}}}\ rad\ /sec - volt \quad (4)$$

Table 1. Performance Data & Curves of the VCO.

| V TUNE | TUNE SENS (MHz/V) | FREQUENCY (MHz) | | | POWER OUTPUT (dBm) | | |
|---|---|---|---|---|---|---|---|
| | | -55°C | +25°C | +85°C | -55°C | +25°C | +85°C |
| 0.00 | 45.63 | 723.0 | 713.8 | 705.4 | 8.96 | 8.81 | 8.08 |
| 2.00 | 43.09 | 812.3 | 800.8 | 792.7 | 9.21 | 9.30 | 9.10 |
| 3.00 | 42.43 | 856.0 | 843.9 | 835.2 | 9.19 | 9.07 | 8.69 |
| 4.00 | 43.76 | 898.4 | 886.4 | 878.4 | 8.80 | 8.69 | 8.43 |
| 5.00 | 45.80 | 940.7 | 930.1 | 922.8 | 8.41 | 8.22 | 7.96 |
| 6.00 | 46.34 | 985.3 | 975.9 | 968.9 | 8.11 | 7.58 | 7.20 |
| 7.00 | 49.78 | 1030.8 | 1022.3 | 1015.7 | 7.26 | 6.86 | 6.71 |
| 8.00 | 50.19 | 1080.1 | 1072.0 | 1065.4 | 6.59 | 6.24 | 6.11 |
| 9.00 | 50.44 | 1130.8 | 1122.2 | 1115.2 | 5.89 | 5.75 | 5.67 |
| 10.00 | 47.77 | 1182.0 | 1172.7 | 1165.1 | 5.63 | 5.56 | 5.52 |
| 11.00 | 43.92 | 1230.1 | 1220.4 | 1212.2 | 5.99 | 5.90 | 5.72 |
| 12.00 | 42.22 | 1275.5 | 1264.4 | 1255.3 | 5.92 | 5.96 | 5.96 |
| 13.00 | 35.20 | 1317.4 | 1306.6 | 1297.3 | 6.43 | 6.40 | 6.18 |
| 14.00 | 34.91 | 1352.7 | 1341.8 | 1332.9 | 6.34 | 6.72 | 6.65 |
| 15.00 | 28.75 | 1388.6 | 1376.7 | 1367.1 | 6.61 | 6.65 | 6.50 |
| 16.00 | 26.07 | 1416.4 | 1405.4 | 1397.3 | 6.72 | 7.02 | 6.88 |
| 17.00 | 24.56 | 1443.1 | 1431.5 | 1422.7 | 6.47 | 6.86 | 6.82 |
| 18.00 | 21.19 | 1468.6 | 1456.1 | 1446.8 | 6.43 | 6.65 | 6.58 |
| 19.00 | 17.96 | 1489.8 | 1477.3 | 1468.5 | 6.54 | 6.62 | 6.45 |
| 20.00 | 17.26 | 1508.0 | 1495.2 | 1486.6 | 6.17 | 6.38 | 6.25 |

The aim is 1GHz output so according to the table 1 the VCO needs 6.62V input to generate the require frequency. And Vtune can change it by using the variable resistor in the loop filter.

Results show that JTOS-1300+VCO possesses linear tuning sensitivity. To describe tuning sensitivity at a given point, it synchronizes with the datasheet and will be identical. The critical aspect about tuning sensitivity vicinity of 1GHz is important due to its pattern and tuning voltage with all 10MHz VCO frequency points ranging from 900MHz to 1100MHz. It is also calculated to show accuracy in tuning sensitivity throughout 1000MHz. The results are shown in table 2

Table 2. JTOS-1300+VCO Tuning sensitivity table from 900MHz to 1100MHz.

| Frequency [MHz] | Tuning Voltage [V] |
|---|---|
| 900 | 4.8 |
| 910 | 4.87 |
| 920 | 4.93 |
| 930 | 5.0 |
| 940 | 5.6 |
| 950 | 5.74 |
| 960 | 5.86 |
| 970 | 6.00 |
| 980 | 6.10 |
| 990 | 6.24 |
| 1000 | 6.62 |
| 1010 | 6.72 |
| 1020 | 6.99 |
| 1030 | 7.07 |
| 1040 | 7.2 |
| 1050 | 7.32 |
| 1060 | 7.5 |
| 1070 | 8.0 |
| 1080 | 8.30 |
| 1090 | 8.61 |
| 1100 | 8.90 |

The results above are shown as a linear graph in figure 13. The figure shows that the frequency is escalating same as figure 12.

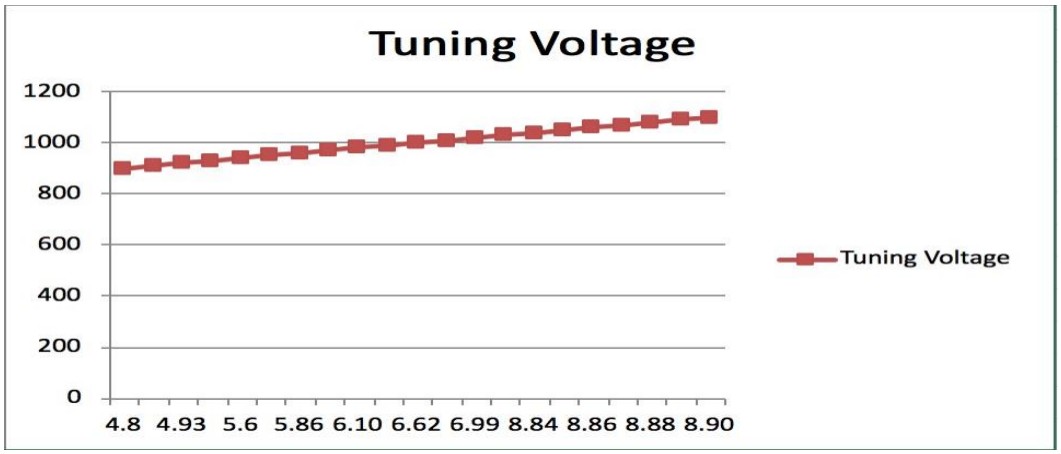


Figure 13. Tuning voltage in line graph.

## 5.4 Prescaler

Type: MC12080, 1.1 GHz Prescaler.

A prescaler can be defined as an electronic counter circuit that utilizes by reducing the frequency through performing an integer division N for the input frequency for high frequency signals towards lower signals. To be more precise, prescaler is an integrated frequency divider circuit.

$$F_{out} = \frac{Fin}{N}, \text{ where ‘‘N’’ is an integer.} \quad (5)$$

The MC12080 is a single modulus divide by 10, 20, 40 and 80 prescaler for low power frequency division of a 1.1 GHz high frequency input signal. And the frequency division factors are controlled by three switches SW1, SW2 and SW3 to select the required divide ratio of ÷10, ÷20, ÷40, or ÷80.

Table 3. Control signal states and their related division factors taken from MC12080 1.1 GHz prescaler datasheet.

| SW1 | SW2 | SW3 | Divide Ratio |
|---|---|---|---|
| L | L | L | 80 |
| L | L | H | 40 |
| L | H | L | 40 |
| L | H | H | 20 |
| H | L | L | 40 |
| H | L | H | 20 |
| H | H | L | 20 |
| H | H | H | 10 |

**Table Key:** H stands for high
L stands for low the control signals
Low signals are usually high if they are attached to 5V. On the other hand, they are low if they are associated to GND.

## 6 Operating Principle of a PLL

A reference frequency also abbreviated as Fref is implemented on the PLL. This factor creates plenty of error voltage and can effect the voltage-controlled oscillator. This kind of frequency and its output signal are meant to have many variations, because the error voltage keeps on changing. The given voltage-controlled oscillator is reverted again to the PLL partially. It moves from the prescaler circuit and acts like a second input taken from the error detector. When error detector gives an error voltage that is equivalent to the differentiation of the two signals. i.e. reference signal and the feedback signal then both can have equal frequency with respect to PLL. It is also perceived to be locked.

- The feedback and reference signal retains identical frequencies with minor phase difference.

- The error voltage produced through the error detector is set to be constant. Two input signals differences are given be error detector i.e. zero.

When the loop is locked, PLL automatically modify itself in order to deal with change related to input frequency $F_{ref}$ within lock range. When input $F_{ref}$ is increasing or decreasing slightly, error detector orderly produces an error voltage corresponding to the scenarios. This error is given to the loop filter. Resultantly, the loop filter keeps on changing and the tuning voltage related to the VCO also starts changing the respective VCO output frequency. During these changes, the feedback frequency also shows significant transitions. The feedback frequency modifications retains the loop locked until the applied frequency comes within the lock range specified by PLL.

As per formula, if $F_{ref}$ is abbreviated as applied reference frequency and $F_{out}$ is set as frequency of output signal generated by VCO and N is declared as the frequency division factor of the prescaler, we can write the frequency of both input signals at the error detector is $F_{ref}$ and $F_{out}/N$.

If e(s) is the error voltage, then,

$$e(s) = F_{ref} - \frac{Fout}{N} \quad (6)$$

When the PLL is locked, e(s) = 0 [1].

$$F_{ref} - \frac{Fout}{N} = 0 \quad (7)$$

$$F_{ref} = \frac{Fout}{N} \quad (8)$$

$$F_{out} = N \times F_{ref} \quad (9)$$

## 7 Design and Measurement

To achieve this PLL circuit, initially a schematic along with its corresponding layout is created through Pads which is a design software and mainly helps in electronic circuit design. Pads is assists with handy tools for designing schematics and incorporating them with PCB layout design. The schematic for PLL circuit is illustrated in figure 14.

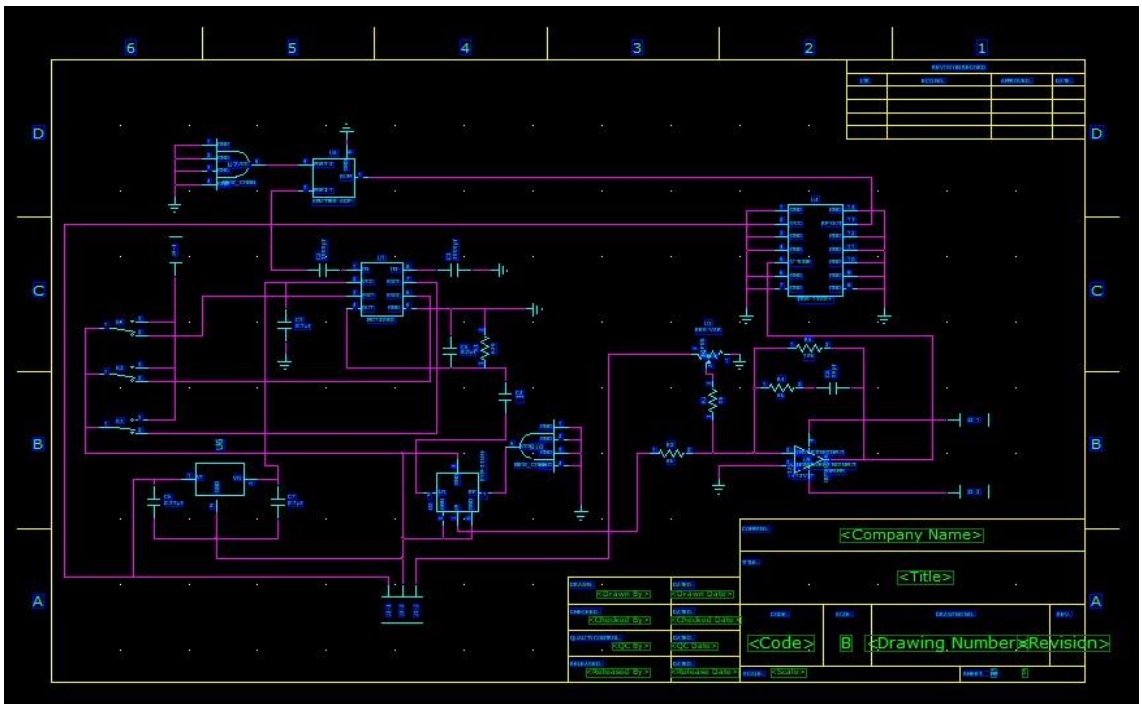


Figure 14. Schematic for PLL circuit.

Starting this schematic by putting first the prescaler, pin No.1 connected to the port 1 of power splitter, pin No.2 is the input 5V and to get exactly 5V input adding a regulator LM7805 with 2 CAPS and connected to it, pin No.3, 6 and 7 they are connected to 3 switches (three terminal switch) the switch is connected to 5v and ground they work as high and low. The output of the prescaler is connected to 1000pf cap and continue to the LO of the mixer, the RF connected to the connector for the reference frequency and IF connected to the Filter and it is going to the input of the VCO and the output connected to the sum of the power splitter, and port 2 connected to the connector. In addition, after the filter has been checked in Multisim to see if the variable resistor work and affect in the output voltage of the loop, it works perfectly and it was changing the output voltage for the same values that need to make the VCO generate 1GHz output frequency.

After finishing all the schematic and checking all the parts, then the next step is doing the layout as shown in figure 15. As shown in figure 16 first try was to make the board small as possible but the milling machine was not that much accurate it makes some mistakes in connections. Like 2 wires are touching each other or the copper around the hole was not in the middle, so the board needed to be expanded and making some extra space between all components and wires as shown in figure 15.

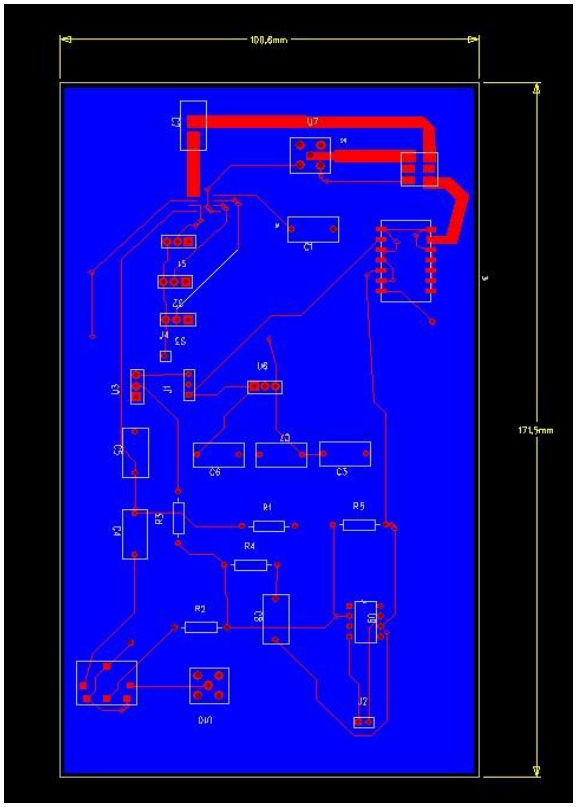


Figure 15. PCB layout for the Final PLL circuit.

The size of the smallest board is 5.7 cm x 7.5 cm and figure 16 shows how much it was small and all the components are close to each other's without any free space and using both top and bottom layers to make the connections.

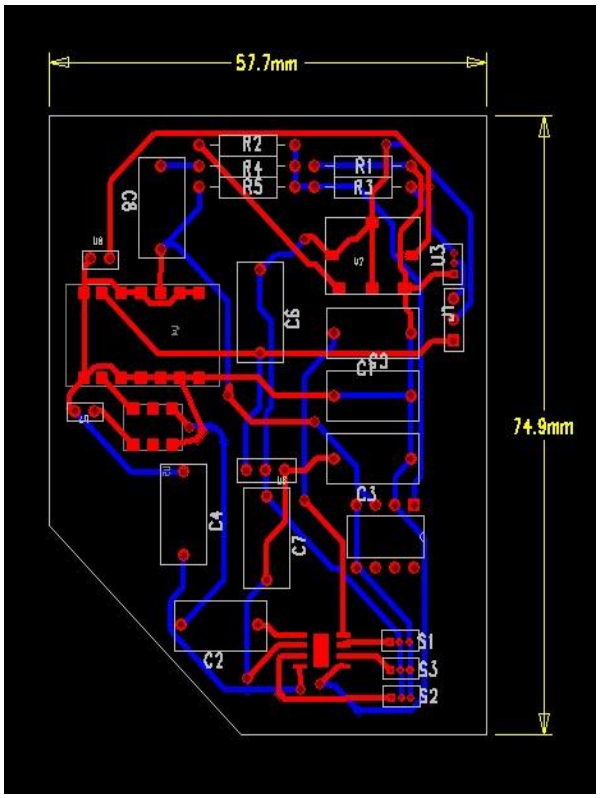


Figure 16. PCB layout for the smallest size of PLL circuit.

The size of the final board figure 15 is 17.15 cm x 10.06 cm.

For the layout all the bottom layer has to be made as ground plane as well to connect all the ground pins to the ground plane directly without putting and ground connections in the bottom Layer. Placing the VCO, prescaler, power splitter and connector all together up on top of the board, and the rest are down. Also, all 1GHz wires that come from the VCO and go to the power splitter, connector and prescaler their width was calculated in the website [12] and all calculations are shown in Figure 17 below.

On this website https://www.emtalk.com/mscalc.php the data were entered are.

| | |
|---|---|
| Dielectric constant = | 4.2 |
| Dielectric high = | 1.5mm |
| Frequency = | 1GH |
| Zo = | 50Ω |
| Elec. Length = | 90° |

After all data were entered, the website shows the width and length of the wire but here only the width is needed, and it is 2.92mm.

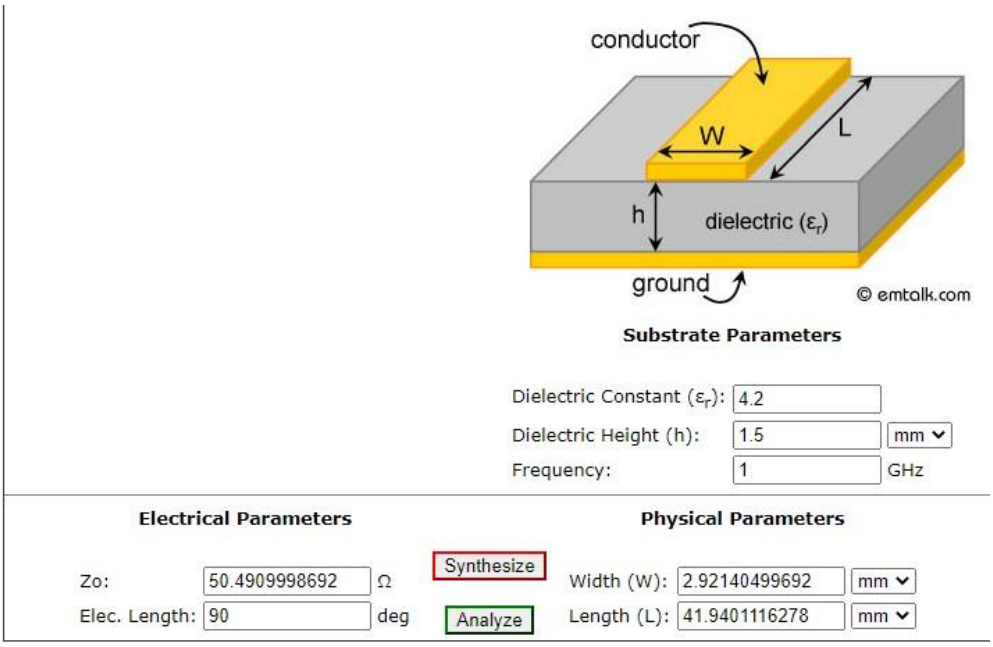


Figure 17. The result of the 1GHz wires width.

For the pin number two in the prescaler which go to the regulator it is not connected well in the layout because there was no possible way to make or to find a route for it. So due to that it has needed to be done separated, there after printing the board. So pin number two was completed manually using a thin wire and soldering it to both sides. Here is the final board after printing and soldering all the components on it as shown on figure 18.

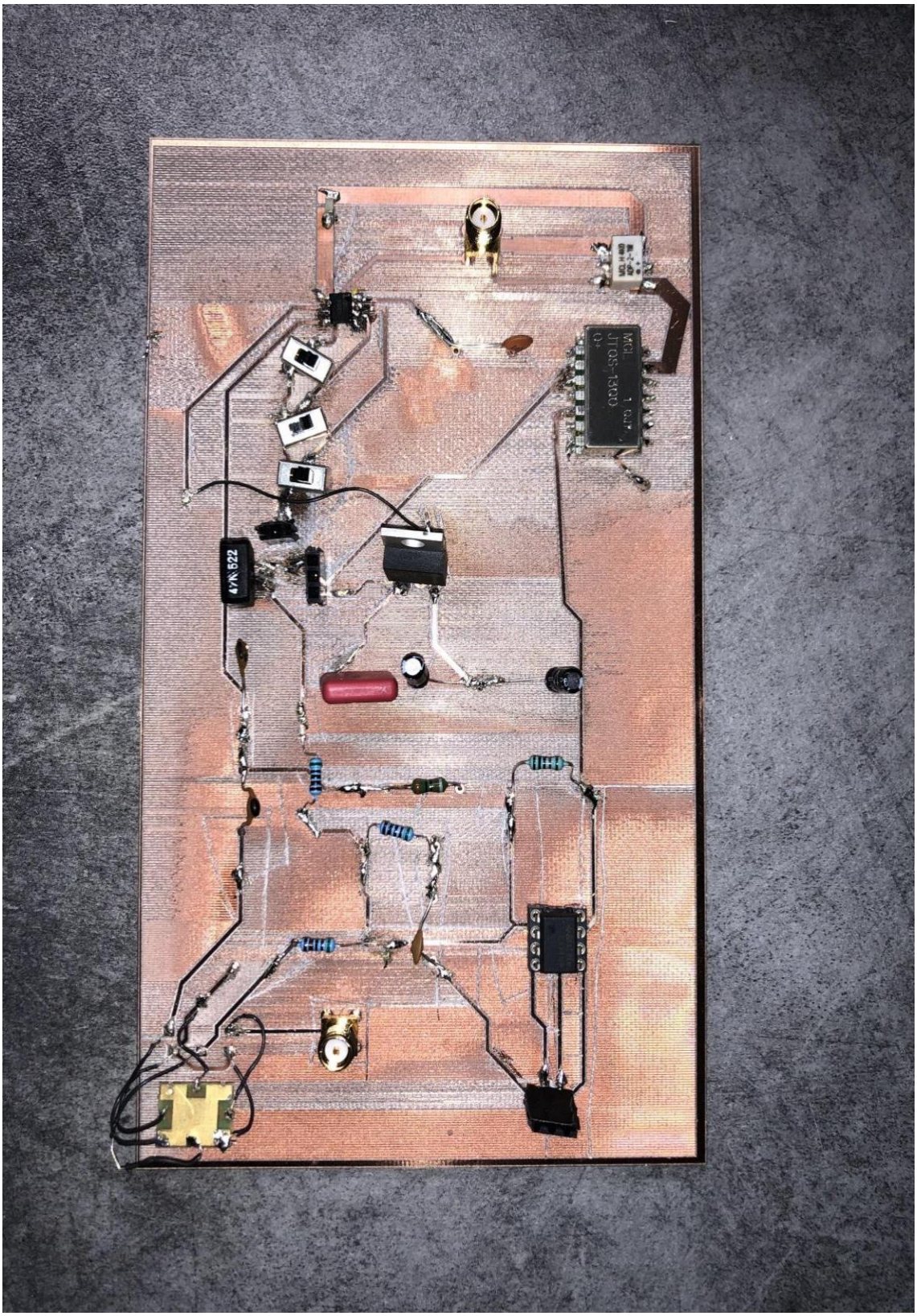


Figure 18. Final PCB board.

Here is the bottom layer that shown in figure 19, there is no connections on it and only the ground pins of the top components are solid with it.

Figure 19. Bottom layer of the final PCB board.

## 7.1 Two Additional Tasks

And here is the two tasks that are additional to my work because the circuit did not work due to problem with one component, the tasks are:

1) Design two circuits on PCB: a) one with everything else except the prescaler. b) Another one with everything else except the prescaler and the loop filter.
2) Use surface mount components whenever possible for all circuits, have the ground plane below the PCB everywhere unless extremely necessary. Make the PCB much smaller in order to minimize the lengths of the lines to minimize the coupling / overhearing.

So, starting with the first board the prescaler, regulator and the three switches were removed. The final schematic and layout design shown in figures 20 and 21.

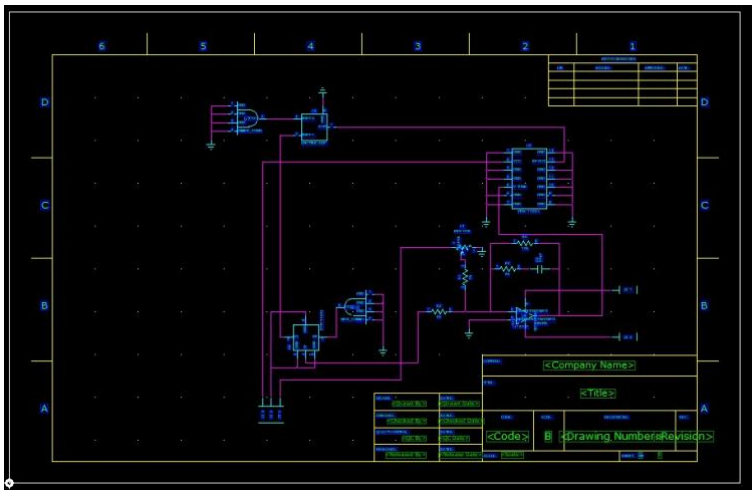


Figure 20. PLL schematic without the prescaler, regulator and switches.

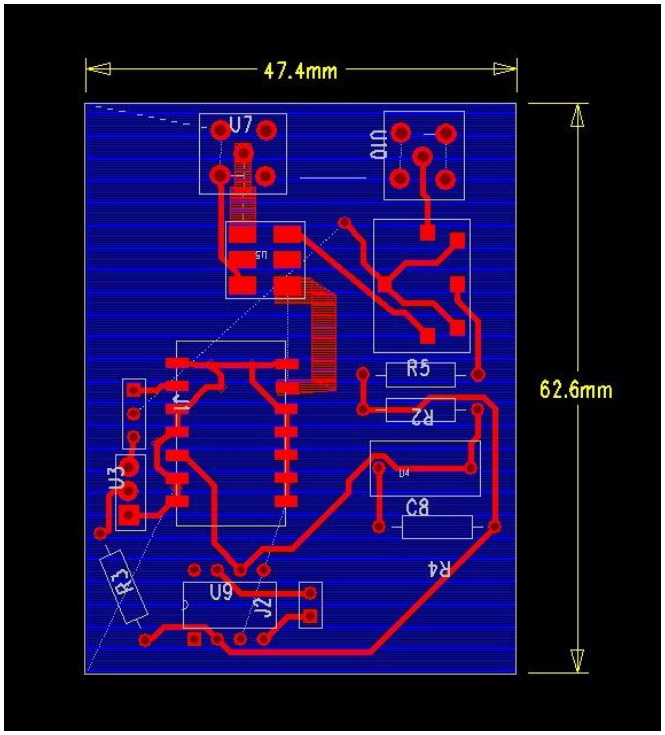


Figure 21. PLL layout without the prescaler, regulator and switches.

The second board is the same as first one but in addition the filter was removed also. The final schematic and layout design shown in figures 22 and 23.

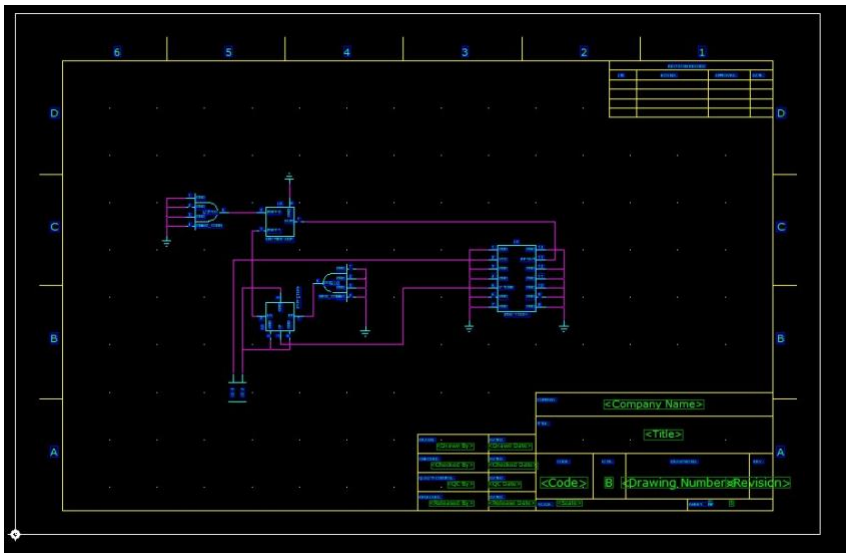


Figure 22. PLL schematic without the prescaler and loop filter.

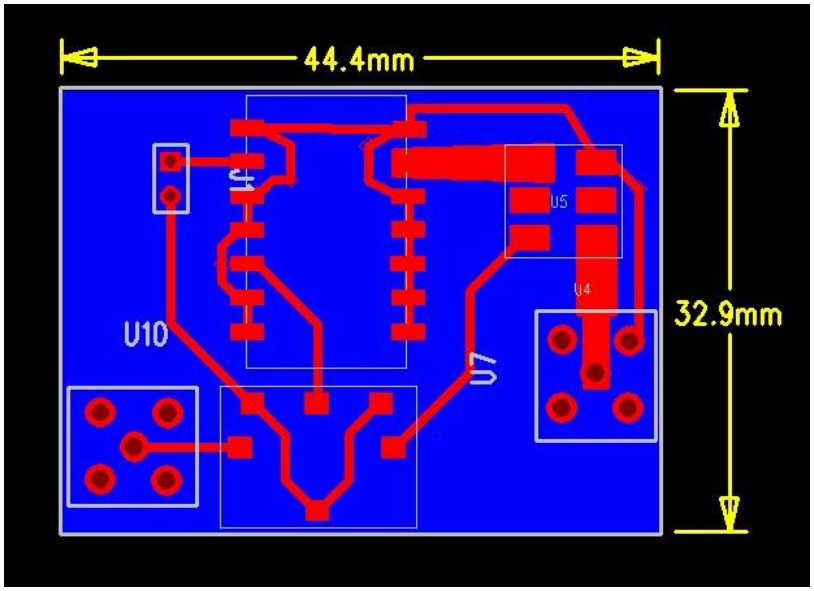


Figure 23. PLL layout without the prescaler and loop filter.

# 8 Discussion and Conclusion

In this thesis, the whole PLL system and their components are discussed, analyzed, and measured. The whole theoretical part of the system is discussed, and each component is studied and analyzed.
The goal to achieve a locked state of the PLL system was not attained successfully. After checking and testing the board the results shows that the only thing that not working is the prescaler because the output of it was giving wrong signals to the mixer. Also when changing the division factors they were not affecting in the output so there are only two possible options for this problem:

1) The prescaler not working probably
2) The reference oscillator is somehow connected / overheard in the prescaler output. It can be only one of the problems or both.
In my opinion, the only problem is only the first option because everything was connected perfectly and checked but this prescaler was ordered from Alibaba.com because it is was not available in Finland or Minicircuit website that time and it might be not working, or it's stopped working during the testing. Because many times during the previous classes in the laboratory the components purchased from china they stop working or burned during the work.
The loop filter and VCO are working well, the loop's output voltage that goes to the VCO it can be increased/decreased by using the potentiometer in the loop filter, and for this work the required frequency is 1GHz so the VCO need only 6.62Vinput. Mixer is also working well with the reference signals and the connections are good around it, the regulator gives 5V input to the prescaler, switches working well they give L/H, power divider is also 100% working.
So only changing the prescaler will make this PLL system locked, but due to lake of time and long shipment period it is not possible to make a new order for new prescaler.

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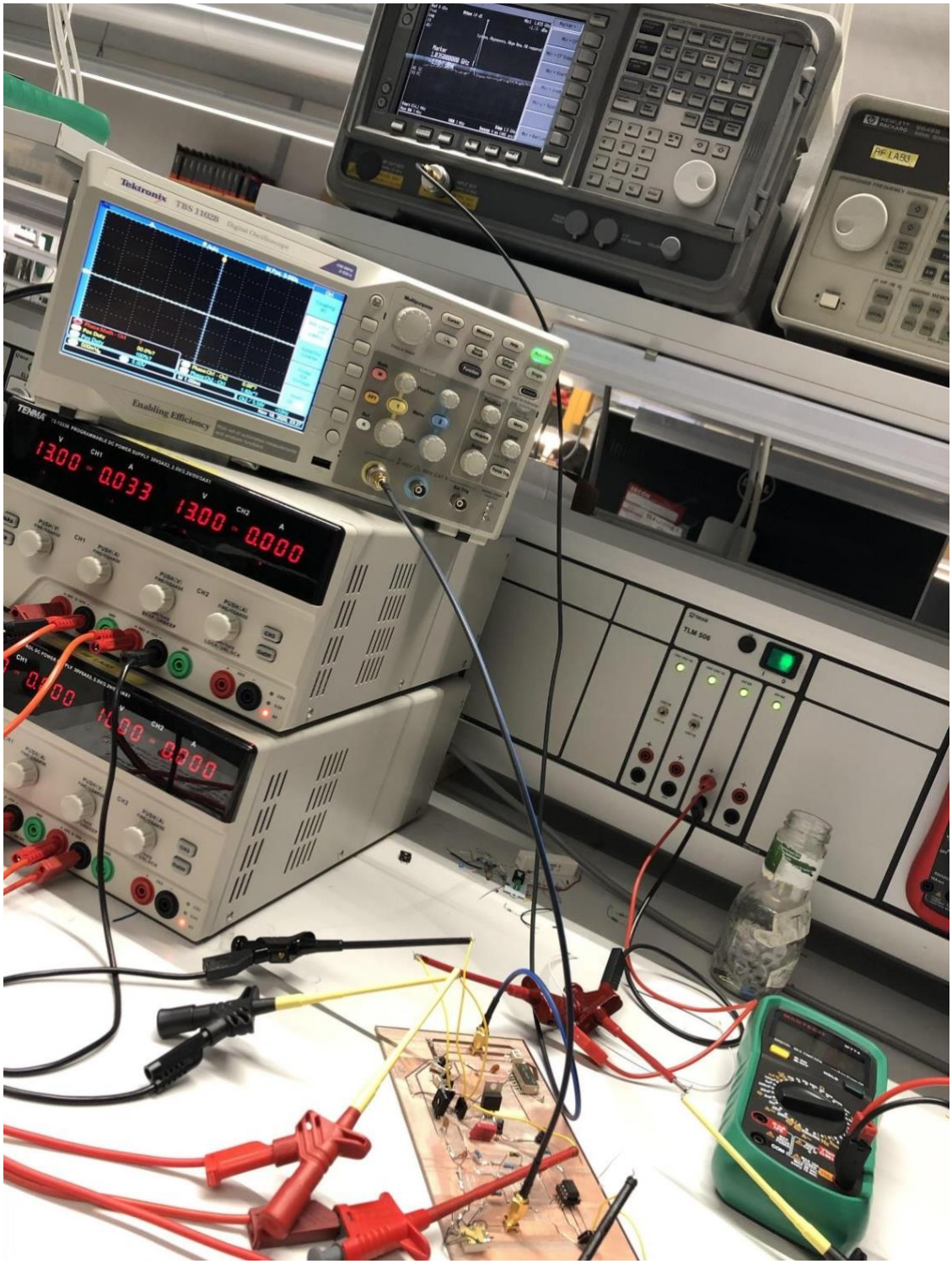


Figure 24. Measurement setup for testing PLL circuit and as you can see in the spectrum analyzer the output is 1GHz.