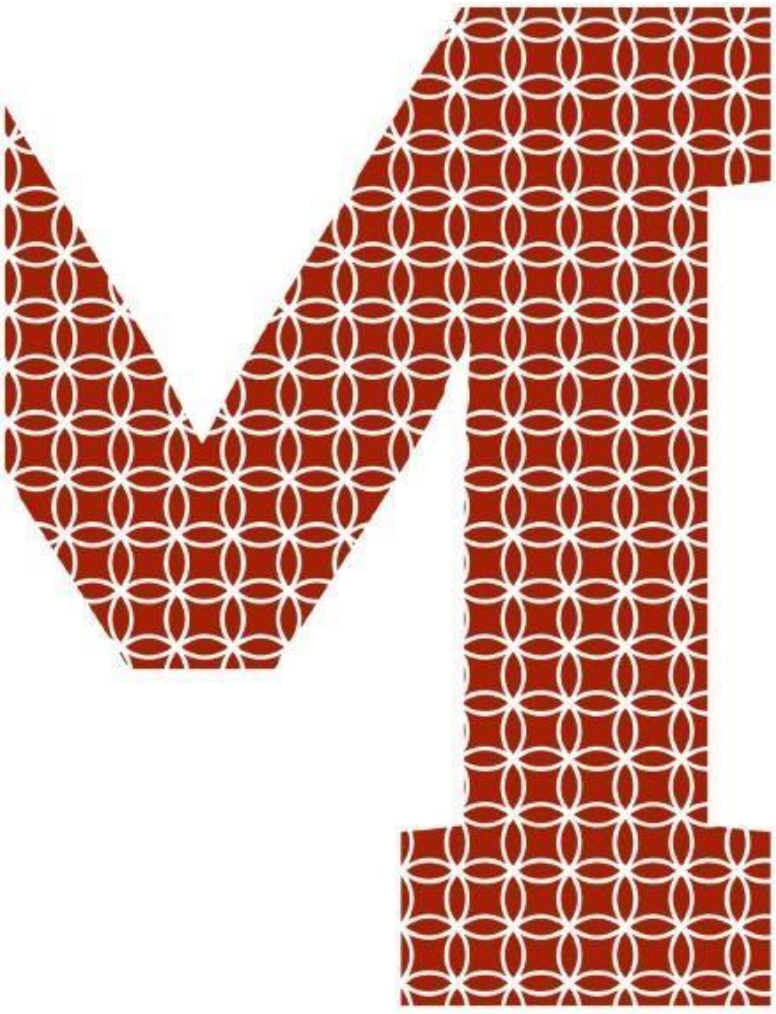

Expertise
and insight
for the future

Arjun Poudel

Review of Data Converters

Metropolia University of Applied Sciences

Bachelor of Engineering

Electronics

Bachelor's Thesis

Abstract

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The goal of this report is to review different types of electronic data converters developed till now. The report also goes through working and characteristics of those converters in brief. To support the review, a demonstration of data converter is also included.

The digital world we are now living on stands on the foundation of data converters. Almost every device we use relies on data converters which work in different environment from space to underwater. This has been possible with coherent development of digital to analog converters that helps visualize the unseen world around us or existing's in a different angle. The communication sector, embedded systems, instrumentation widely depends on the data converters. Different applications require different converters like one used inside earth environment might not be feasible for space exploration. Performance, resolution, bandwidth, quantization noise, interference, manufacturing cost are the important parameters to deal with. Different converters have different characteristics and all of them have been there to fulfill our needs.

To show the working of converters, demonstration is done using easily available components to show the whole cycle of data conversion i.e., from analog to digital signal and vice-versa. A microcontroller is used to assist signaling and work as processor to relay information to and from data converter chips. All this has been carried out in simulation software and additionally circuit board is also designed.

Finally, what we see is that devices we are surrounded with like the mobile phones, smart watches, television, washing machines and even space rovers are equipped with data converters that helps to perceive natural sensations. With this it is evident that data converter technology is a very important aspect of digital world and further development, and research will continue to improve and expand the application of data converters.

Keyword	ADC and DAC

Contents

List of Abbreviations

List of Abbreviations

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
PTM	Pulse Time Modulation
PCM	Pulse Code Modulation
ENIAC	Electronic Numerical Integrator and Computer
UNIVAC	Universal Automatic Computer
MSPS	Mega Sample per Second
KSPS	Kilo Sample per Second
IC	Integrated circuit
CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large-Scale Integration
LSB	Least Significant Bit
MSB	Most Significant Bit
TTL	Transistor Transistor Logic
R	Resistor
V	Voltage
I	Current

1 Introduction

Data converters are responsible to convert the format of signal with conservation of sufficient information. Field of signal and systems has identified two main types of signals so far analog and digital signal. Analog signal generally represents a real physical parameter like temperature, pressure, color etc., these signals are susceptible to error while processing, storing for future and transferring from one location to the other. Therefore, in microprocessor based industrial products, it is necessary to translate an analog signal into digital signal. Those systems that converts the analog domain signals to digital signals, as their operation suggest are termed as ADC (Analog to Digital Converter). On the other side, since our senses make more sense out of analog or natural signals as the complementary side of coin, there exists the necessity of conversion of digital signal to analog signals and the converting units are termed as DAC (Digital to Analog Converter).

2 Background of Data Converters

Communication, instrumentation, industrial automation, image processing, data analysis, nanotechnology and artificial intelligence are the most popular topics of this age. The essence of the physical development is saturating, and recent trend suggests that the world is moving on towards information technology and digitization. According to Moore's law, the size of integrated chips has been decreasing by double every 2 years. The whole credit goes to an extensive research, collaboration and persistent research happening around the world. Educational institutions are flowing tons of research in technology.

Looking the present situation, digitization is increasingly replacing the analog and human-based systems. Digital circuits and digital processing technology are omnipresent. Digital systems are resistant to interference, offers high stability and wide adaptivity, have now become easy to design and manufacture and versatile to changes through programming, also digital systems are less susceptible to noise, customized filters can be adopted, but also because of wide development in manufacturing, fabrication and design industry for integrated circuit technology, performance and applicability are vast. Advancement of nano technology and VLSI has increased the performance of the digital circuits, more sensitivity, faster operation, bit count, power conservation and cheapness of digital technology is increasing which is propelling the world to digitization as a compulsion to stay ahead.

Data is an essential resource today, very large volume of data is pushed out in the world every data since most people are using the digital platform for survey, work, entertainment. Most of the data is digital even if the source is continuous signal. And here come the revolutionary ideas of conversion of signals. Transducers are the facilitators that allows us to see a piece of data in different forms mostly analog and digital. Data communication and data analysis uses the most out of the conversion technology. All this digital process can only be practical when interface between digital processors and analog domain, which involves data preprocessors, data acquisition, data representation and domain converters. Therefore, Analog-to-Digital Convertor (ADC) and Digital-to-Analog Convertor (DAC) comes to fulfill the role of the interface.

2.1 History and Evolution of Data Converters

In the mid-1920s, Harry Nyquist had already been studying on telegraph signaling keeping in mind to discover the method for maximizing signaling rate that could be possible over a single channel using the similar bandwidth criterion. W. Alec Harley Reeves had studied analog-to-time conversion

techniques using PTM. While ADC got its first boost in 1930s because of its widespread use of PCM technology in telecommunication industry. Noise immunity was a major concern for telecommunication over the copper lines resulting in a revision to PCM which motivated re-invention of pulse PCM by Reeves. The ADC and DAC developed by Reeves represent one of the first allelectronic data converters on record. Those ADC and DAC use counter and similar clock source. Early electron tube coders used a binary-coded shadow mask, and large errors (sparkle codes) could occur if the beam straddled two adjacent codes and illuminated both. So, there was always need of a different method or a revolutionary idea.

ENIAC, a powerful computer of those times whose development started around 1942 was introduced later in 1946 for general use. Till those time, computers were made from vacuum tubes that could perform calculations in 10s of thousands fps (flops per seconds). The ENIAC had pioneered similar projects and laid foundation for the development of UNIVAC, the first digital computer. Transistor started to be doped with germanium and germanium transistor was invented in 1947 which is an important milestone in the field of electronics and PCM also reached to its hype. With the development of the repeater (Wrathall repeater) in 1956, PCM became capable to support more voice channels with these technological advances and existing copper cable capacity was increased without replacement. Hence, PCM proved to have a lot of possibility. Digital computer encouraged the commercial sector to invest in development of data converters too. In 1954, Epsco introduced an 11-bit, 50 KS/s vacuumtube based ADC. It is believed that this was the first commercially developed ADC.

Converters in 1950s were using old and new technologies together like vacuum tubes, diodes and transistors in a single implementation. This was an indication that adoption of new technologies has started then. The IBM-360 mainframe computer and solid-state minicomputers (such as the Digital Equipment Corporation's Programmed Data Processor series starting in 1963) got attention of public for data analytics. The military division worked in their best interest to develop weaponry using the available technology, and data converters got the military interest. Converters were big, heavy and power consuming. At those times, even 8-bit, 10-MSPS converter were as big as that they have to be mounted in racks since they used to have their own power supply unit. They dissipated power near to about 150 W. Several companies were developing discrete transistor-based circuits which helped reduce size and power consumption. At the same time scientist and engineers also were developing ADCs and DACs using the transistors. Bernard Gordon filed a patent in 1958, for the logic to perform the successive approximation algorithm (a popular analog to digital conversion method), and in the early 1970s, Advanced Micro Devices and National semiconductor introduced commercial successive approximation register logic ICs. Computer Labs, Datel, hybrid Systems, ILC/Data Device Corporation,

Micro-networks, National Semiconductor, Teledyne Philbrick, and Zeltex are major companies of those times. [1]

In 1970s, technologies like monolithic, hybrid and modular development were in peak which benefitted by improving resolution and speed efficiency of converters chips. There was phenomenal development in design and fabrication. It was 1971 when analog/digital interfacing circuits were designed using monolithic technology for the first time. Earlier monolithic DACs used bipolar process which consisted of resistors, voltage references, latches, op-amps and various compensating capacitors, and other variable components like variable resistor for trimming. In addition, separate but easily integrable component design like autonomous ADCs, DACs integrated chips and other devices became popular. Power output and speed capabilities and multi in one concept got chance to penetrate industries concern. Phillips was one of the early manufacturers of audio DACs and Analog device collected expertise worthy enough.

In 1980s, the implementation of ADC and DAC in audio and video industry got attention. And people got very affectionate with audio and video. Industries pushed their product in the market which was highly demand. The launch of 8-bit ADC in 1979 with a remarkable 30Ms/S flash challenged other manufacturers to work for similar devices. For that time, 4 to 10 bits of resolution and 500MS/S was overwhelming. The development of microprocessor triggered a revolution in digital signal processing and computing. Hybrid nodular chipsets included different devices together in a single chip which hugely changed manufacturing and made devices cheaper compared to single-chip monolithic converters in performance. By the mid-1990s, the sigma-delta architecture began to replace the parallel DACs in audio applications since they offered higher resolutions than prior DACs.

Till the date computing platform and the data conversion endeavor has increased its tremendous importance over the world which is evolving towards digital globe. The progression from early rack mounted instruments to modules, hybrids, and ultimately ICs is in pursuit. CMOS technology has reduced the power consumption and relaxed scaling of speed which has led to increase in electrical and small signal performance. A lot of features are accommodated in today's converter and various standard have been formulated by globally recognized institutions and specification are introduced. Today we have converters in range of GSPSs and resolution to more than 32-bits and compactional power is reaching the limits of Moore's law. In the past 20 years, due to deep sub-micron integrated technology becomes more popular; it promotes a new area of analog integrated circuits: mixed signal integrated circuit. Some important milestones in development of data converters are assimilated in Table 1.

Table 1: timeline of converter technology [1]

Landmarks	**Year of Introduction**
Reeves' counting ADC	1939
Successive approximation ADC	1947
Flash or parallel ADC (electron tube coder)	1948
Tracking ADC	1950
Delta modulation and differential PCM	1950
Voltage-to-frequency converter	1952
First- and second-order loops, multibit, with oversampling with noise shaping (sigma-delta, but without the digital part)	1954
Bit-per-stage ADC (binary and Gray)	1956
Sub ranging ADC	1956
Dual-slope ADC	1957
Multibit sigma-delta implementation	1961
Sigma-delta ADC (first use of the name)	1962
Folding ADC (Gray code)	1962
Sub ranging ADC with error correction (redundancy)	1964
Pipelined ADC with error correction (redundancy)	1966
Triple-slope ADC	1967
Complete sigma-delta ADC with digital filtering	1969
Generalized pipelined architecture	1971
Quad-slope ADC	1973
Continuous time sigma-delta	1976
Bandpass sigma-delta	1988

3 Data Converters

Two converters, ADC and DAC are discussed in brief with their types and features in the following sections.

3.1 Analog to Digital Converter

Any electronic device that converts a continuous time, varying amplitude to a discrete time and amplitude digital signal are analog to digital converter. Signal available from natural sources are analog in nature. Almost all signals or voices, videos, colors, heart signals, temperatures, pressure readings are analog. And there is nothing much we could do, on these analog signals.

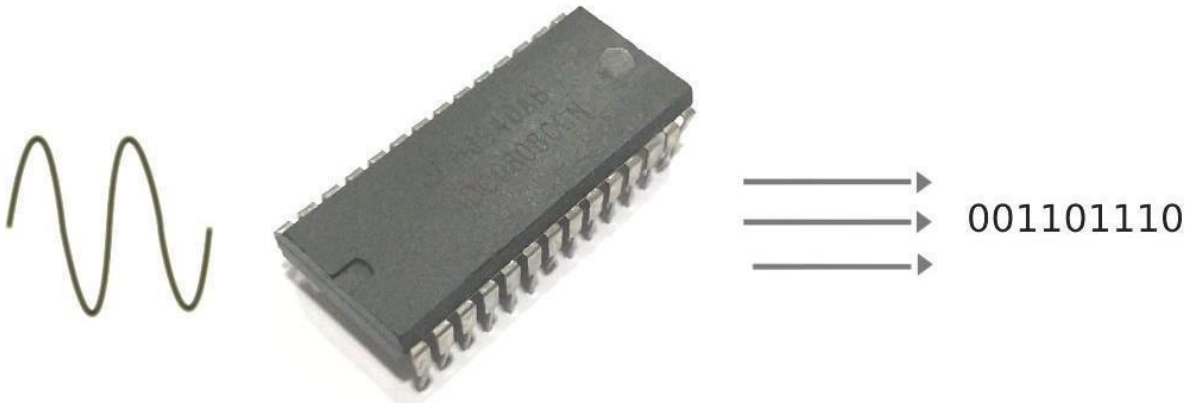

Figure 1: analog to digital converter

The conversion includes various action to be done upon the continuous signal. The signal has to pass through a series of steps, that are fundamental in every type of ADC. The conversion involves a rounding up like operation called quantization of the input, hence a small amount of error also called as noise is introduced. There is always trade of in between data volume generated after conversion upon the information useful for regeneration of the signal, which means there is a sampling process involved since discrete time value are measured and converted to discrete values. Also, there is bandwidth limitation involved to be considered.

The A/D converter is a quantizing process whereby an analog signal is represented by equivalent binary states. Basically, there are two techniques, first one involves comparison of input analog signal with discrete signals generated internally. Counter, flash type and successive approximation are some of them. Second one involves comparing these acquired parameters to known values by changing the

domain of input signal like transformation of analog signal into frequency or time. This group includes integrator converters and voltage to frequency converters.

The successive approximation and the flash type are faster but voltage to frequency converters and integrator generally are more accurate. The flash type cost more in manufacturing also there are design complexities for high accuracy. Data converters are manufactured in chips like as one ADC chip shown in Figure 1.

3.1.1 Parameters (Characteristics) of ADC

While construction, various parameters of ADC should be considered which defines the properties of it. Some important parameters are discussed below:

Resolution, the original analog signal in ADC have unlimited resolution as the signal are time continuous. Converted digital signal will collected some but enough information from the analog signal thus limiting the resolution. The resolution of an ADC is the tiny and tiny change that can be differentiated in the analog input.

$$Resolution = Full\ Scale\ Range\ (FSR)\ /\ 2n \quad (1)$$

Conversion Time, another critical parameter in A/D conversion is the conversion time. This is defined as the total time taken by the specific converter to process and convert analog signal into its digital output.

Accuracy is the comparison of actual output and the expected output. The lesser the variance the more accurate is the converter.

Linearity determines output to be the linear function of input. Every signal or the signal range should be treated the same across the converter to achieve high linearity.

Full scale output value is the maximum binary output achieved from the respective input range.

3.1.2 Phases of Conversion

These are the important fundamental steps of an analog to digital conversion. The different steps involved are as follows:

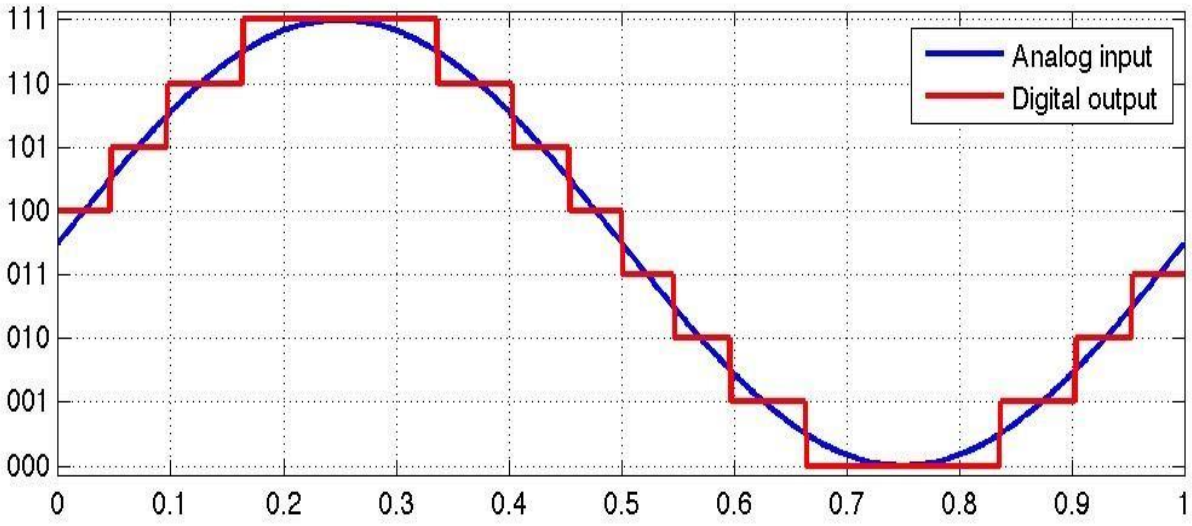

Figure 2: sampling, quantization and encoding [2]

Sampling is the first step of conversion in which the analog signal is broken into instantaneous values in a fixed or variable interval of time. The correct term to represent the sampling parameter is a sampling rate that is suitable to retain the most information content of the analog signal.

Quantization is the step of assigning the correct discrete value to the instantaneous signal that would almost represent the amplitude of the signal at the instant. Quantized levels are the voltage level, and this voltage levels are discrete that is determined by analog reference voltage and the number of bits used for the representing a state of a single analog value as digital data in the ADC.

Encoding is the final step of assigning an appropriate digital bit combination for the value set by the quantization step to represent the sampled signal most accurately in digital form. In the Figure 2, the value in the Y-axis is the encoded value i.e., 3 bits.

3.1.3 Types of ADC

Different types of ADCs have been developed for the application in various industries and products. Every single type has its own features. Most fundamental ADC technology are discussed below:

3.1.3.1 Flash Type ADC

It is known with different names like Direct ADC, Simultaneous ADC but every name indicates its different features. This is the fastest ADC that utilizes comparators that compares reference voltage with input analog voltage divided over a resistor divider network.

A priority encoder helps to select the highest value in digital form to the actual representation as shown in Figure 3. To achieve a n-bit ADC, 2n-1 comparators are needed, so this is expensive. Its conversion time is less and can even digitize video signal.

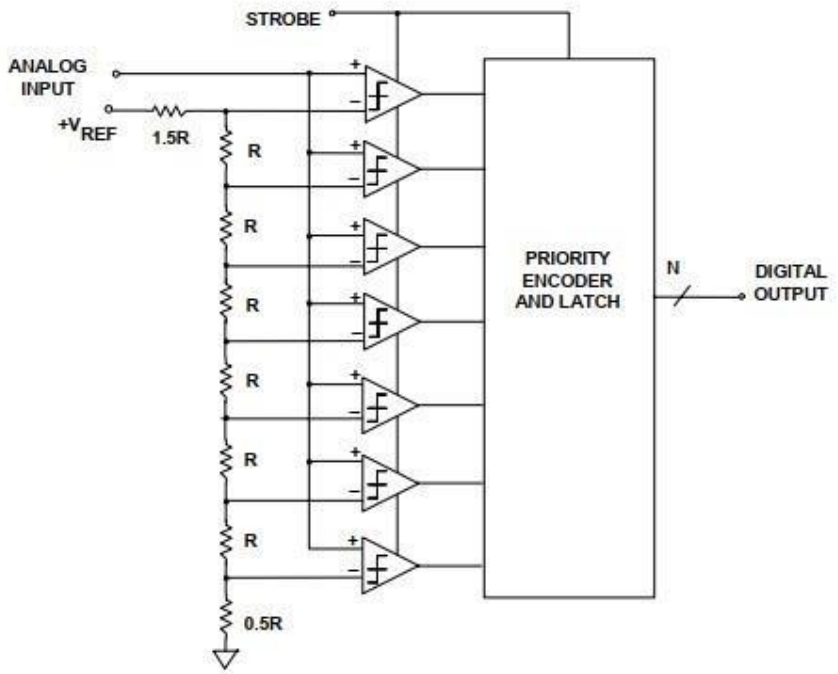

Figure 3: 8-bit flash ADC [3]

The input voltage for conversion is applied to the non-inverting inputs of all the comparators arranged in parallel. The divider network divides the full-scale reference to equal interval which is then supplied to different pin of comparator successively. Now comparator switches its output to logic one if the input voltage on to the comparator is greater than the reference voltage on the inverting input. The outputs give us a digital representation of the voltage level of the input signal only the highest value is supplied to the main output of ADC using priority encoder. Each comparator represents a state in the bit combination except the lowest state. So, the comparator count for this ADC is greater and increases exponentially.

The priority encoder accepts the highest state comparator with the output as logic high (1) to represent the relative state of the analog voltage.

The pros of this converter are that they are very Fast and don't require clocks inputs. And the cons can be that they are expensive, power hungry and the complexity doubles for each addition of bit.

3.1.3.2 Successive Approximation A/D Converter

It is one of the most used ADC. Conversion time is faster than Dual slope but slower than Flash. It has fixed conversion time for any value of analog input. Successive approximation register (SAR) generates a series of bit and DAC convert it into analog value which is compared with output. Figure 4 shows a block diagram of components involved in the conversion.

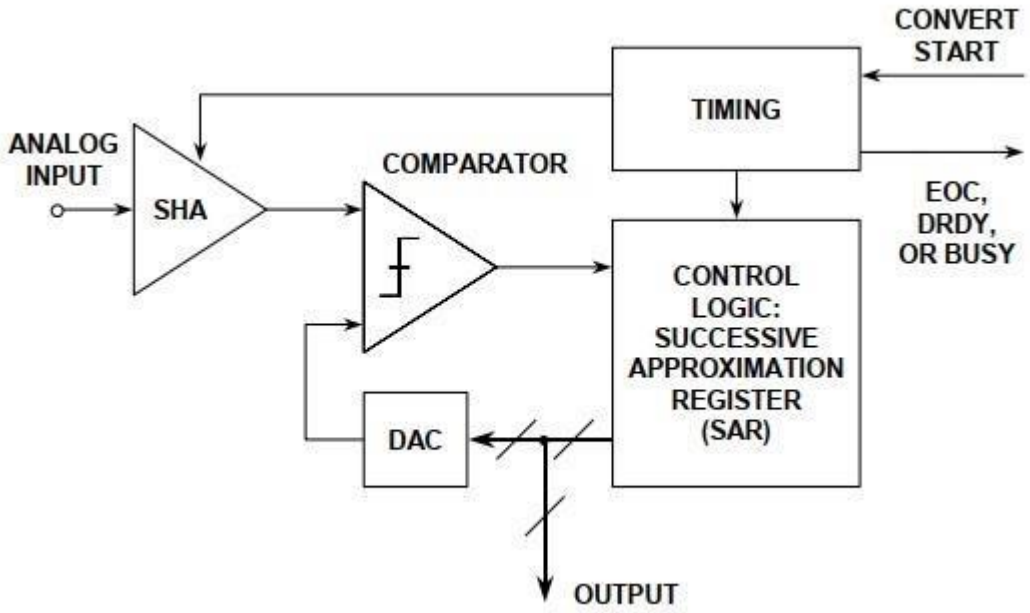

Figure 4: structure of successive approximation A/D converter [3]

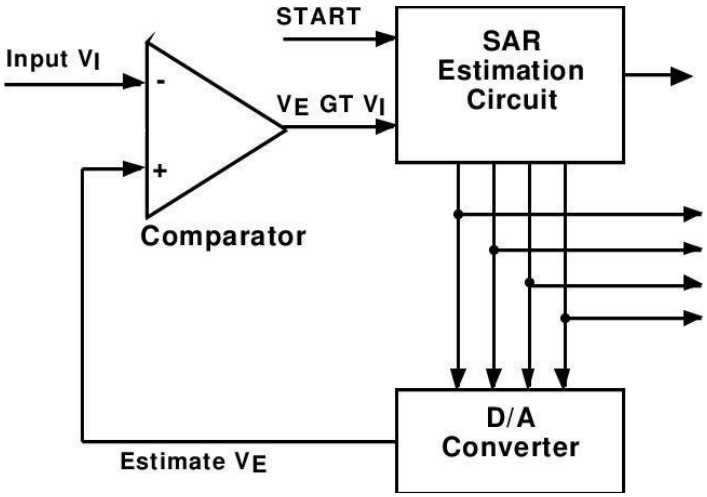

Figure 5: 4-bit SAR ADC

Operation

It is based on the binary search approach since the equivalent output is generated by reaching in every half part of the suspected region. The first iteration starts from a half value e.g., 1000 for 4-bit and 10000000 for 8-bit.

For 4-bit ADC as shown in Figure 5, 1000 binary value is generated with DAC and the analog value of 1000 is compared with the output. If it is greater, 1 is flipped to 0 otherwise retained. Then in next clock cycle the second bit is changed to 1 and the whole cycle continues till every bit is flipped and checked.

It includes three major elements: The A/D converter, the successive approximation register (SAR) and the comparator. The conversion technique involves comparing the output of the D/A converter VO with the analog input signal Vin. The digital output becomes equivalent to the analog signal when the DAC output matches the analog signal. In the case of a 4-bit A/D converter, bit D3 is turned on first and DAC's output is compared with the analog signal. If the comparator changes the state, indicating that the output generated by D3 is larger than the analog signal, bit D3 is turned off in the SAR and bit D2 is turned on. The process continues until the input reaches bit D0.

Features: Faster but not fast than flash type, low amount, and simpler components

3.1.3.3 The Counter type ADC

The analog input is fed to the non-inverting pin of the comparator which can be seen in Figure 6. The AND gate's output is high (enable) and so clock pulses are passed along to the counter if V+ is greater than V- input. And the other input given to comparator is the feedback of the output voltage that is the analog version of the digital output of the converter. Thus, the counter counts until and unless its output voltage has value equivalent to the analog input. And whenever the output voltage exceeds the counter stops and the conversion is complete and finally the digital output reached at that point is the digital equivalent of the input signal.

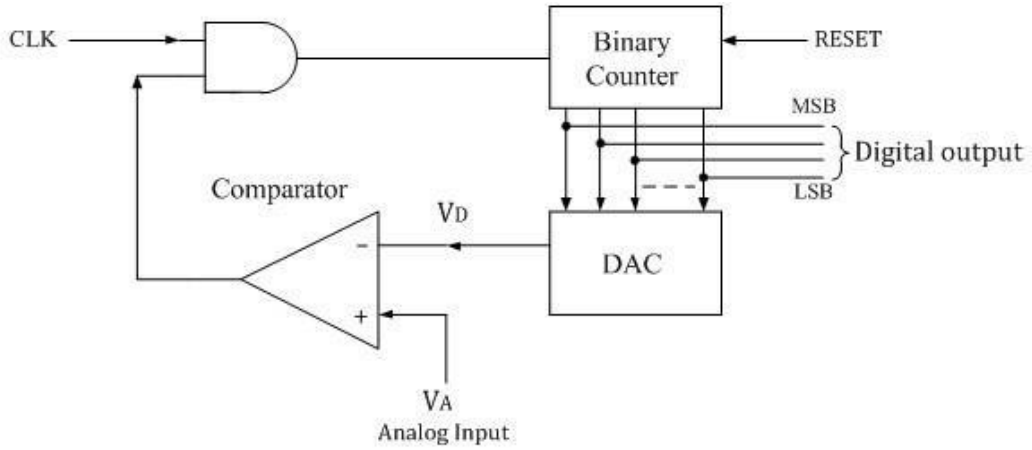

Figure 6: architecture of counter ADC [4]

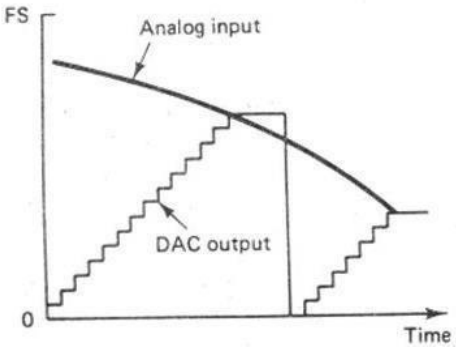

Figure 7: waveform of counter ADC

The waveform in Figure 7 shows a conversion of analog signal. It can be noticed that the higher the value higher is the conversion time, that is conversion time is dynamic. Also, every clock tick increases a step-in ladder and sample frequency should be greater than the signal frequency, so it is a necessity to have clock frequency of,

$$\text{Clock frequency} > 2\text{NFmax} \qquad (2)$$

Where, N = size of counter or bit output of ADC

Fmax = largest frequency in the analog signal

3.1.3.4 Ramp ADC / Dual slope ramp ADC

In this type of ADC, analog form is converted to digital form using basic components like comparator which compares the given analog voltage to some reference or some other constants. This ADC technique involves enabling a counter that count until the feedback of the outputted digital form is less

than the actual applied signal. Feedback circuit contains a DAC that converts the output back to analog signal which when exceeds the input stops the counter resulting in a digital output to stabilize and indicate an end of the conversion. The output of the counter is the final output. The capacitor maintains a fixed charging /discharging time for the purpose. The block diagram is shown in Figure 8.

Dual Slope ADC is used in the Digital Voltmeter and other type of measuring instruments because of its large resolution and low cost.

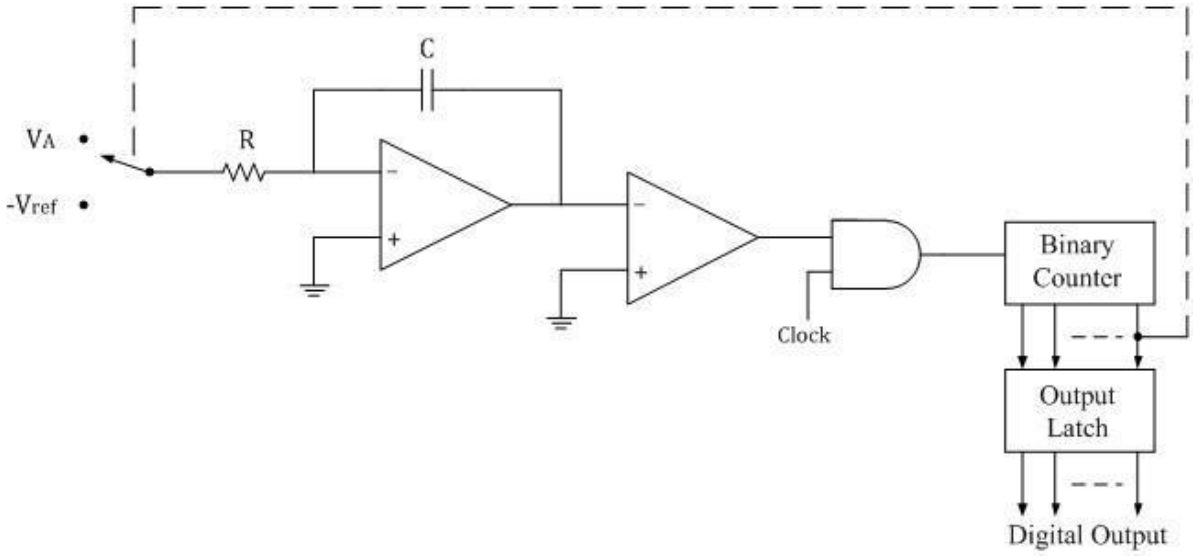

Figure 8: dual slope ADC [5]

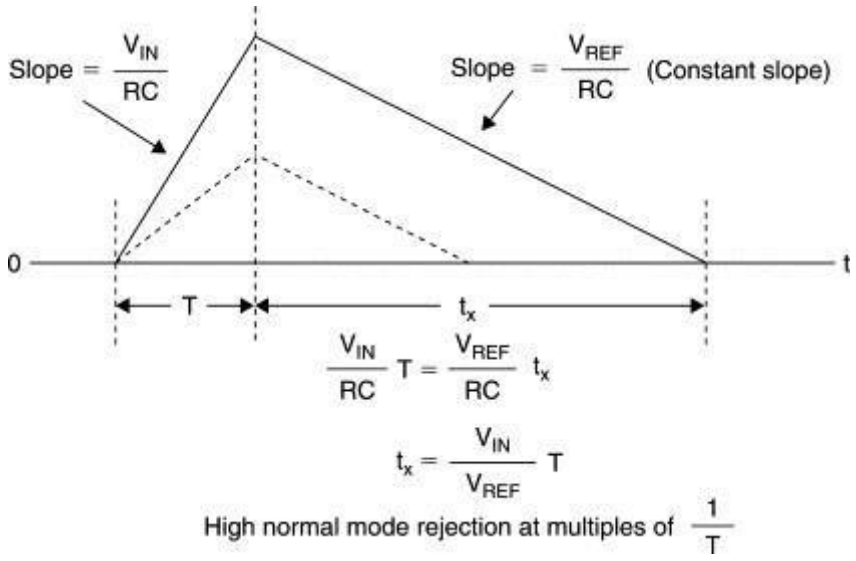

Figure 9: waveform of ADC and timing [3]

Operation

First, capacitor is reset (i.e., V_o is made zero)

For positive V_{in} we need negative V_{ref}.

As shown in the Figure 9 during time T1, the capacitor is charged by the Vin for fixed time interval which is controlled by the control unit with a fixed current (I equal V_a/R).

After time T1, the control unit switches the connection from Vin to – V_{ref} through which the capacitor is discharged. This discharge through the fixed slope until it becomes zero which is sensed by the comparator. The reading of the counter is the output for the input.

3.1.3.5 Integrator ADC

Circuit of integrating ADC incorporates op-amp as integrator and selection switch to switch between input voltage and the reference. The schematic of simple integrator is shown in Figure 10.

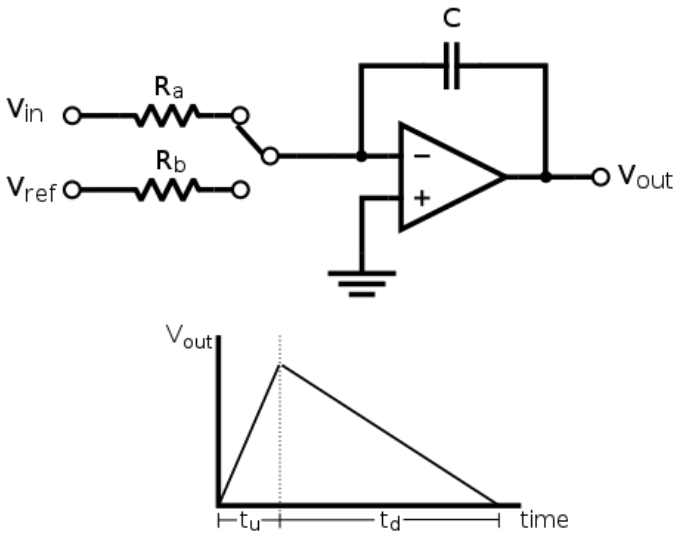

Figure 10: integrating ADC

Based on implementation, flip switch can be placed parallelly with integrator capacitor to discharge the capacitor such as to reset the integrator. There is a converter control/logic unit that can control this switch and other components. Conversion is carried out in two phases: run-up and rundown phase as indicated in graph of Figure 10 by t_u and t_d respectively. During run-up phase accept input as the voltage to be converted and run-down phase is where input is the reference voltage (the highest value up to which input voltage can be recognized). This selection process is where switch comes into play. The time taken in these both phases are compared in time using a charging and discharging time-period each operation takes determines the digital value.

3.1.3.6 Pipeline ADC

Pipeline ADC is step-by-step model of amplitude quantizer where digital signal is generated by passing the input signal through a cascade of different topologically identical stages with low resolution encoders. Conversion rate improves throughput with sample and hold amplifiers between consecutive stages performing operation concurrently. But this multi-stage architecture and holding operation increases the circuit latency. Figure 11 can elaborate more visually. A single stage has its own sample and hold and a quantization sub-ADC.

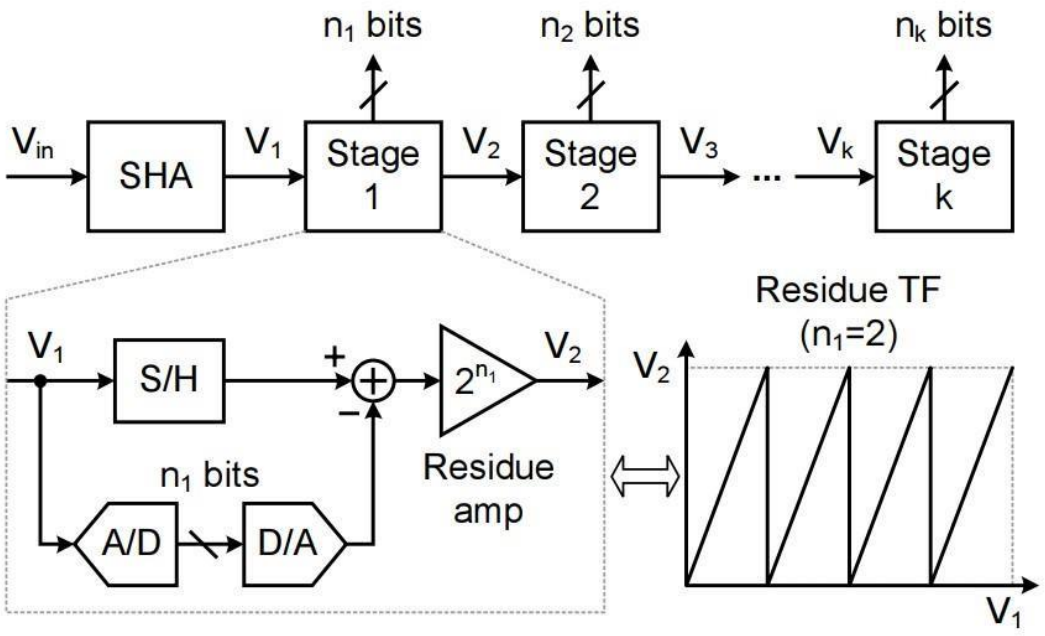

Figure 11: block diagram of pipeline ADC [6]

A single sample must go through the series of stages laid inside the ADC get the full resolution which is achieved by combining output of those different stages. Almost all pipeline ADCs applies digital error correction to decrease the accuracy demand of flash ADCs [6]. Notice that the residue at the summation-node output has a dynamic range one-nth (n is the bits count of first stage, subsequent stages can have different bit count) that of the original Stage 1 input (VIN), yet the subsequent gain is only half [6]. Hence, at stage 2 only half range signal is passed and is responsible for conversion of half range signal which contributes to half range in n-bit too.

If one of the comparators in the first n-bit flash ADC has a significant offset when an analog input close to the trip point of this comparator is applied, then an incorrect n-bit code and thus an incorrect n-bit DAC output would result, thus producing a different residue. If this gained-up residue does not overrange the subsequent n-bit ADC, it can be proven that the LSB code generated by the remaining pipeline (when added to the incorrect n-bit MSB code) will give the correct ADC output code [6]. The implication is that none of the flash ADCs has to be as accurate as the entire ADC. In fact, the 3-bit flash ADCs in Stages 1 through k require only about n + 1 bits of accuracy. [6]

3.1.3.7 Sigma-delta ADC

Fundamental components present in Figure 12 and involved principles are briefly explained below:

Modulator: The first stage is a modulating stage that converts the input to a single bit PCM code stream as shown in the Figure 12.

Oversampling: The input signal is oversampled (sampling the input signal at much higher rate than Nyquist rate) to reduce the quantization noise, which happens at the first stage that is the modulator stage, and it lowers the noise power to a lower level as seen in Figure 13(B).

Noise shaping: The density of "ones" at the modulator output is proportional to the input signal. The comparator generates larger amount of high logic when input is increasing and similarly greater amount of low-level logic for decreasing input. On accumulation of error voltage, the integrating part behaves like a high pass filter for noise due to quantization and a low-pass filter to the input signal. Therefore, most of the noise is shifted to the higher frequencies which can be filtered out with a low pass filter with ease as shown in Figure 13(C). Oversampling is responsible to changing the distribution only but actual noise power remains the same.

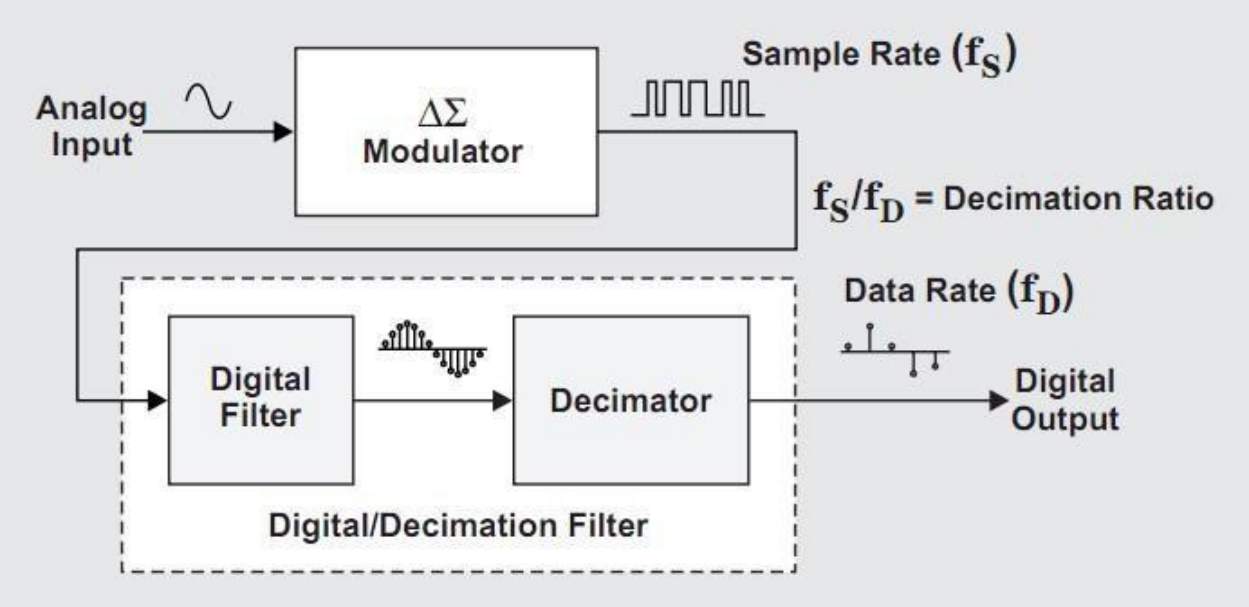

Figure 12: full sigma-delta ADC [7]

Digital filter: Digital filter is non less than a low pass filter implemented in digital domain which is fundamentally integration. Best is to use a sinC filter of different order to segregate high frequencies from our interested signal range.

Decimator: This is an implementation of the running average. Faster the sampling rate more is the possible bit resolution.

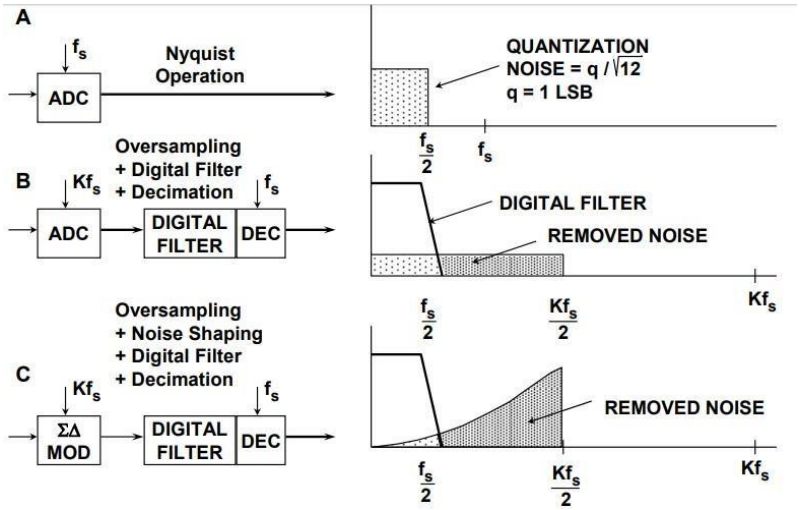

Figure 13: oversampling, digital filtering, noise shaping, and decimation [3]

Features: Very high resolution is possible for high sampling frequency, 32-bit of resolutions is made possible, can be used with very sensitive and small signals.

3.1.4 Sampling Theorem - Nyquist Sampling Theorem

Sampling theorem is the most basic theory in information theory related topics. Or we can call it a most necessary criterion for information acquisition. Generally, the process involved in converting a continuous time, space, or natural signal to series of discrete valued signal that is also the function of same domain of space or time is Sampling. Sampling theorem states: Considering a time function x(t) which in band limited to Frequency B, the information about the signal can only be preserved if the sampled with a period of 1/(2B) or lesser. In other words, to reconstruct a signal in future, the input signal should be sampled at the frequency greater or equal to twice the greatest frequency present in the input signal i.e., **fs ≥ 2fm.** The input signal is always sampled assuming a band limited signal and when saying bandlimited, it means that no energy is present in the frequency distribution above the certain band limit given by B. In formula, the concept can be represented as follow, but before that let us consider x(t) as our continuous time input signal and X(f) as continuous Fourier transform of x(t) in equation 3:

$$X(f) = \int_{-\infty}^{+\infty} x(t)\, e^{-i2\pi ft} dt \qquad (3)$$

x(t) is a band limited and one-sided signal with bandwidth B, if:

$$X(f) = o \qquad for\ all \qquad |f| > B|$$

Then according to sampling theorem, for exact re-constructability following is a necessary condition if f_s is the sampling frequency:

$$f_s > 2B \tag{4}$$

or:

$$B < \frac{f_s}{2}$$

There is a time interval between the successive samples which is called sampling interval as formulated in equation 5, the 2B frequency is Nyquist rate and fs / 2 is termed as Nyquist frequency and is a property of this sampling system.

$$T = \frac{1}{f_s} \tag{5}$$

and equation 6 is representation of the samples:

$$x[n] = x(nT), \qquad where \quad n \in Z(integers) \tag{6}$$

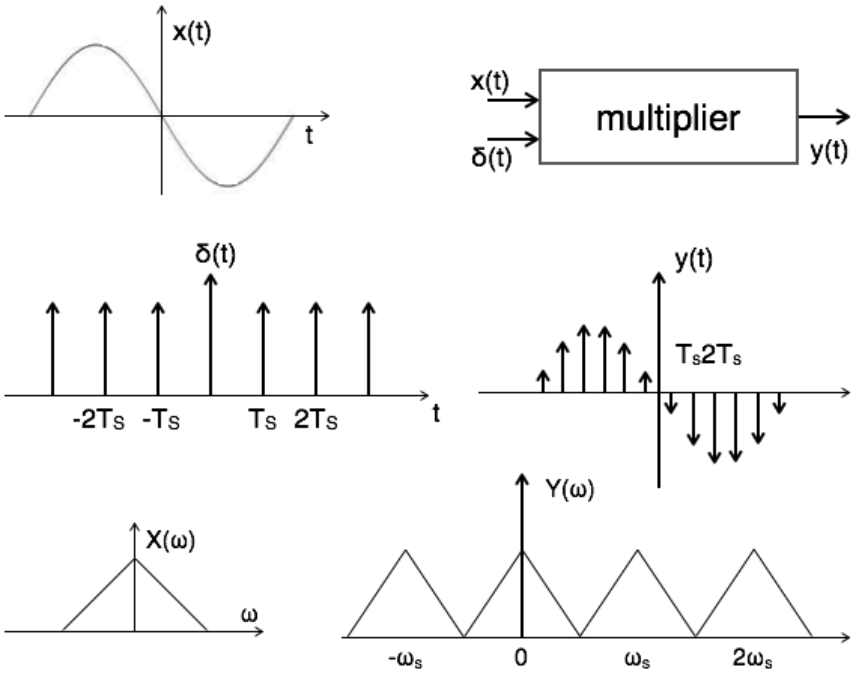

Figure 14: sampling, Nyquist rate [8]

Sampling theorem is a first step know for a proper reconstruction principle of analog-digital conversion and is a sufficient condition. Also, it is important to know about a phenomenon that happens when the

sampling theorem is violated, the term aliasing comes into existence which is the presence of unwanted fragments in the reconstructed signal which scrambles the original signal or the information. The fragments are the overlap of the harmonics the distorts the reconstructed signal and some frequencies of the original signal are lost which makes the acquired meaning less. The Figure 14 shows the proper minimum situation when a healthy signal can be received form the converter system and those frequencies which folds, or overlaps are also known as folding frequency.

Also, we should be careful in determining the signal bandwidth before implementing the converter for sampling since there are times when input is polluted with noise in high frequency. In those cases, the high frequency noises should not be considered as part of the signal since their sampling will demand higher sampling rate, but we should be able to recognize the actual range of signal bandwidth and apply appropriate low pass filter to bypass those high frequency noise before even sampling.

3.2 Digital to Analog Converter

DACs convert digital encoded numbers, usually a binary sequence, into a continuous flow of physical quantity e.g., voltage, a temperature, sound or pressure.

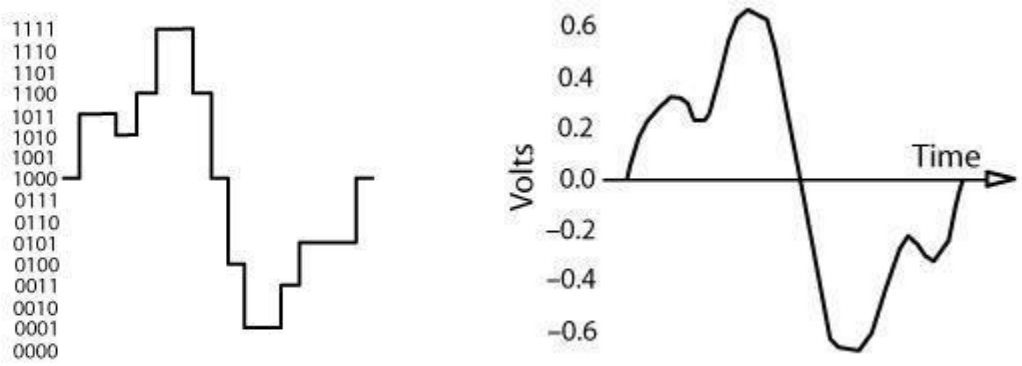

Figure 15: digital to analog conversion

Batches of binary data flowing from a digital source are first represented into pulses between the range limit of the converter and along the converter the impulse form is interpolated to generate a smooth sequence of output signal like in Figure 15 through various filtering procedure. Conventional DACs convert binary values to rectangular spikes with sequence hold period for which the value remained constant which some DACs generates the varying density pulses which is later averaged to smooth the output as a continuous signal.

According to Nyquist–Shannon sampling theorem, a DAC can regain the original signal from the sampled data given that the bandwidth satisfies a certain criteria e.g., Nyquist frequency and bandwidth limitation should be considered. Quantization error is introduced during sampling process that manifests itself as low-level noise in the reconstructed signal.

3.2.1 Parameters (Characteristics) of DAC

Resolution is determined by the number of bits in the input binary word. A 12-bit converter has a resolution of 1 part in 2^{12}.

Full scale output voltage is th**e** maximum output voltage of a converter (while all inputs bits are 1) will always have a value 1 LSB (lowest significant bit) less than the named value.

Accuracy, the actual output voltage of a DAC is different from the ideal value; the factors that contribute to the lack of linearity also contribute to the lack of accuracy. The accuracy is measured as the difference between actual output voltage and the expected output voltage.

Example: A DAC with ±0.2% accuracy and full scale (maximum) output voltage of 10V will produce a maximum error for an output voltage is of 20 mV.

[0.2/100 * 10V = 0.002*10 V = 20mV]

Linearity, an ideal DAC should be linear i.e., the output voltage should be a linear function of the input code. All DACs depart somewhat from the ideal linearity. Typical factors responsible for introducing non-linearity are non-exact value of resistors and non-ideal electronic switches that introduce extra resistance to the circuit. The non-linearity (linearity error) is the amount by which the actual output differs from the ideal straight-line output.

Settling time, when the output of DAC changes from one value to another, it overshoots the new value and may oscillate briefly around that new value before it settles to a constant value. It is the time period between the passing of analog voltage into converter to the output reaching the constant value in the output specified error band about its final value.

Monotonicity, a converter is said to be monotonic if its output voltage value continuous to increase with a continuously increasing input value.

Temperature Coefficient, it is defined as the degree of inaccuracy that the temperature change can cause in any of the parameter of the DAC.

3.2.2 Types of DAC

Like different types of ADCs, there are different types of ADCs developed over time. Major important and most used DACs are discussed as follows,

3.2.2.1 Binary weighted resistor DAC

This is a simple implementation of the summation network to add up the bits value, in a digital quantity, according to their place value. A simple N bit circuit is shown in Figure 16.

Place value significance is obtained through an inverting amplifier summing configuration with an amplification ratio (which provides the place value significance different for every bit position). MSB gets highest ratio i.e., V_{ref} and LSB gets lowest ratio i.e., V_{ref}/n, where n is no. of bits used and V_{ref} is the reference voltage.

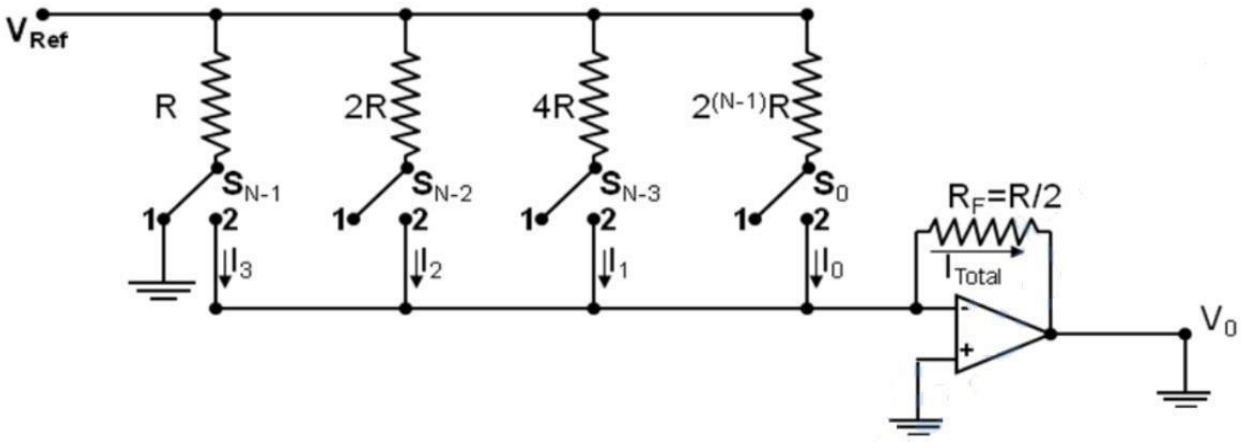

Figure 16: generic binary weighted resistor [3]

$$V_{out} = -i_{Total} \times R \quad (7)$$

$$S \quad = -V_{ref}\left[\frac{0}{2^{(N-1)}} + \cdots + \frac{0}{2^{(2)}} + \frac{0}{2^{(1)}} + \frac{0}{2^{(0)}}\right] * \qquad S \quad S \quad S$$

$$or, \quad V_{out}R_f \quad (8)$$

It is simple to construct and easier to understand yet there is major complication with scaling since on adding more bits, the network becomes large and resistor value will not be practical, every resistor

should be different in the network. Also, exact value is critical to maintain linearity. Conversion procedure is formulated in equation 7 and equation 8.

3.2.2.2 R-2R Ladder Network

This type of DAC consists of ladder like structure of resistors of two values all over (simple analogy, one resistor as vertical section and the other as horizontal one). It consists of two modes in general: Voltage mode, Current mode.

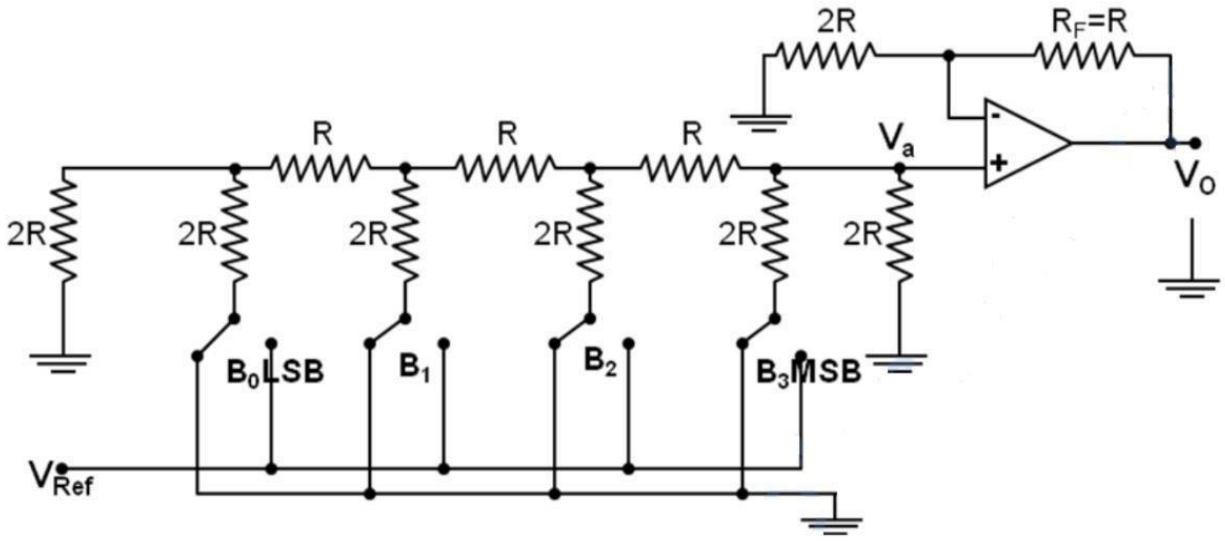

Figure 17: R-2R Ladder (voltage mode) [3]

In the circuit shown in Figure 17, the LSB is contributing 2 times less than the next bit since LSB passes through a resistor 'R' (result of parallel connection) and the next bit passes through a resistor 2R. Similarly, the network grows maintaining two times greater value to the next bit while moving towards the MSB.

Former DAC design required highly precise resistor of different value which is very usually impractical. Manufacturing and cost margin were also affected. But with this new design, only two precision resistors are to be manufactured or fabricated which largely improves its scalability, manufacturing, and cost margins. Also, output impedance is always constant to R however big the network. Thus, simplifying filtering, amplification, and signal processing for integration in the circuits.

3.2.2.3 PWM Digital/Analog converter

PWM signal locks like a sequence of highs and lows with varying duty cycle (the proportion of active time to a total cycle time).

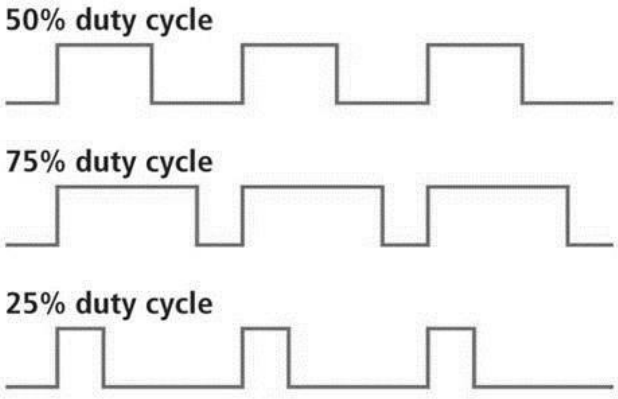

Figure 18: PWM signals

PWM signal is fixed frequency digital signal that can travel between two state high and low. It is dc signal that is chopped in fixed interval as in Figure 18. The average of the signal is the analog value. Less width of high state makes lower analog values (or voltage) while more width indicates higher value. The analog value ranges between the reference supply voltage. There is a term to represent the width of the PWM signal, the term is called Duty Cycle. Duty cycle ranges from 0% to 100%.

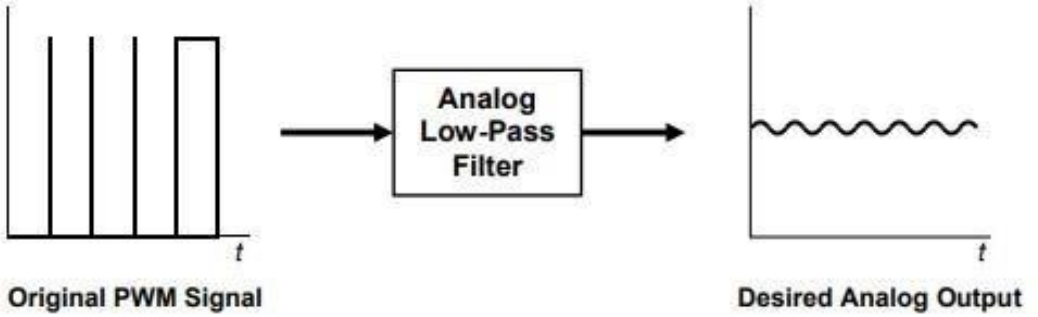

Figure 19: waveform of PWM d/a converter [9]

Additionally, the converter requires a low pass filter in the output stage to average out the PWM signal resulting in an analog value. As in Figure 19, low-pass filter removes the unwanted higher frequency component. This type of DAC is most popular in microcontroller, since many microcontroller (Atmega chips, pic controllers, etc.) uses this type of DAC.

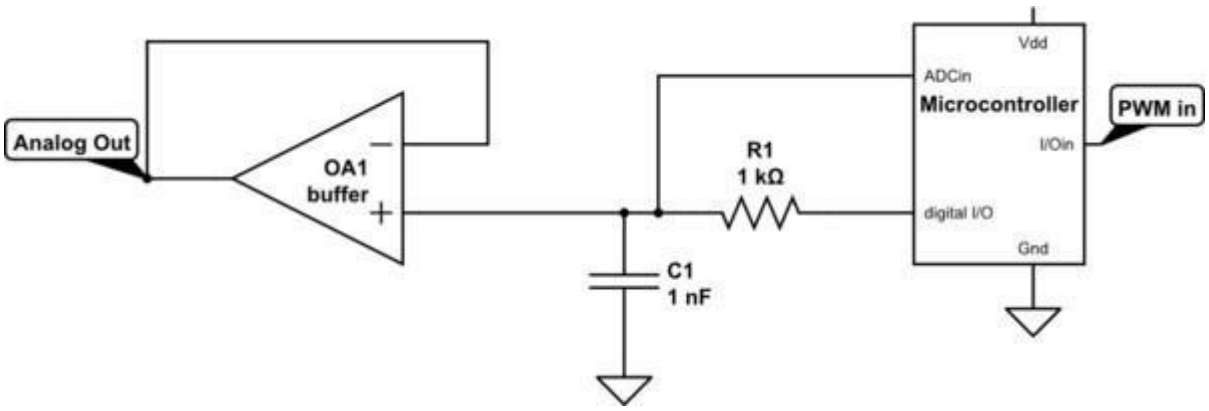

Figure 20: PWM based d/a converter with microcontroller

However, this is intended to be used with a RC filter as shown in Figure 20, to convert the PWM signal into a voltage value by filtering out the AC component and leaving behind the DC component. The voltage output is proportional to the duty cycle of the input – the higher the duty cycles the greater the output voltage of the filter.

3.2.2.4 Over-sampling DAC (Interpolating DAC)

The digital interpolation filter receives the N-bit data at a frequency of f_s indicated in Figure 21. The filter is clocked with the frequency of $k*f_s$. Greater the value of K greater is the separation between the harmonic spectrum as shown in Figure 21. When only considering a minimum Nyquist rate possible, analog anti-imaging filter requirement should be extensive. So, by oversampling and performing interpolation, it will require a simplified filter for similar performance. Another benefit that can be sensed in later part is that the quantization noise is also spread in a greater range reducing the noise density over the frequency domain which is graphically shown in Figure 21. As a result, less amount of noise remains in the signal of interest. It is seen that doubling the sampling frequency helps to improve the signal-to-noise ratio by 3 dB which is further scalable almost linearly. Early CD players took advantage of this, and generally carried the arithmetic in the digital filter to more than N-bits.

Today, most DACs in CD players are sigma-delta types [3].

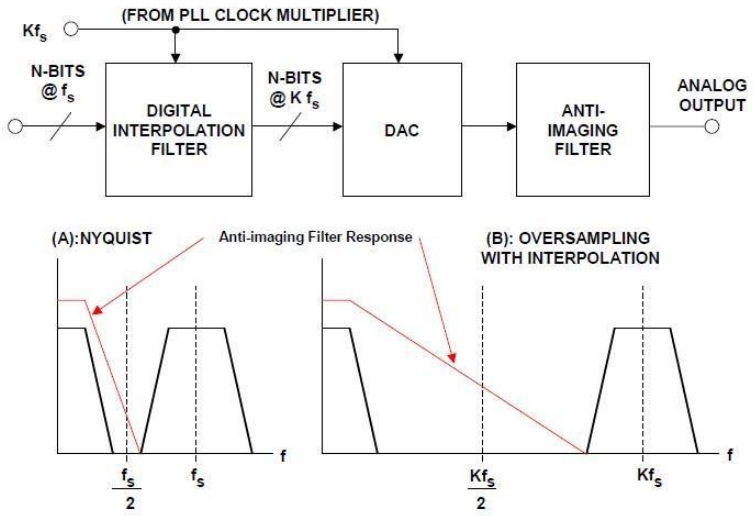

Figure 21: over-sampling DAC [3]

3.2.2.5 Thermometer-coded DAC

This is a DAC that is counterpart with the flash ADC. The thermometer-code DAC consists of equal number of current source part as the number of possibly output values, a thermometer-coded DAC, one for each one. For instance, a thermometer-coded DAC will have 255 segments and 65,535 segments of it had been designed for 8 and 18-bit input respectively. Although such DACs have the highest speed and accuracy, they are highly expensive, and complex compared to other kinds of DACs. Such DACs can process greater than 1 billion samples per seconds which is greater than any other type of DAC.

3.2.2.6 Hybrid DAC

Hybrid DACs tries to accommodate the feature and special characteristics of the different DACs which ultimately make improve the overall operation. Hybrid DACs also provided flexibility, lower cost, greater speed, precision as compared to individual DACs. Existing segmented DACs are the hybrid DAC and uses thermometer-coded principle for most significant bits, and binary-weighted principle for least significant bits. This type of combination of DACs seems to beat the individual DACs which are limited in various scenarios. Also, with this concept, a tradeoff is achieved in between the precision of the DAC and the number of current sources required by the DAC.

4 Simulation and Analysis

This simulation is aimed to represent a model of the ADC and DAC system which will eventually reveal the concept of the conversion procedure. Both system of ADC as well as DAC and a control interface

will be discussed in the simulation and result will be presented. Simulation will be done with the help of popular software which will facilitate to produce schematic, simulation environment, instruments for observation and finally also the PCB lay-outing. The simulation software, Proteus [10] is used that favorable condition for the purpose. Special guidelines are mentioned wherever needed.

4.1 Architecture

The implementation includes an ADC circuit, a microcontroller and finally a DAC. Data acquisition, Conversion (A/D), Manipulation, Conversion (A/D), Presentation are the steps involved in a full conversion cycle. Figure 22 shows the flow of information from source to a sink and a full cycle of data conversion in a digital system is shown. The components that are going to used require various signaling requirements like digital outputs and interrupt handling which can be realized easily with a microcontroller. Having familiarity with Arduino mega controller, it is used for microcontroller.

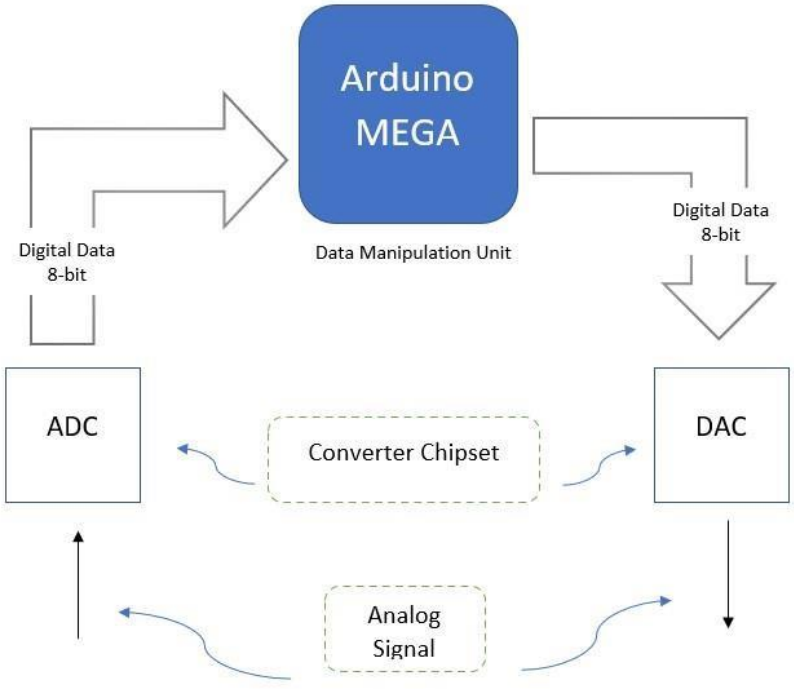

Figure 22: general architecture

4.2 ADC Section

The following section includes the simulation, analysis and recognition of the tools and converter system. The first part, the analog to digital converter will be discussed along with the microcontroller

section here. Needed parts and instruments required to realize the circuit are listed in Table 2 and Table 3.

Table 2: parts/components used in ADC section

Component	**Type/Value**
ADC0801	8-bit ADC
Potentiometer	100 K
Resistor	10 K
Switch	2 Way
Capacitor (Electrolytic)	1 nF, 100u
Power Supply Adapter	5 V
Arduino Mega	Atmega2560

Table 3: instruments used in the simulation

Instruments
Function generator
Logic Analyzer
Serial Terminal

4.2.1 ADC0801

ADC0801 is an 8-bit device that can directly drive other peripherals with its tri-state output latches [11]. It is based on both TTL and CMOS specification, so it's output as well as input logic are compatible with both family of standards and therefore there is no need an interface option for compatibility. ADC0801 has differential input model fed with V_{in} (+) and V_{in} (-). Double ended mode is normally used but with a single ended input one of the Vin is asserted to a fixed reference and signal is fed to ground. The input span range is realized with a certain voltage, which is half of the required span, at the $V_{ref}/2$

of ADC0801. For example, if 5v span is required then 2.5V is applied to $V_{ref}/2$. This translates input range to a voltage span between 5V and 0V also in digital form FFh to 00h respectively. Unconnected $V_{ref}/2$ pin makes the voltage span from supply voltage 5V to ground. If the span is less than 5 and the range of input signal starts with an offset from 0V, the same can be achieved by applying corresponding voltages at pins $V_{ref}/2$ and V_{in} (-).

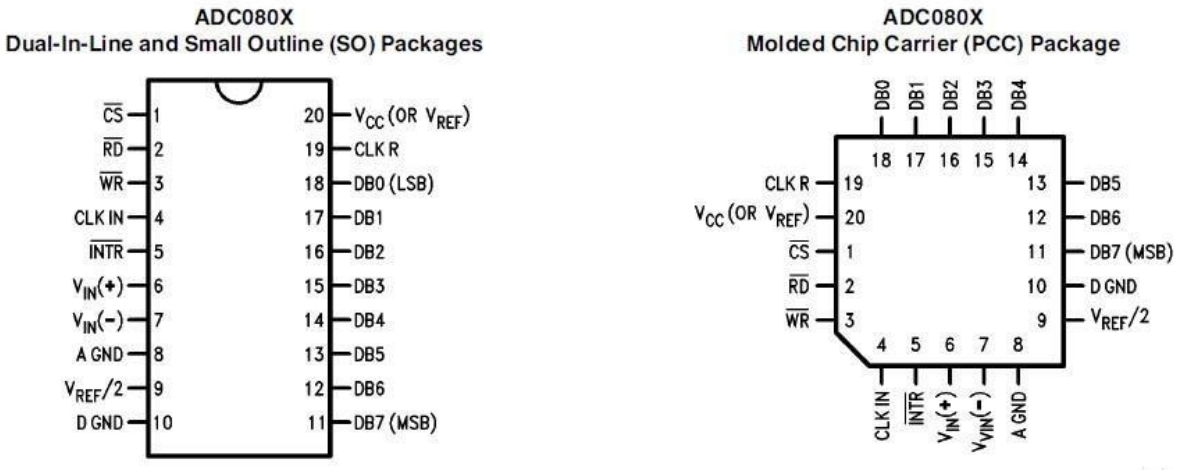

Figure 23: pin configuration of ADC0801 [11]

The AD converter contains an internal clock generator circuit. For putting the chip into operation, either an external clock or the built-in clock generator can be used. ADC0801 provides the pin, CLK IN (pin 4), for connecting external clock signal. The internal clock generator circuit of the ADC can be used for generating the necessary clock signal to the system. Clock can also be generated externally by attaching a RC (resistor capacitor) network of desired frequency which is controlled with the very value of the R and C, the R and C configuration is also discussed in later topics. There is internal connection of CLK IN pin to a Schmitt trigger and CLK R is also attached to output pin of the same Schmitt trigger.
The pin diagram of the chip is shown Figure 23.

4.2.1.1 Specifications:

- 8-bit ADC (by Texas Instruments)
- Type: Successive approximation resistor (SAR)
- Supply Voltage: 6.5 V (max.)
- Clock Frequency: 1.460 MHz (max.) and 640 kHz (typical)
- Conversion time: 66-73 Clock-Cycles
- Easily compatible with Microprocessors and Microcontrollers
- Distinct analog and digital grounds

- Power consumption:
- Follows TTL specifications for digital logic

4.2.1.2 Clocking Options:

There are two clocking modes in ADC0801 i.e., internal clocking mode and external clocking mode. External clocking is easier since an externally generated clock is fed to the CLK IN pin of the IC keeping the CLK R pin unconnected [11].

And the internal clocking is achieved by using a customizable R-C network externally installed outside the chip using appropriate resistor and capacitor in the configuration as shown in the Figure 24. Appropriate frequency can be generated by using the formula in equation 9.

$$f_{clk} = \frac{1}{1.1\,RC} \qquad (9)$$

This mode is used in this demonstration i.e., the internal clocking mode.

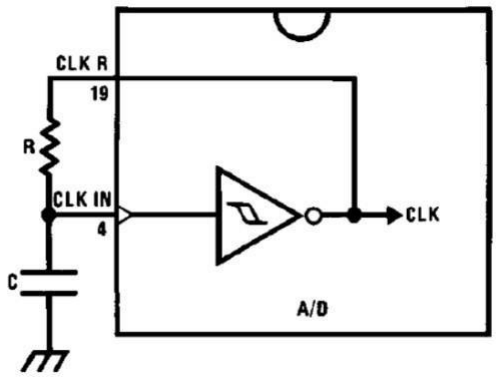

Figure 24: internal clocking mode [11]

4.2.1.3 Conversion procedure:

RD', WR', CS', INTR' are the necessary control signal to operate ADC0801. The CS' signal is used for activating the ADC chip. The conversion starts when active low signals CS' and RD' are held logic low. The internal Successive Approximation Register (SAR) resets, output lines are held in high impedance state after WR' is activated. This signal makes a transition from asserted state to high. The ADC indicates data ready or end of conversion by asserting the line INTR' low. Generally, this signal is used to interrupt a microcontroller which will then read data out of the output line. The digital binary data is available on the 8-bit data bus of the ADC after INTR' has been activated. The INTR' signal is

reset when the RD' signal is asserted low by the microcontroller. Figure 25 shows the flow and signaling involved in conversion.

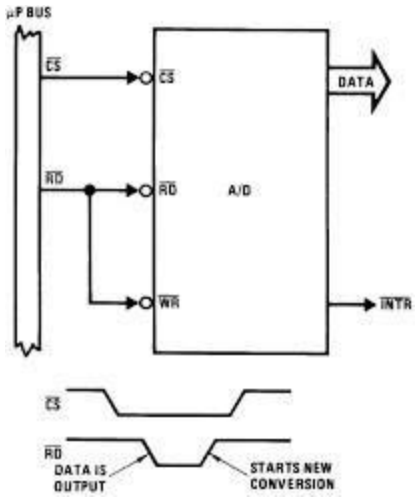

Figure 25: signaling diagram [11]

Schematic diagram:

Figure 26 is a snapshot of the schematic diagram constructed in the Proteus simulation software. It shows a function generator that generates a sinusoidal signal which is connected to the ADC chip ADC0801 and of who's the output data lines are connected to the microcontroller that is used here as a control unit synchronizing all the operation like interrupt handling and action triggering. Beyond the major components, there are simulated instruments like oscilloscope, serial terminal
(Displays the data from the microcontroller)

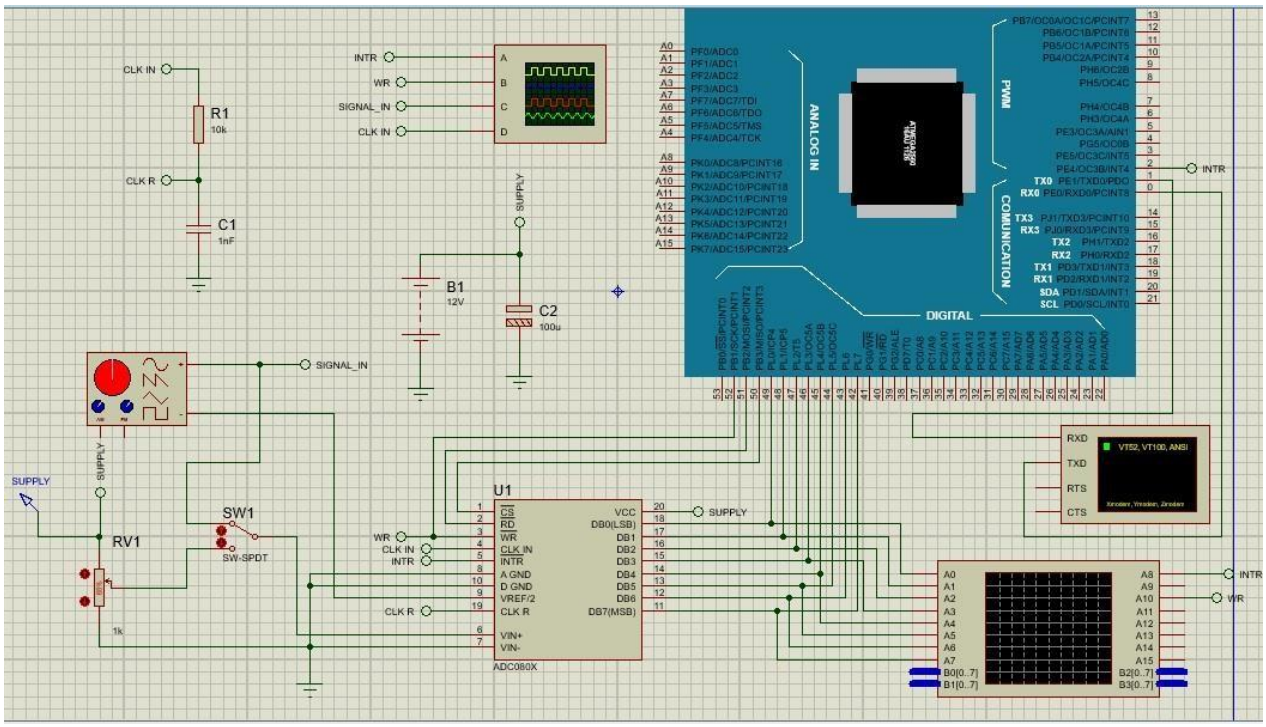

Figure 26: ADC stage

Input

There are two types of inputs to be used for the simulation, they will be, Variable consistent voltage i.e., realized by a potentiometer working as a voltage divider and the signal generated by the lab-bench function generator Figure 27 shown a control dashboard having the options for producing variable periodic signals of different kind: triangular, square, saw-tooth and sinusoidal. The frequency area on left helps to control the frequency output while the amplitude and signal sections towards the right controls the amplitude of output signal and the waveform type respectively. For the purpose, sinusoidal setting is used.

Here the first type of input is used for testing and validation. And the real signal is from the function generator which is used for this demonstration that is shown in Figure 28. The yellow-colored waveform is the sinusoidal signal of frequency of 500 Hz.

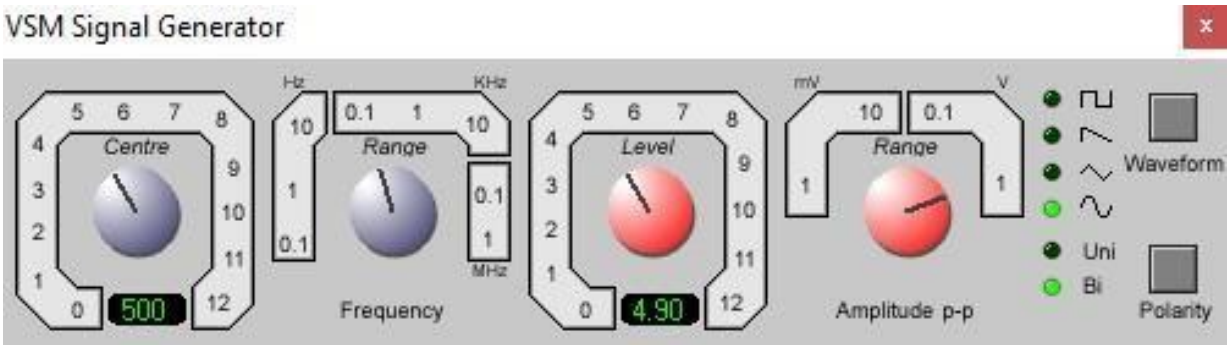

Figure 27: function generator dashboard

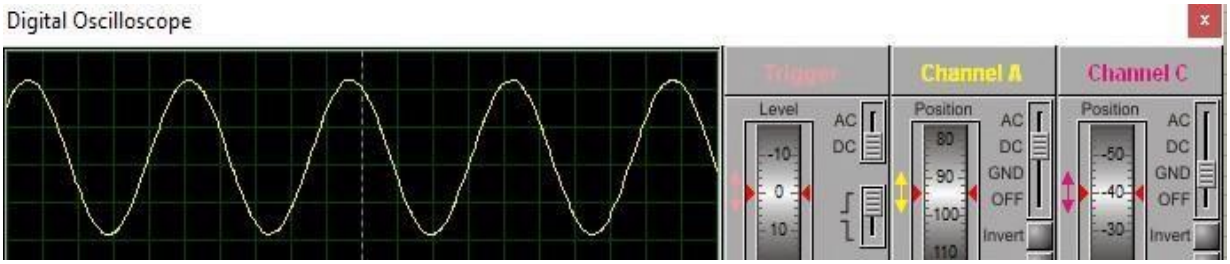

Figure 28: glimpse of sinusoidal input signal (0.5 kHz)

The inputs are fed to the ADC0801 chipset for conversion and the output is sent to 8-bit port of microcontroller. Here PORTL is used as an input in Figure 26.

Due to high popularity, wide support and easier prototyping in Arduino IDE, Arduino MEGA is used. Also, there are many ports (8-bits) in the microcontroller so as the input and output can be demonstrated with a single micro-controller.

Output

Output is 8-bit parallel data stream going to the microcontroller as shown in Figure 29. In the figure, various instruments are attached in the circuit to observe the results of the simulation like Oscilloscope, Logic analyzer, Serial terminal, used for monitoring.

4.2.2 Simulation

Settings

Input signal: sinusoidal – 0.5 kHz

Clock:	internal – 100 kHz
Supply:	5V (also V_{ref})
Mode:	single-ended (Vin (-) terminal is held to ground)
Signal Ground:	$V_{ref}/2$ (pin of ADC0801 to accommodate the bipolar signal)

On running the simulation, we observe that the converter chip is working when right code is implemented on the microcontroller. The code is scripted in the Appendix**.**

This console in Figure 1Figure 29 is a virtual terminal available in the simulator showing the serial terminal output of the microcontroller where the data output of the ADC is printed in each new line.

The trend can be seen to have repeating pattern since it is a digital representation of the sinusoidal input shown in decimal format.

This data will be represented graphically in the DAC section where we can be able to observe it more naturally.

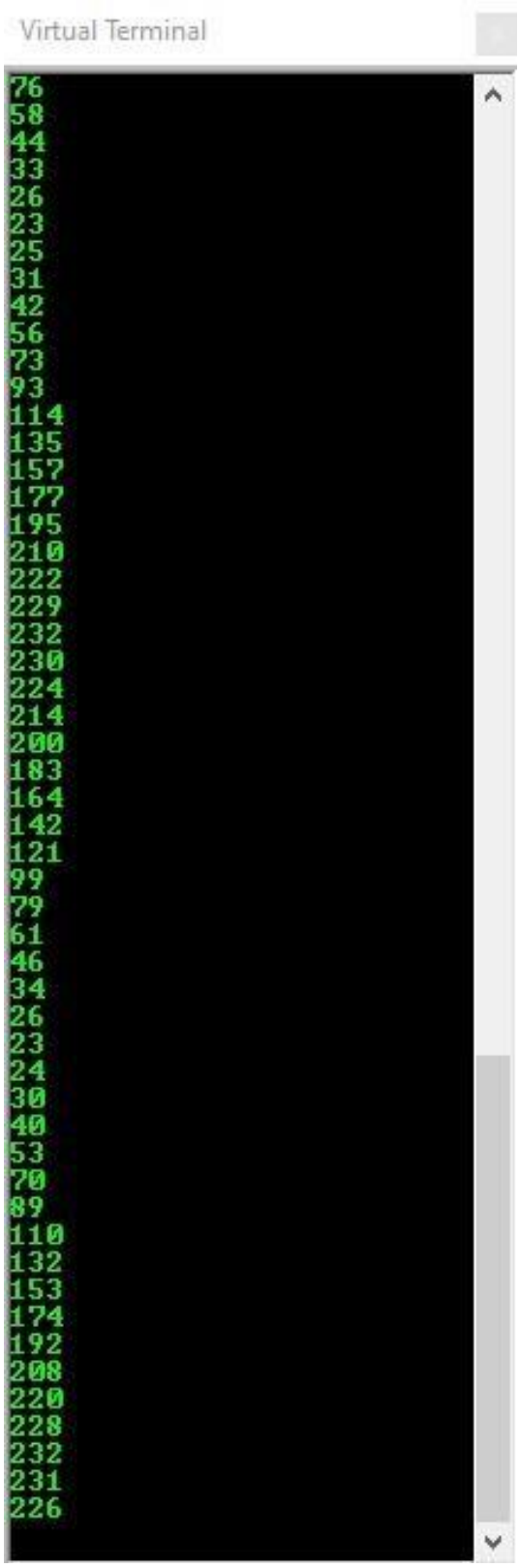

Figure 29: virtual terminal

4.3 DAC Section

The following section includes the simulation, analysis and recognition of the parts, components, tools and converter system. The first part, the analog to digital converter will be discussed along with the microcontroller section here. The required parts and instrumentation are listed in Table 4 and Table 5.

Table 4: parts/components used in DAC section

Parts	**Type/Value**
DAC0808	8-bit ADC
Resistor	4 K 2 K
Switch	2 Way
Capacitor (Electrolytic)	1nF
Arduino Mega	Atmega2560
OP-AMP	LM741

Table 5: instruments used in the simulation

Instruments
Function generator
Serial Terminal
Lab Bench Supply

4.3.1 DAC0808

This DAC0808 is designed in such a way that its tri-stated output latches can directly drive the processor/controller data bus/port [12]. The logic inputs and outputs of ADC0801 meets both TTL and CMOS voltage level specifications and can be used with both and CMOS/TTL logic family without using any interface conversion logic. The pin configuration is shown in Figure 30.

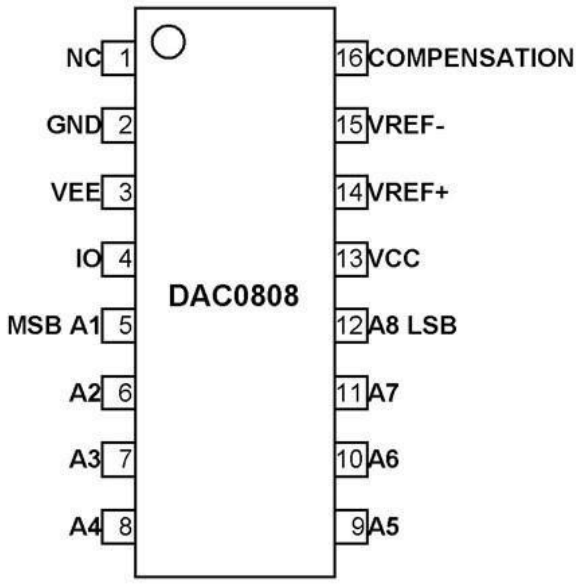

Figure 30: pin configuration of DAC0808 [12]

DAC0808 is an independently usable digital to analog converter chip requiring not more of signaling. The IC supports all the compliance of a TTL device for digitally operated pins. It supports 8-bit digital TTL input at a rate of 20 MSPS (mega sample per second) at maximum. The reference voltages V_{ref} (+) and V_{ref} (-) terminal passes through a current mirror which ensures isolation of the references, which passes to the ladder network to convert the input bits to corresponding analog value through the pin IO.

The network that is used to construct the DAC is R-2R ladder network without an op-amp fitted inside the Integrated chip, DAC0808. The output further needs to be processed which is shown in the output section.

4.3.1.1 Specifications:

- 8-bit DAC (by Texas Instruments)
- Faster settling time (typical value): 150 ns

- Relative accuracy at ±0.19% maximum error
- High speed multiplying input slew rate: 8 mA/us
- Full scale current match: ±1 LSB
- Non-inverting digital inputs are TTL and CMOS compatible
- Supply voltage range: ±4.5V to ±18V
- Operating temperature range: 0ºC to +75ºC
- Low power consumption: 33 mw@ ±5V
- Maximum Power dissipation: 1000 mw

4.3.1.2 Schematic Diagram

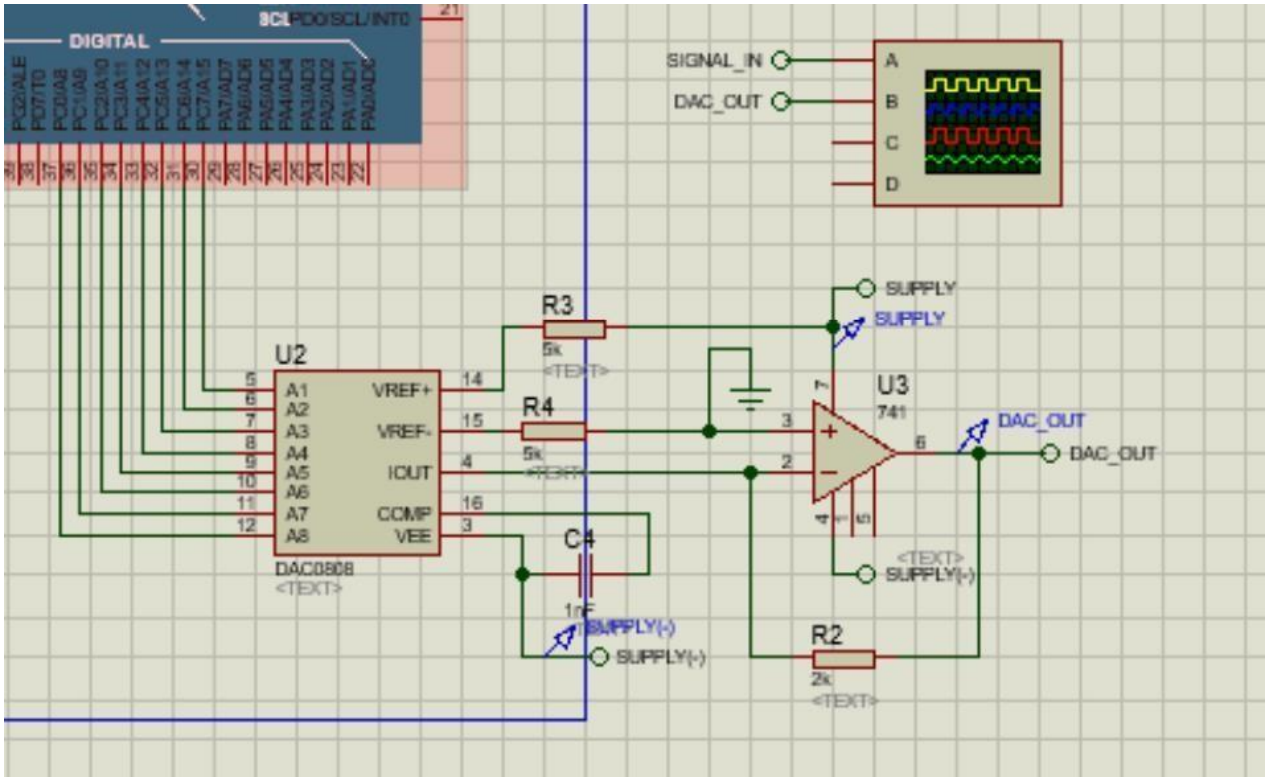

Figure 31: DAC stage

Input

In Figure 31, an 8-bit data is continuously fed to the input data terminals of the DAC0808, a digital to analog converter. The 8-bit data is sourced from the microcontroller, Arduino mega. **PORTC** of the

microcontroller is used in output mode to make outward flow of the data gathered from the ADC. The input is the digital representation of the sinusoidal signal.

Generally, the applied output is a replica of the raw data collected from the ADC in real-time, but there might be some delay associated due to various reasons which will be demonstrated later.

Maximum rate of conversion allowed in the IC is less than 6.66 MHz (propagation and settling time included 150 nS) which is faster enough for our input rate of 0.5 kHz**.** But some chips can handle a bare maximum of 20 MSPS.

Output

The output of the IC DAC0808 is quite interesting since the output is the current in a micro-ampere range. The output current is proportional to difference in reference voltage and to the digital input data bits. Since output in the form of current is not too presentable so it needs to be converted to a voltage, equivalent to the value of the output current.

So, an amplfier stage is constructed as a final ouput stage which used an op-amp circuitary as shown in Figure 32 which also converts the current signal to a more presentable voltage reading.

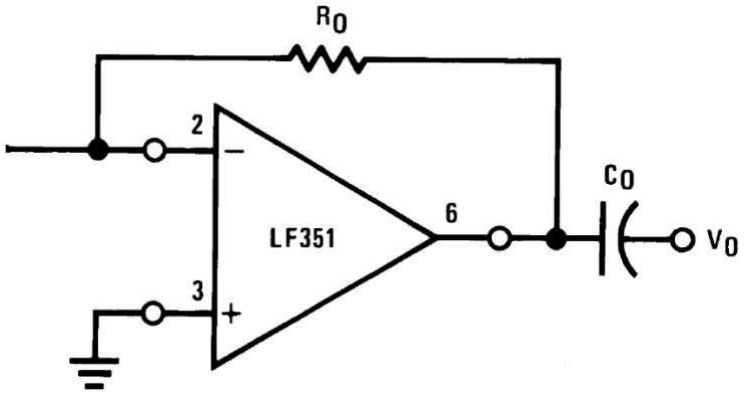

Figure 32: output stage [12]

4.4 Complete Schematic

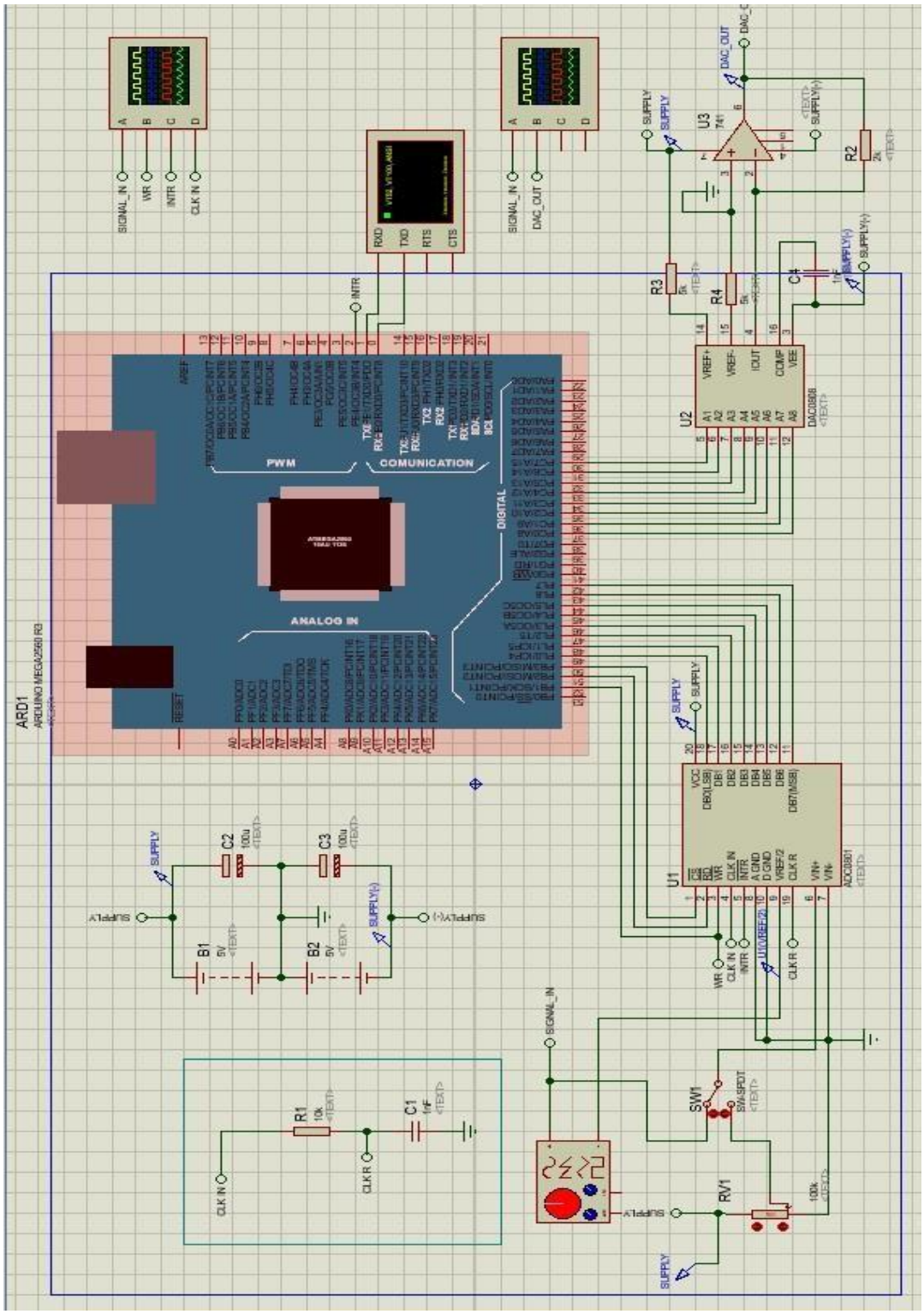

Figure 33: whole system of ADC, controller and DAC

4.4.1 Simulation

Settings

Vref(+):	5V through a 5k resistor
Vref(-):	GND
VCC:	5V
VEE:	5V

On running the simulation with setup in Figure 33, we observe that the converter chip is working when right code is implemented on the microcontroller. The code is scripted in the Appendix**.**

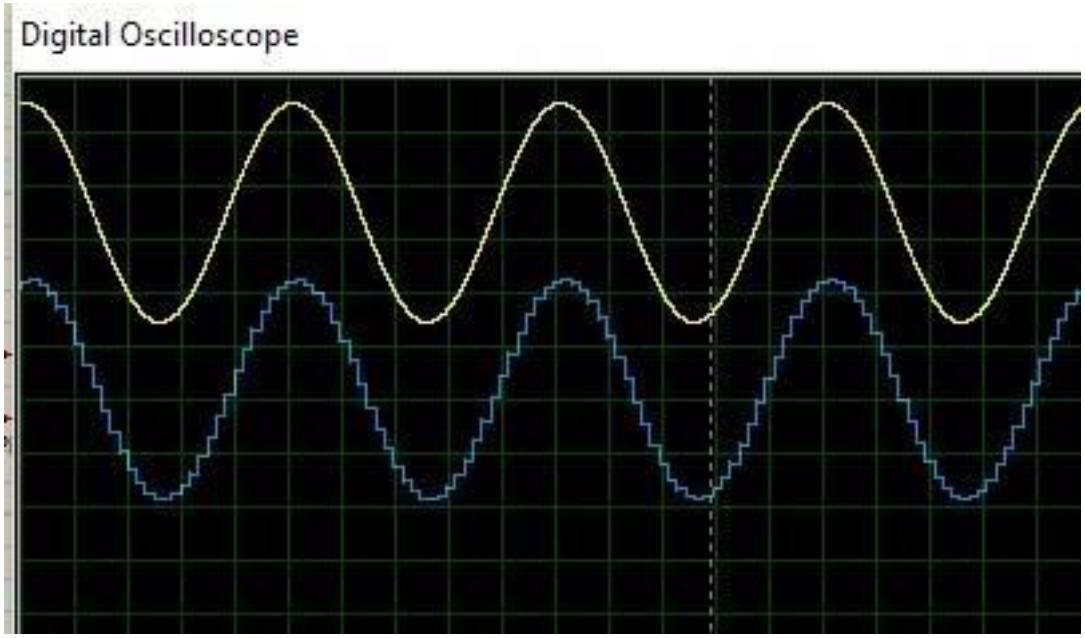

Figure 34: oscilloscope snapshot (yellow->input signal, blue->output signal)

Figure 34 shows an output of the oscilloscope where the first channel is connected to the input signal fed to ADC0801 (A/D converter), the second channel is the output of DAC0808 (D/A converter). This is a representation of the 0.5 kHz signal.

Sample frequency is made constant which is 103-117 microseconds (acc. to datasheet of ADC0801). The sampling period was set to 200 microseconds i.e., 5 kHz (which is 103-117 microseconds according to datasheet of ADC0801), which can be easily done using an Arduino that run with a crystal of 16 MHz Timing signals are also recorded in the oscilloscope. First, we started from a intermediate frequency and raised the frequency until the sampling frequency reached to its limit (given by Nyquist criterion). Later the signal frequency is further increased giving following major and significant observations:

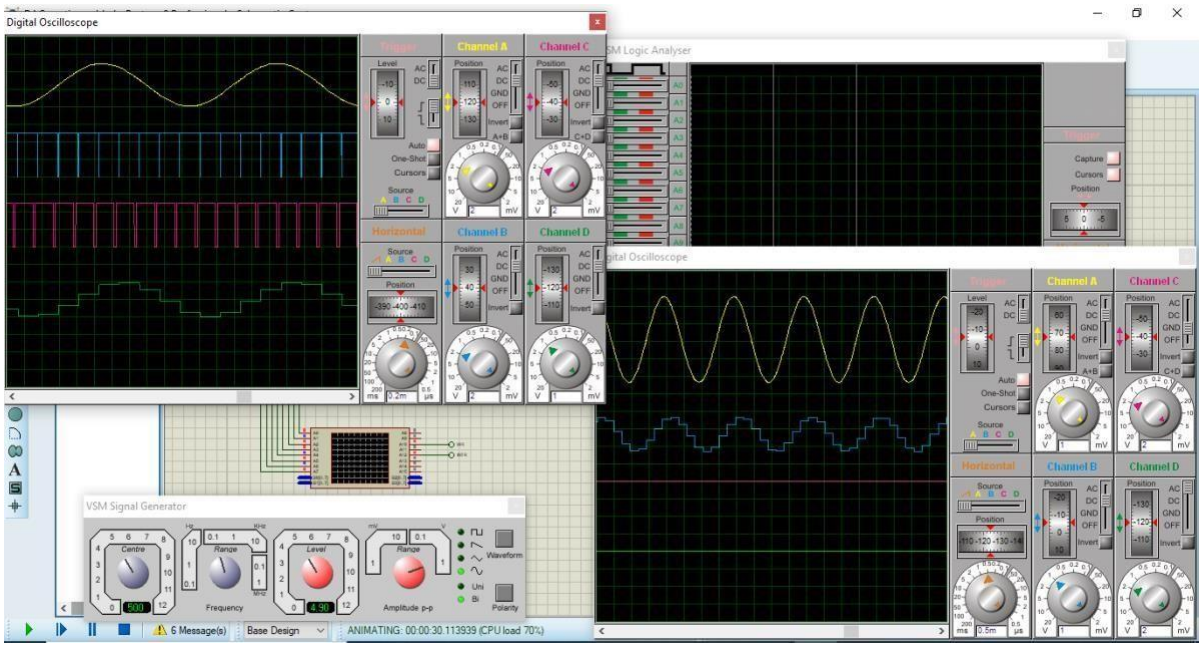

Figure 35: observation at 500 Hz input signal

As in figure 35, the left top oscilloscope shows the signal from various signals analog as well as digital, in sequence. The identification of the signal is presented below:

Setting of instruments in simulation for top left oscilloscope:

- Input signal (Yellow)
- Start conversion or WR' pin of ADC0801 (Blue)
- Interrupt pin of ADC0801 or INTR' (Pink)
- Output of DAC0808 (Green) For bottom right oscilloscope:
- Input signal (Yellow)
- Output of DAC0808 (Blue)
- Other lines are not used

The bottom right oscilloscope is presented in the screen only to represent the input and the output signal. So that it will be easier for comparison. Two oscilloscope have different settings in time scale and amplitude so they might appear to be different, but they are the same signals.

Note *, Following observations will also have similar structure and color scheme as in the above settings.

The conversion starts when active high signal (WR') make a low pulse. And after conversion complete INTR' pin goes low giving a low pulse and then the data is read in the port of the microcontroller. During all these operation CS' and RD' are held high (means keep them active).

Stepped output can be seen which signifies that it is constructed from a digital signal and sampling period is constant.

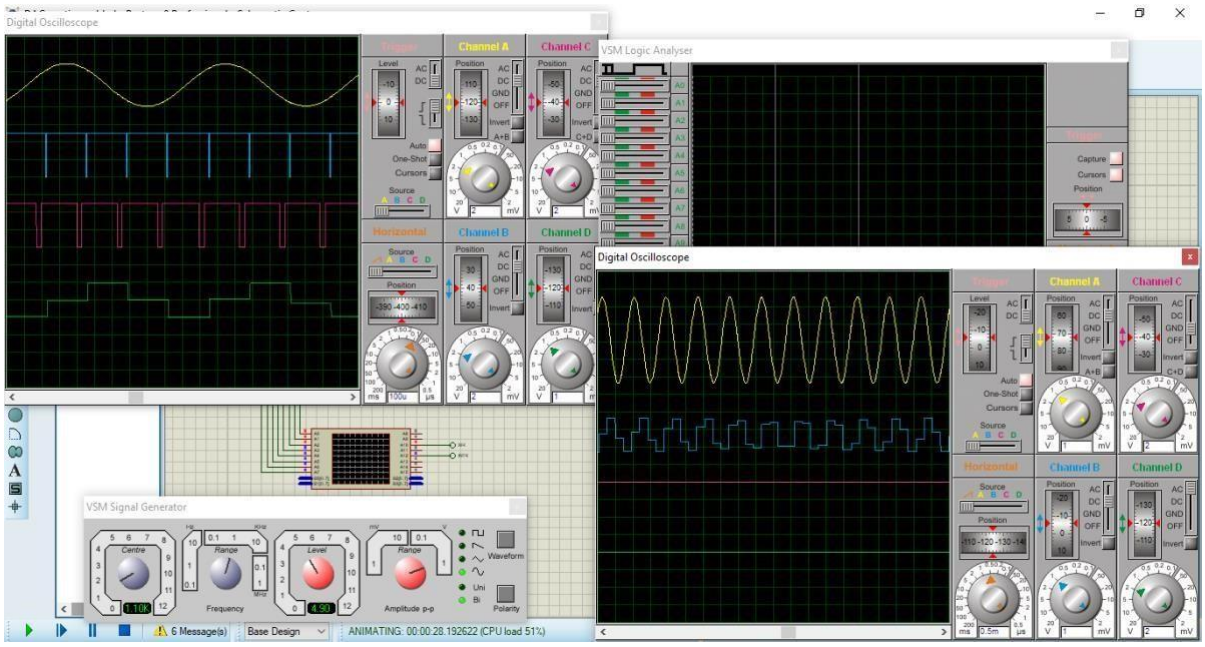

Figure 36: observation at 1.1 kHz input signal

At 1.1 kHz input as in Figure 36, the number of samples is lower, and the quantization noise is higher since less information is available.

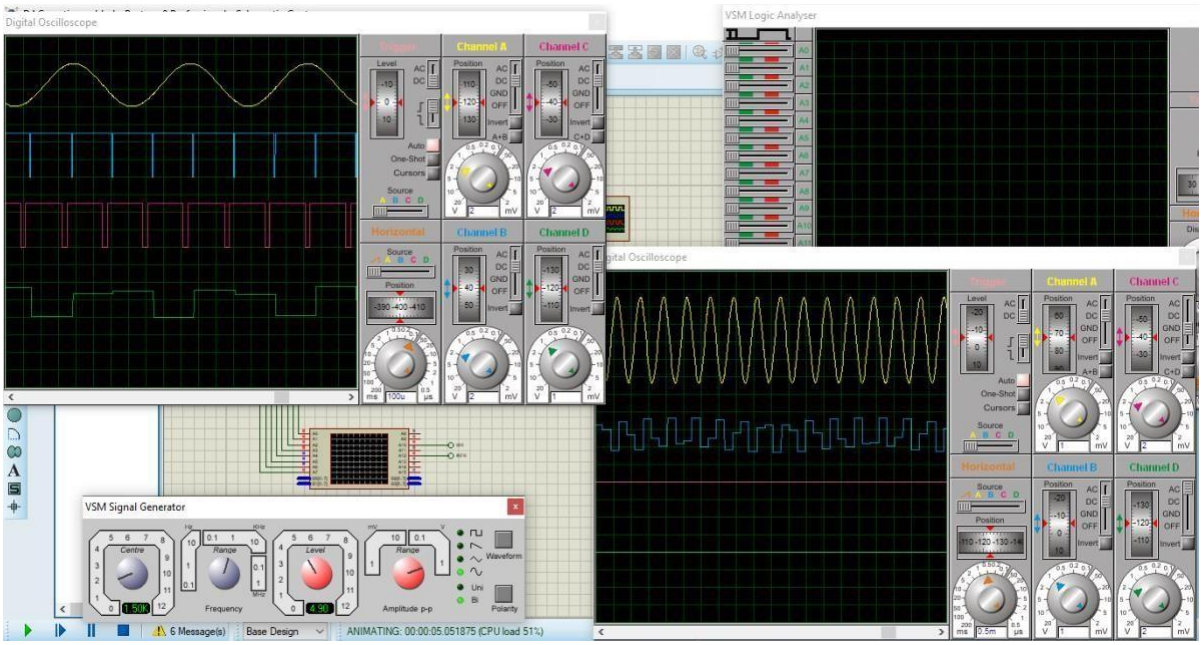

Figure 37: observation at 1.50 kHz input signal

At 1.5 kHz as in Figure 37, information content is decreased further and about only three samples are there in a full cycle of sinusoidal input. The Nyquist criterion is at its extreme and barely the signal appears to be like the input signal.

On further increasing frequency of input signal yields a distorted signal output that is non-recoverable so now the frequency of input is decreased ahead to show a nicely recoverable signal.

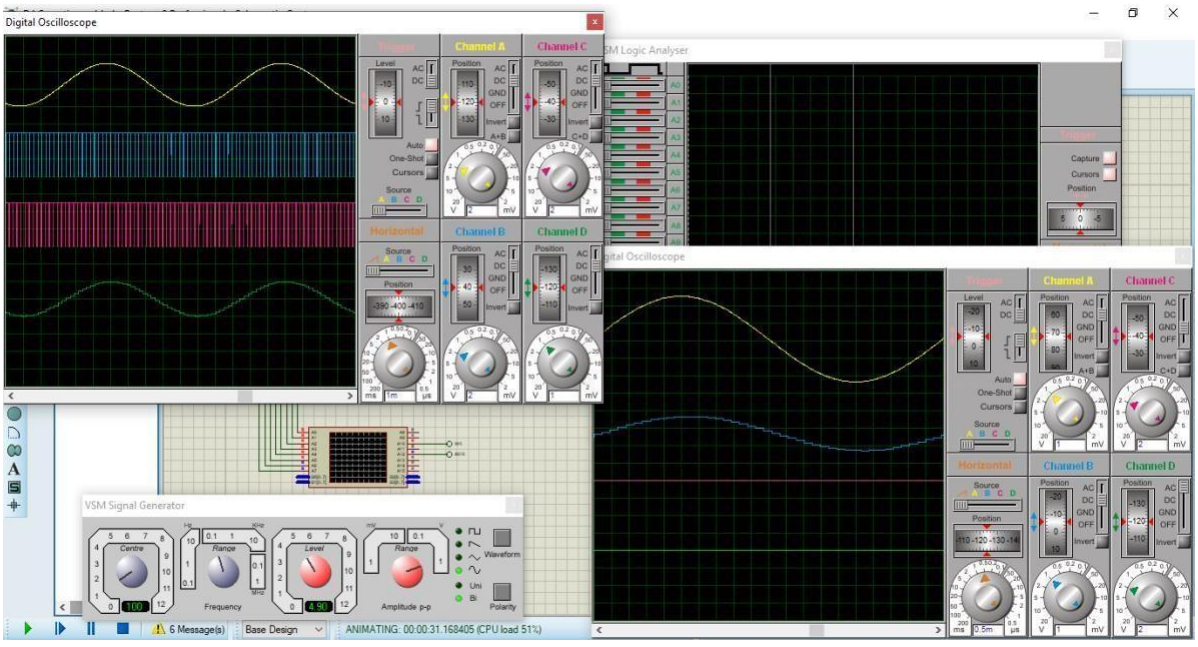

Figure 38: observation at 100 Hz input signal

But at a very relaxed frequency of 100 Hz as in Figure 38, the output signal is smooth since more sample are gather in a cycle (a cycle of input signal is represented by more than 40 samples). And it can be said that the signal contains the most information out of the input signal. With this it is seen that for a given sampling circuit, it is better to convert only those signal that have frequency much less than the Nyquist Criterion.

4.4.2 PCB and CAD Model

Using the schematic mentioned in Figure 33, the CAD models and PCB traces are made. The same software [10] that is used for simulation was used to make the PCB layout. The prepared schematic can be directly used as a schematic for PCB routing. All the components are integrated in a single board since effort is made to demonstrate a complete cycle of data conversion i.e, data acquisation, manipulation and presentation. This section contains the essential templates to make a PCB board. The microcontroller Arduino mega is also attached in the board. The prints are for the double-sided boards.

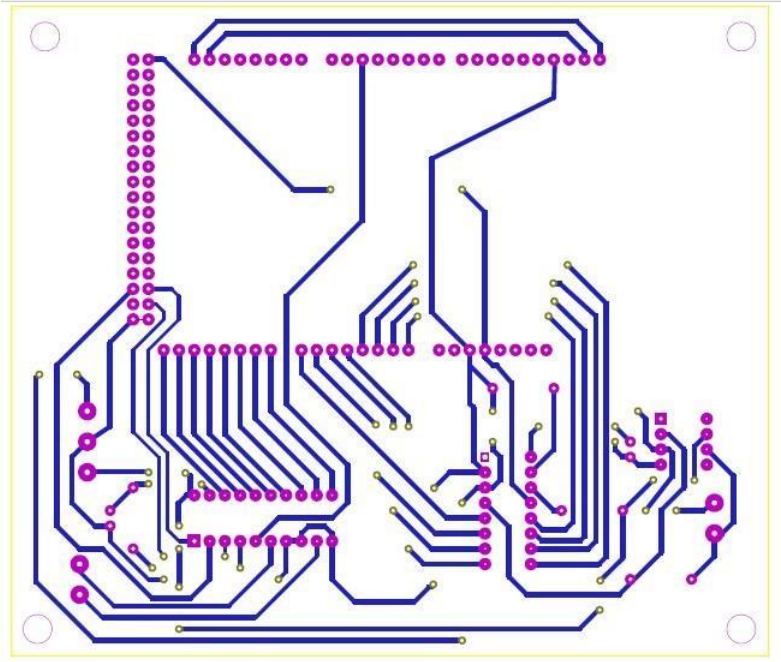

Figure 39: bottom trace (solder section)

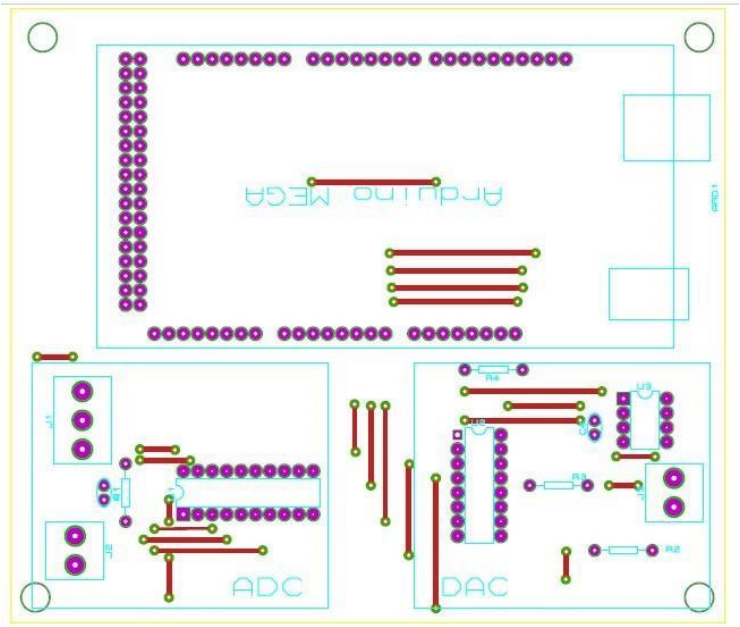

Figure 40: top trace (component section)

For more of the visualization of the board, the 3d view of the board is shown in Figure 41 and Figure 42. In the Figure 42, the red panel is supposed to be an Arduino mega board which is facing the bottom and is connected to the board with the header pins.

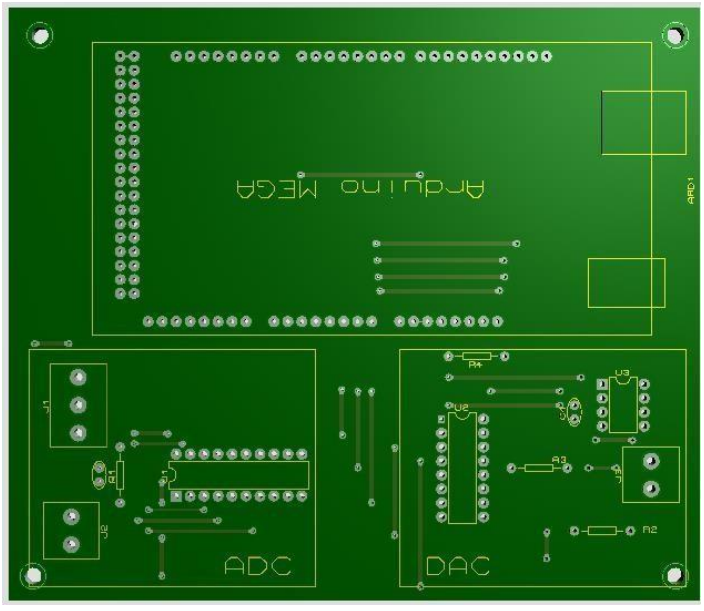

Figure 41: 3D view without components

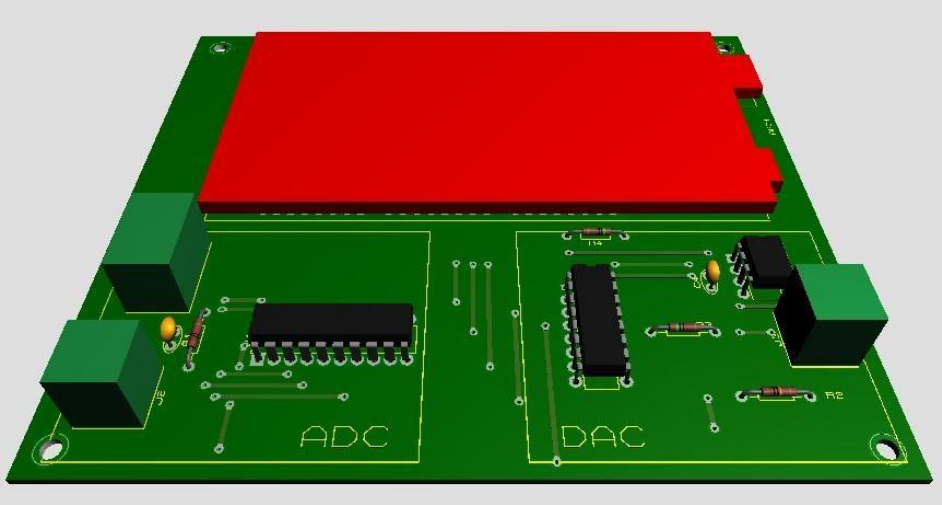

Figure 42: 3D view with components

5 Discussion and Conclusion

History shows that research, development, and design of data converters have been emphasized with high priority due to its wide applications. Realizing the importance of digital communication and digital computing; several scientist, engineer, researcher, and organization has spent their time, effort, and money to devise a better representation of signal and information, its storage and manipulation. Majorly, the development of data converters has started rapidly from the state of war (World Wars) to transfer intelligence from radio. And it has reached all the way to this era where large variety of method, application specific data converters (ADC and DAC) are easily available in market and large group of companies are manufacturing it for wide areas (for temperature sensing to 5G technology).

Regarding the observations, all the observation presented throughout this report is based on simulation, so it might not be the case when real chips and hardware come into play. But it is tried to make this simulation as applicable as possible when transferred for real construction including all the necessary preparation. Also, real hardware may be more prone to external interference, power, temperature, and other conditions. During simulation, limitations were different than when it would have been implemented in hardware.

The computer used for this simulation is equipped with a 2.8 GHz intel-i5 5^{th} generation running a windows 10 operating system. Even with this power it is difficult for the simulation to run at higher frequency signal. As a result, when higher frequency signal set in simulation, the simulation software crashed very often. So, it was necessary to find a maximum runnable parameter during the simulation which has been noted when such condition has occurred.

The whole system of conversion and application is demonstrated through simulation. A sinusoidal continuous signal is digitized, interfaced, and converted back to analog signal following the Nyquist Criterion. Properties of conversion were also discussed along.

In conclusion, data converters are important in electronics, computing and digitized world. So, further development in this field will continue.

6 References

[1] W. Kester, "A Brief History of Data Conversion," *IEEE SOLID-STATE CIRCUITS MAGAZINE*, 2015.

[2] dwellangle, "Quantization in ADCs," [Online]. Available: https://dwellangle.wordpress.com/2008/05/21/quantization-in-adcs/. [Accessed October 2020].

[3] D. Sheingold, Analog-Digital Conversion Handbook, Analog Devices, 1972.

[4] electronics-tutorial.net, "counter-type-adc," [Online]. Available: https://www.electronicstutorial.net/analog-integrated-circuits/data-converters/counter-type-adc/. [Accessed 12 September 2021].

[5] electronics-tutorial.net, "dual-slope-type-adc," [Online]. Available: https://www.electronicstutorial.net/analog-integrated-circuits/data-converters/dual-slope-type-adc/. [Accessed 12 September 2021].

[6] I. Ahmed, "A power scaleable and low power pipeline ADC using," 2004.

[7] Texas Instruments, "High-Performance Analog Products," *Analog Applications Journal*, 2011.

[8] tutorialspoint, "Signals Sampling Theorem," [Online]. Available: https://www.tutorialspoint.com/signals_and_systems/signals_sampling_theorem.htm. [Accessed October 2020].

[9] D. M. Alter, "Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller," Texas Instruments.

[10] Labcenter, "Proteus," [Online]. Available: https://www.labcenter.com/.

[11] Texas Instruments, "ADC080x 8-Bit, µP-Compatible, Analog-to-Digital Converters", 2009 (Revised 2015).

[12] National Semiconductor, "DAC0808 8-Bit D/A Converter," 1999.

[13] R. Hedayati, "A Study of Study of Successive Approximation Registers and Implementation of an UltraLow Power 10 bit SAR ADC in 65nm CMOS Technology," 2011.

[14] A. Kumar and D. Mehra, "Review of Different Types of Power Efficient Flash," *IJSR*, 2013.

[15] "History of SPICE," [Online]. Available: https://www.allaboutcircuits.com/textbook/reference/chpt7/history-of-spice/.

[16] B. Saima, A. Samiya, A. Suhaib and K. Vipan, "Analog-to-Digital Converters: A Comparative Study and Performance Analysis," in *ICCCA*, 2016.

[17] A. S. Kherde and P. R. Gumble, "A Review of Various Trends of Digital-To-Analog Converter with Performance Characteristics and Behavioral Parameters," 2013.

[18] C. Hugo and R. Sreeja, Implementation of 12-bit delta-sigma DAC, 2005.

[19] R. Tumati, "Digital to Analog Converter," 11 May 2006. [Online]. Available: https://ece.umaine.edu/wpcontent/uploads/sites/203/2012/05/ECE547_RaghuTumati.pdf.

[20] Maxim Integrated, "TUTORIAL SIGMA-DELTA ADCS," [Online]. Available: https://www.maximintegrated.com/en/design/technical-documents/tutorials/1/1870.html.

[21] RADIOSPARES, RADIONICS and A. ELECTRONICS, "Arduino Mega 2560," [Online]. Available: https://docs.rs-online.com/9ab3/0900766b80e8ba22.pdf.

[22] K. Cattermole, "History of pulse code modulation," *IET*, vol. 126, 1979.

7 Appendix

Code for Arduino

[code]

```
uint8_t data = 0x00; int
interrupt_pin = 2;

//////////////////// setting up pins, ports, and communication lines ////////////////// void
setup() {
  // initialize digital pin 13 as an output.
  DDRL = 0x00; // use port L as input
  DDRB = 0xFF; // use port B as output, for control lines
  DDRC = 0xFF; // use port C as output

  pinMode(50, OUTPUT);
pinMode(51, OUTPUT);   pinMode(52,
OUTPUT);   digitalWrite(50, LOW);
digitalWrite(51, LOW);   digitalWrite(52,
HIGH);
  // use interrupt on pin 2 of arduino mega for falling edge since active LOW
attachInterrupt(digitalPinToInterrupt(interrupt_pin), ISR_data_ready, FALLING);
Serial.begin(9600);          //          begin     serial     communication
start_conversion();
}

//////////////////// interrupt service routine does read operation/////////////////////
//////////////////// when interrupt occurs//////////////////////////////////////////// void
ISR_data_ready() {     data = read_data();    //
read data from port L
  Serial.println(data); // print data through serial terminal
  PORTC = data;          // write data on port C    start_conversion();
}

////////////////// signals the WR' pin of ADC0808 ////////////////////////////////////
bool start_conversion() {    digitalWrite(52, LOW);   digitalWrite(52,
HIGH);
  return true;
}

//////////////////// reads data from the portL ////////////////////////////////////////// uint8_t
read_data() {    uint8_t data = PINL;   return data;
```



```
}
```

```
//////////////////// manipulation function either relay the same signal /////////////////
//////////////////// or manipulated it before relaying ////////////////////////////////
//////////////////// not used now since this is done through interrupt routine //////////
void relay_update() {   start_conversion();   data = read_data();

  PORTC = data;
}

//////////////////// signal could be generated ///////////////////////////////////////
//////////////////// or emulated using different functions ////////////////////////////
//////////////////// not used ////////////////////////////////////////////////////////// int
delayy = 1; void emulated_update() {
  // below implementation generates a triangular wave
  for (int i = 0; i < 32; i = i + 8) {     PORTC
+=                      8;
delay(delayy);
  }
  for (int i = 32; i > 0; i = i - 8) {     PORTC
-=                     8;
delay(delayy);
  }
}

//////////////////// every statement in this function runs ////////////////////////////
////////////////////  infinitely  (infinite  loop)////////////////////////////////////  void
loop() {
  // nothing to be placed here since interrupt does all the operations  }

[/code]
```