Miska Heino

Envelope Generator for Analog Synthesizer

Metropolia University of Applied Sciences
Bachelor of Engineering
Degree Program of Electronics
Bachelor’s Thesis
14.11.2022

Tiivistelmä

Author:	Miska Heino
Title:	Verhokäyrägeneraattori analogiseen syntetisaattoriin
Sivumäärä:	25 sivua + 1 liite
Aika:	14.11.2022
Tutkinto:	Insinööri (AMK)
Tutkinto-ohjelma:	Sähkö- ja automaatiotekniikka
Ammatillinen pääaine:	Elektroniikka
Ohjaajat:	Yliopettaja Heikki Valmu

Työn tarkoituksena oli suunnitella verhokäyrägeneraattori analogiseen modulaarisyntetisaattoriin. Verhokäyrägeneraattori on tarkoitus liittää osaksi henkilökohtaista syntetisaattoriprojektia. Piirilevyn suunnittelu tehdään myöhemmin.

Työssä on myös lyhytsanainen kertomus syntetisaattoreiden synnystä sekä selitys analogisen syntetisaattorin perusteista. Suunnitellun verhokäyrägeneraattorin toiminta on kuvailtu yksityiskohtaisesti käyttäen apuna piirikaavioita.

Ohjausjänniteiden vaikutus ulostuloon mitattiin oskilloskoopilla. Mittaustulokset vaikuttavat lupaavilta, mutta kytkentää ei ole vielä perusteellisesti testattu muiden syntetisaattorin osien kanssa.

Tuloksena on muunneltu versio vanhemmasta piiristä, joka perustuu 555-ajastimen käyttöön. Lisäksi piiriin kehitettiin jänniteohjaus, joka mahdollistaa parametrien säädön ulkoisella jännitteellä. Se toteutettiin ohjaamalla JFET-transistoreiden läpi kulkevaa virtaa.

Avainsanat: syntetisaattori, elektroninen musiikki

Abstract

Author:	Miska Heino
Title:	Envelope Generator for Analog Synthesizer
Number of Pages:	25 pages + 1 appendix
Date:	14 November 2022

Degree:	Bachelor of Engineering
Degree Programme:	Electronic and Automation Engineering
Professional Major:	Electronics
Supervisors:	Heikki Valmu, Principal Lecturer

The purpose of this thesis work was to design an envelope generator circuit for an analog modular synthesizer. The device was designed to be added to a personal synthesizer project. Circuit board layout of the schematic will be made later.

The thesis contains also a brief history of the birth of synthesizers and basic principles of an analog synthesizer. Operation of the designed envelope generator circuit is explained in detail with schematic diagrams.

Measurements illustrating the effects of the control signals were made with an oscilloscope. The measurements are promising, but the circuit is not yet thoroughly tested with a full synthesizer system.

The result is a modified version of an old circuit based on the 555 timer. Voltage control was also added to the circuit to allow parameters to be controlled with an external voltage. It was implemented by controlling currents of junction field-effect transistors.

Keywords: Synthesizer, Electronic Music.

Contents

List of Abbreviations

CV: *Control Voltage.* A signal that controls a parameter of a module

EG: *Envelope Generator*.

JFET: *Junction Field-Effect Transistor.*

LFO: *Low frequency Oscillator.* An oscillator operating below audio frequencies.

OTA: *Operation Transconductance Amplifier.*

VCR: *Voltage Controlled Resistor.*

1 Introduction

The purpose of this thesis work was to design an envelope generator, henceforth referred as the EG, for an analog modular synthesizer. The result is a schematic diagram, measurements and analysis of the device. The end product can be used to make a layout for a circuit board which can be added to any modular synthesizer complying with the Eurorack standard.

A driving concept of modular synthesizers is voltage control. Many components of the synthesizer have inputs for control signals which can alter the components parameters. An EG creates such a signal, typically to control the gain of an amplifier.

The design will have conventional features of an EG and voltage control as an extra feature. Core of the design will be largely based on circuits available from the internet.

Motivation for the project is personal interest in synthesizers. Out of all the possible synthesizer components, EG was chosen for the topic of this thesis work to supplement my home-made modular synthesizer.

2 Synthesizers

Synthesizer is a broad term that can mean many different things not only in general, but also in the scope of audio synthesis. For example a frequency synthesizer is also a component used in radio technology to generate different frequencies [1].

In the scope of this paper synthesizers are electronic musical instruments which create and shape sounds. The function of a synthesizer can vary from a full-featured professional music instrument to a tiny gadget making noise. It can be a physical device or a piece of software. Usually synthesizers have a piano-like keyboard or a step-sequencer to play the notes with. Step-sequencer is a programmable device for creating rhytm patterns. Additionally, a digital audio workstation (DAW) such as Pro Tools or Ableton can be used to send the notes to the synthesizer via MIDI-interface.

2.1 History of Synthesizers

In the first half of the 20th century various items were invented which can be seen as predecessors to synthesizers. Probably most famous such item is the theremin created in 1920 by a soviet inventor Leon Theremin [11]. Theremins are still being manufactured and sold in 2022 [12].

In New York in 1960 Harald Bode, introduced his ”Audio System Synthesizer” at Audio Engineering Society convention. His device was the first modular synthesizer ever created. Harald Bode’s synthesizer was an inspiration to the Moog synthesizer. [13.]

The beginning of commercial analog synthesizers can be traced back to R. A. Moog company. Their first model was first sold in 1964. The Moog synthesizer was a modular design with components like oscillators, filters, envelope generators, noise generators and ring modulators. To make a sound, the instrument needed to be properly patched. The design was inspired by how some electronic music artists made compositions with electronic test equipment and other lab instruments.

During that time the modular synthesizer was not fit for mass production because its complexity and obscurity made it hard to sell for musicians. During the late 1960s, engineers at Moog came up with the idea of a more simpler and portable synthesizer to access a larger customer base. They found out that they would always patch the modular synthesizer in the same way, so they made the components hard-wired. As a result of their new innovations the Minimoog was released in 1970 being the first ever synthesizer to be sold in a retail store. The Minimoog had a built-in keyboard for playing the notes and it could be carried easily which appealed to touring musicians. [2.] Minimoog has surely made an enormous impact on pop and rock music and introduced the synthesizer to a wider audience.

2.2 Eurorack

Today the most popular hardware modular synthesizer format is the Eurorack, originally specified in 1995 by Doepfer Musikelektronik and used in the A-100 modular system [3]. It is based on the Eurocard standard which was used in industry to standardize circuit board sizes [4].

Eurorack has been adopted by many small and independent companies with over 500 vendors and over 13000 modules listed on the modular synth database modulargrid.net [3].

The Eurorack specification is referenced from the A-100 technial details provided by Doepfer [5]. A full sized modules panel height is 3 U or 133.5 mm.

Electrical specifications of the Eurorack are the following:

- Supply voltages are +12 V, -12 V and optionally +5 V.

- Frequency of oscillators and filters have 1 Volt/octave tracking.
- Gate signal is a binary 0/+5 V
- Modules are triggered with a rising edge of the gate signal
- Audio signals are typically 10 V peak-to-peak.
- LFO signals are typically 5 V peak-to-peak.
- Envelope signals are from 0 to +8 V

Many of the specifications can be taken as a guideline rather than strict definitions. The modular synthesizer is an instrument of experimentation and should imply as few limitations to the user as possible.

2.2.1 Connectors

Modules are connected to the power supply or a bus board with ribbon cables. Connectors on the power supply side are dual-in-line 16 pin headers with 2.54 mm spacing. In addition to the supply voltages, one gate and one CV signal can be carried with the connector. The headers on the modules side usually have 10 pins. Some modules that demand the +5 V supply voltage, internal gate or internal CV have 16 pin headers. Figure 1 shows the pinout for both of the connectors. The synthesizer modules are interconnected with 3.5 mm mono cords.

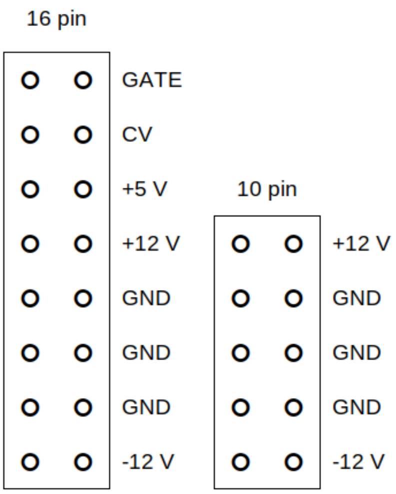

Figure 1: Euroracks power connectors

2.3 Subtractive Synthesizer

There are many methods to sound synthesis. The modular synthesizer traditionally relies on subtractive synthesis, in which the oscillator output is reduced or boosted with a filter, as well as amplitude modulation (tremolo). Frequency modulation is also present, in which the carrier oscillator is modulated by a modulator oscillator to add more frequency components into the carrier signal.

Various circuits like oscillators, filters, envelopes, amplifiers and step-sequencers are used in an analog synthesizer. In addition to audio signals, low frequency and DC control signals are also present in a synthesizer. These control signals are used to modulate and control different components of the synthesizer. Regular targets for modulation are oscillator frequency, amplifier gain and filter cutoff frequency.

A simplified block diagram of a subtractive synthesizer is seen in figure 2.

Oscillators commonly output basic functions such as sine, triangle or pulse. The frequency of the Oscillator is controlled with a voltage generated from the keyboard. A common scheme in voltage control is 1 V/octave tracking, where the oscillator frequency is increased one octave for 1 Volt increase in the control voltage. This scheme was already present in the Minimoog.

To generate more complex waveforms, the signal is fed into a resonant filter. The filter cutoff frequency can usually be modulated and has the same 1 V/octave tracking scheme as an oscillator. Some filters have such high levels of resonance that they self-oscillate at the cutoff frequency, effectively making them also function as sine wave oscillators.

Finally, in order to have varying levels of volume, the signal is fed into an amplifier which is controlled by an EG. The EG is usually triggered with a gate signal from a keyboard or a sequencer. Most simple EG’s only have attack and release parameters. By far the most common type of EG has four parameters, namely attack, decay, sustain and release. These type of EG’s are usually referred simply as an ”ADSR”.

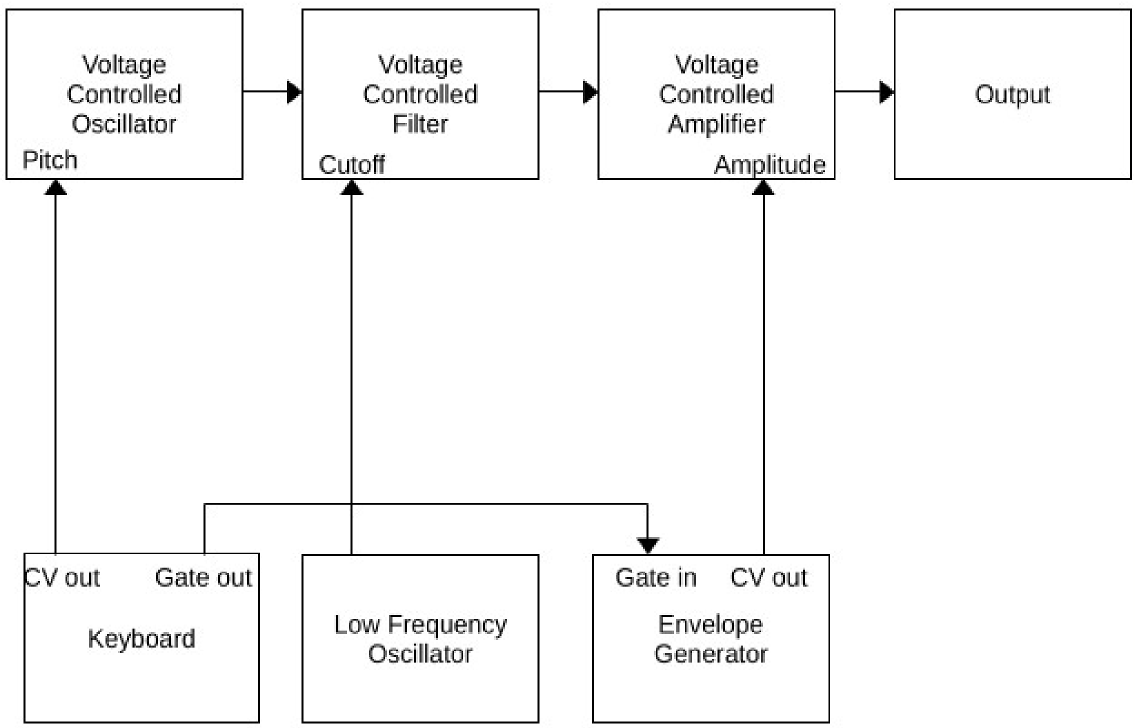

Figure 2: A Simple Synthesizer Block Diagram

3 Envelope Generator Operation

The EG is triggered with the rising edge of a gate signal. It then goes through four phases called: attack, decay, sustain and release. The output of the device consists of line segments illustrated in Figure 3.

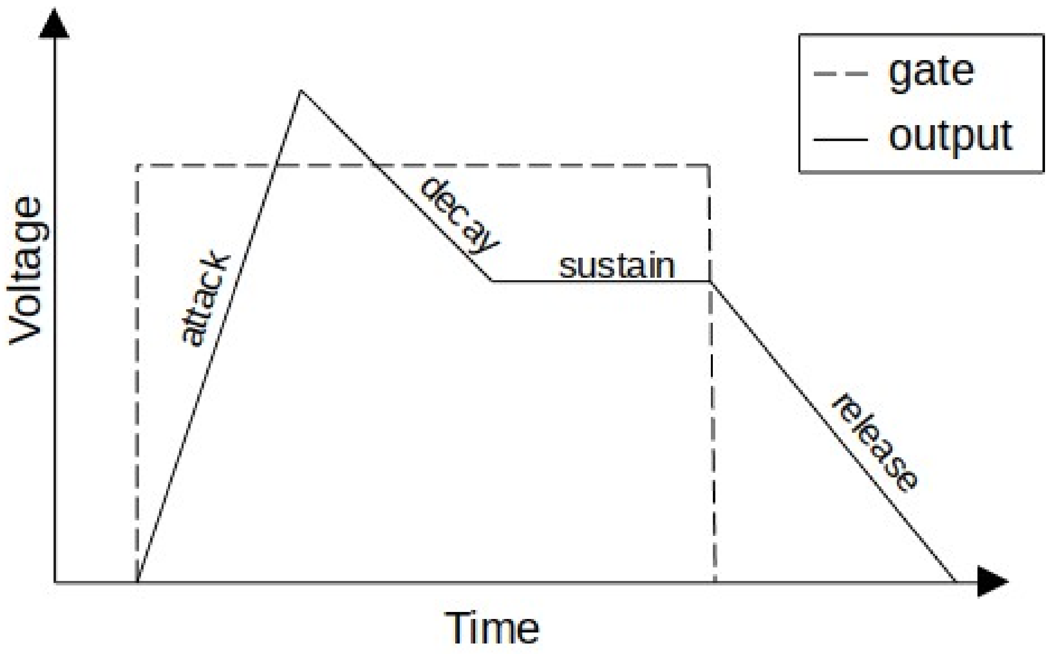

Figure 3: Envelope generators full cycle

3.1 Output

The voltage of the output is the buffered voltage of C2 which varies from 0 to 8 Volts. C2 voltage is essentially controlled by a 555 timer in monostable mode. The output level magnitude is visualized by an LED.

3.2 Gate

The EG can be triggered with a push button or an external gate signal. The external gate signal can vary depending on the source. To ensure correct operation of the device, the gate signal levels used throughout the circuit should be consistent. To achieve this, the external gate signal is fed into a Schmitt trigger which turns it into a 0 to +12 V signal. The processed gate signal is fed into a high-pass filter and inverted to create a short negative pulse that triggers the 555 and starts the attack phase.

3.3 Attack Phase

Once triggered the 555 output pin goes high. The capacitor C2 is now starting to charge through a diode and a JFET VCR connected to the 555 output. The sustain voltage reference is pulled up by R27, reverse biasing D4 so that the capacitor cannot discharge during the attack phase.

3.4 Decay and Sustain Phase

Decay phase starts when the voltage over C2 reaches the threshold voltage of the 555 internal comparator (8 Volts). 555’s pin states change so that the output pin goes low and discharge pin connects to ground through an internal transistor. As a result of the discharge pin now connected to ground, R27 and Q7 form a voltage divider setting the sustain voltage which allows C2 to discharge through Q6 until reaching the sustain level. The purpose of the diode in series with Q6 is to prevent charging of C2 from the sustain voltage reference point. In sustain phase C2 voltage is kept constant at the level of the set reference voltage. Sustain phase lasts as long as the gate is high.

3.5 Release Phase

When the gate goes low, D5 becomes forward-biased allowing C2 to discharge through the release VCR. Release phase can start at any point of the cycle if the gate signal goes low, skipping any phases in between. If the gate goes low before the start of sustain phase, C2 can also discharge through the decay VCR.

4 Design

4.1 Defining Features

Different ideas were pondered when specifying the features of the device. Voltage control was a desired feature from the get-go, as voltage controlled modules are usually the most interesting and versatile ones, with a lot of room for experimentation and finding interesting sounds.

An example of CV utilization is when creating a hi-hat drum sound by running white noise through an EG modulated amplifier, the result can be robotic and dull, but if in addition the release parameter of the EG is modulated with a random voltage, the sound is more organic and human like.

Adding an extra phase to the common ADSR composition was considered mainly to avoid genericity. The first prototype of the device had a hold-phase which held the output high for set amount of time before the start of decay phase. Hold was rather quickly discarded, because it did not feel that useful compared to the increased part count. Also the insight that almost an identical effect as the hold function can be achieved by modulating decay or sustain parameters with a sequencer or another EG weighted on the decision to abandon the fifth phase and stick with four.

The core design of the EG is based on a circuit by Jonathan Jacky [6, 137]. The circuit was further improved by Yves Usson in their Yusynth ADSR circuit [7]. Supply voltages and other voltage levels of the EG will comply with Eurorack standard. Schematic snippets in this chapter illustrate parts of the full schematic (See Appendix 1).

4.2 Power Supply

The module is powered by +12 / -12 Volts provided by the Eurorack system power supply. Bypass capacitors are placed near the IC power pins like in Figure 4. This is common practice in circuits to reduce noise.

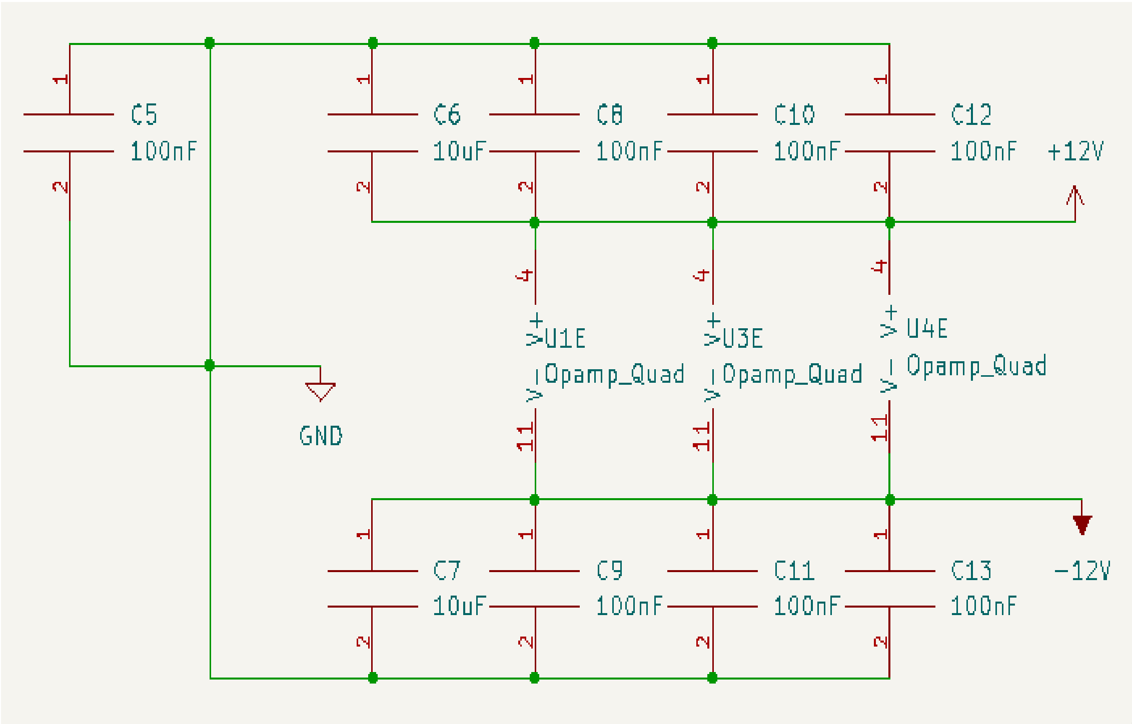

Figure 4: Bypass Capacitors

4.3 Voltage Control

When approaching the task of adding voltage control to the circuit, the first idea to emerge was to replace the potentiometers with voltage controlled resistors, an idea which worked fine. Also it meant that there was no need to heavily re-design the circuit.

The way the voltage control is implemented with the JFETs is not the most conventional way to use them. It is something I came up with on my own and I could not find any similar circuits online. Hopefully it will give original characteristic to the EG.

Before settling with the JFET's, experiments with LM13700 operational transconductance amplifiers were conducted. The LM13700's have very much potential, but were discarded eventually. Reasons for this choice was that the part count increased dramatically compared to the JFET solution.

4.3.1 Junction Field Effect Transistor

Voltage control is implemented by controlling the drain current I_D of an N-channel JFET. 2N5457 N-channel JFET was selected because of local availability, but a device with larger currents would be more suitable.

To control the magnitude of I_D, gate to source voltage V_{GS} is varied between V_S and $V_{GS(off)}$. The drain current can be approximated with equation (1), where I_{DSS} is the zero-gate voltage drain current and $V_{GS(off)}$ is the gate-source cutoff voltage, a value of V_{GS} which causes $I_D = 0$ mA. [10.]

$$I_D \equiv I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (1)$$

As can be seen the relation of V_{GS} and I_D is parabolic which might affect the feel of the EG but does not break the devices operation.

4.3.2 2N5457 Characteristics

I_D is also dependent on the drain-source voltage as can be seen typical drain characteristic curves in figure 5, cited from the device's datasheet [8]. I_D changes linearly when V_{DS} is small. This linear region is called the JFET's ohmic region [10]. The JFET's in the decay and release circuits operate in this region when the capacitor voltage falls close to sustain voltage in the decay phase and zero in the release phase. The effect is further discussed in chaper 5. Ideally in this application the JFET should be in saturation so that the current through it is only dependent on V_{GS}.

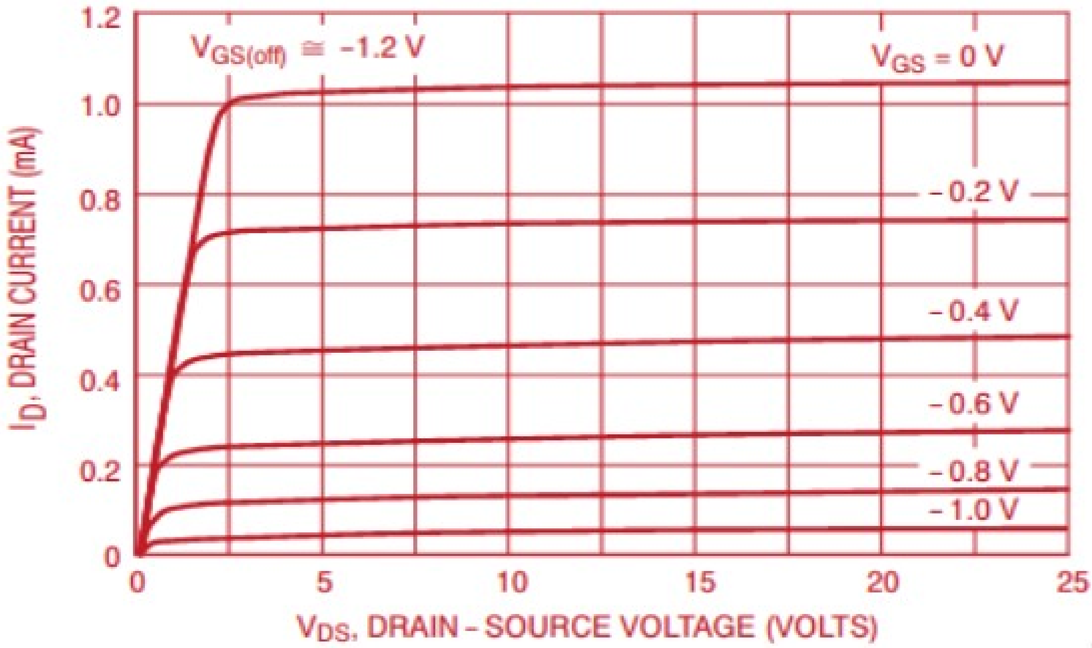

Figure 5: Typical Drain Characteristics for a 2N5457 [8].

According to the 2N5457 datasheet, the cutoff voltage can vary between -0.5 and -6.0 Vdc. To get a rough approximation of V_{GS} the current I_D was measured and V_{GS} increased till the current diminishes to zero or less than 0.01 mA since the Fluke 75-3 used in the measurement has a resolution of 0.01 mA [9]. The 2N5457's used in the prototype all have V_{GS} of approximatxely -1 V.

The maximum current achievable with the device was measured with gate shorted to source and V_{DS} above the linear region (+12 V). The result was 1.55 mA. Equation (2) is for the voltage of a capacitor. Capacitor charging time can be solved substituting values and rearranging it to equation (3).

$$V(t)=V(t_0)+\frac{1}{C}\int_{t_0}^{t} I(\tau)d\tau \qquad (2)$$

The time to charge a 10 uF capacitor with 1.55 mA from 0 V to +8 V should then take 51.6 ms. This time is quite long if a fast envelope is needed. It is a good idea to add a switch and another smaller capacitor to the circuit so it can be operated in fast or slow mode.

$$t=\frac{VC}{I} \qquad (3)$$

4.3.3 VCR Circuits

Some circuitry is required to process the control voltage for the gate of the JFET. Circuit for controlling the attack time is seen in Figure 6. Decay circuit follows the same principle, with only difference being that the capacitor C2 is on the drain side of the JFET. The inverting CV mixer is used for all four CV inputs.

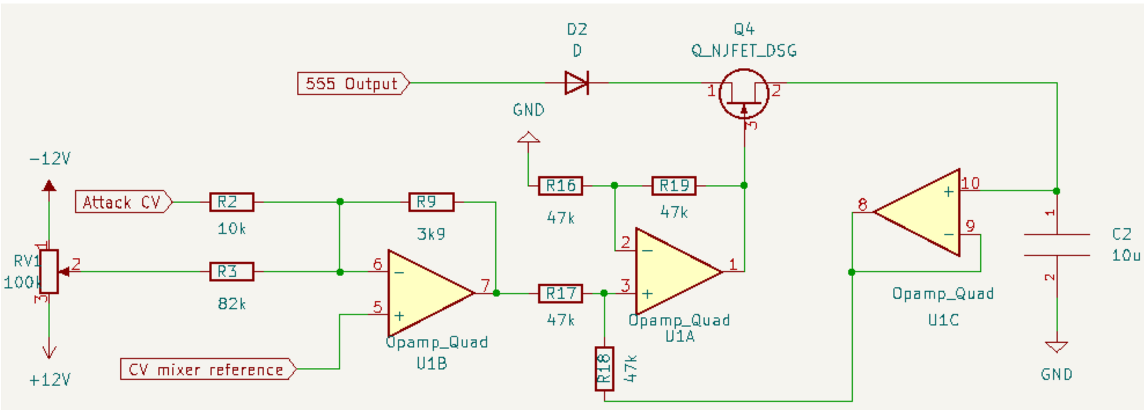

Figure 6: Attack Circuit

C2 is charged through D2 and Q4 when 555 output pin is high. D2’s purpose is to prevent the capacitor discharging to the output pin.

U1B and resistors R2, R3 and R9 form an inverting summer amplifier which transforms the CV to range -1.2...0 V which is near the JFET's gate's range of control. External CV is fed into the device through R2. RV1 is a potentiometer to be mounted on the panel which is used to set the attack time when no external voltage is applied. The gain for this voltage is approximately 0.05 corresponding to minimum output of -0.6 V when input is at +12 V.

Output of U1B is offset with 0.6 V by setting the non-inverting input to -0.6 V to achieve the desired range of output. The offset voltage is created with a resistor divider and buffered with an op-amp voltage follower. All JFET's in the prototype had the same cutoff voltage so the same reference point could be used in all cases.

For the external CV, a smaller input resistor was chosen to increase its gain. The choice is purely a matter of user preference. I felt that the response is more satisfying this way. A potentiometer configured as a voltage divider could also be used to control the amplitude of the incoming CV signal.

U1A together with resistors R16, R19, R17 and R18 form a non-inverting summer amplifier which is used to sum the control voltage signal with the source voltage of the controlled JFET. The amplifier has unity gain such that $V_{out} = V_1 + V_2$. JFET's source voltage is fedback with a buffer U1C to prevent the capacitor discharging through output of U1B.

4.3.4 Release VCR

During the release phase the gate is low, so the source voltage of the release JFET is at ground potential. No feedback is thus needed to keep V_{GS} within the desired boundaries. Only the inverting summing amplifier is needed to apply voltage to the gate of JFET as seen in figure 7. The inverting summer circuit is identical to the attack circuit.

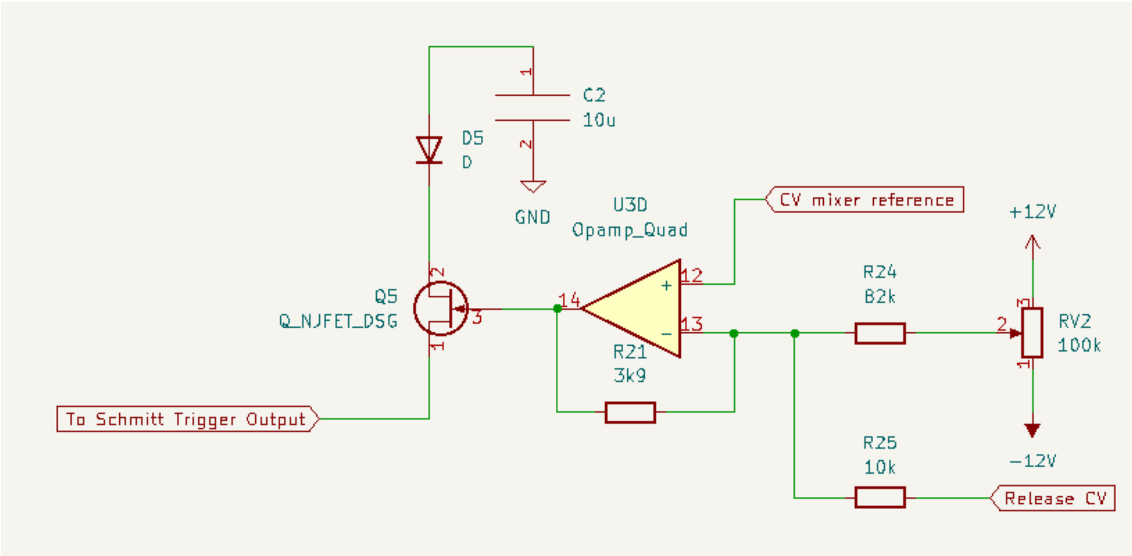

Figure 7: Release Circuit

4.3.5 Decay and Sustain Circuits

Decay circuit is identical to the attack circuit. In the decay phase C2 discharges to a voltage set by a voltage divider consisting of Q6 and R27. The resistor is connected to +12 V and the JFET drain is connected to 555 discharge pin. While the discharge pin is floating the sustain voltage is +12 V and C2 cannot discharge because D4 is reverse-biased. Sustain voltage is set when the discharge pin connects to ground at the start of decay phase. The JFET gate is controlled by a voltage from the inverting CV mixer similarly as the other JFET's. Schematics of the decay and sustain circuit is seen in figure 8.

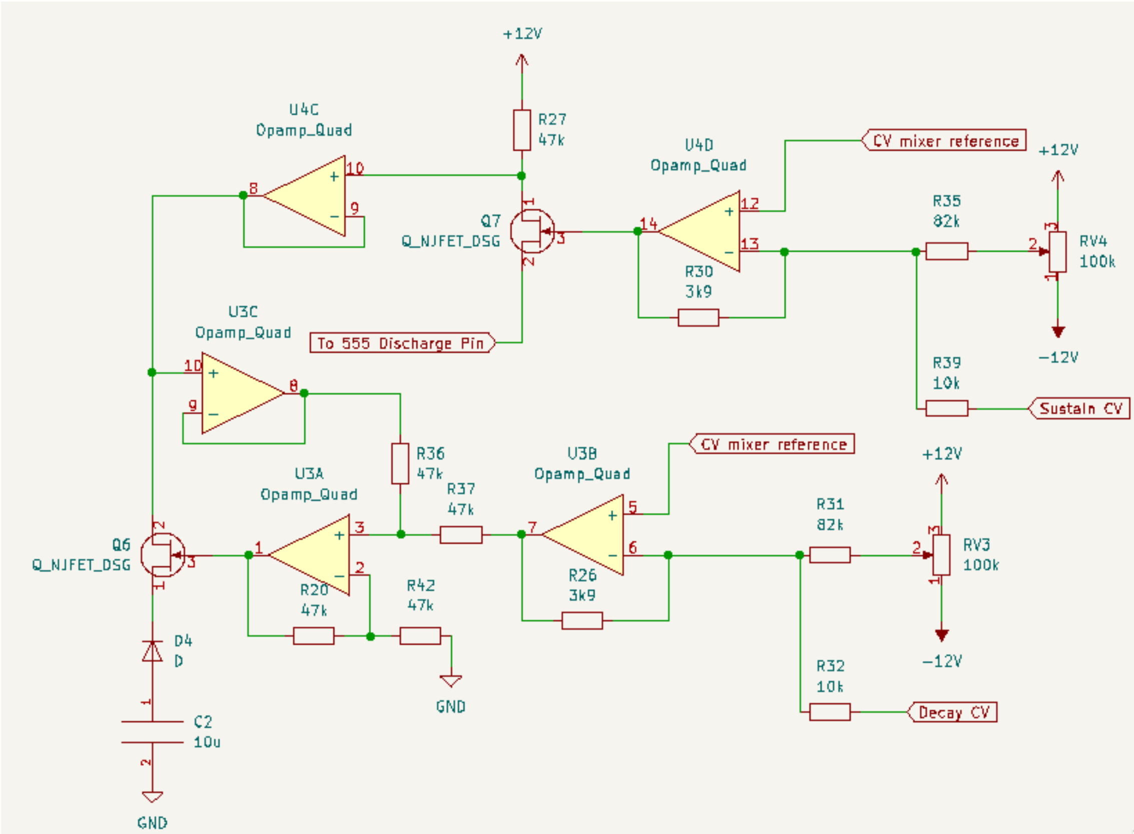

Figure 8: Decay and Sustain Circuits

4.4 555 Timer

Heart of the EG is the 555 timer chip configured in monostable mode. To trigger the 555, a falling pulse is generated from the gate signal with a passive low-pass filter and a transistor inverter. Capacitor C2 is charged when 555 output is high. When the capacitor voltage rises to 2/3 Vcc, threshold pin senses that voltage and resets the output of the 555 and connects the discharge pin to ground through an internal transistor. A 10nF bypass capacitor is connected to the control voltage pin to eliminate AC noise.

4.5 Schmitt Trigger

To make the EG accept a wider range of external gate signals and to provide a clean signal for the use of the EG, a schmitt trigger is used to receive external gate signals. The schmitt trigger is implemented with 2 npn-transistors and 3 resistors. The Schmitt trigger used in this design is the same as in the Yusynth ADSR. [7.]

4.6 LED Driver

The LED driver in Figure 9 consists of an op-amp, a general purpose diode and a resistor. Its purpose is to keep the LED forward biased during the whole cycle of the envelope.

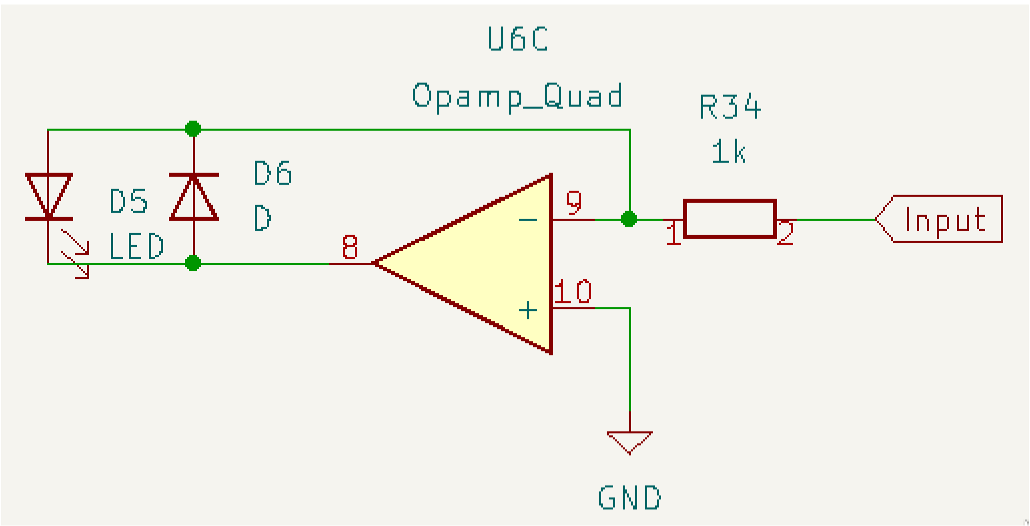

Figure 9: LED Driver Circuit

When the input voltage is higher than the voltage of the non-inverting input (0 Volts) the output of the op-amp is the inverse of the LED's forward voltage drop, effectively making the inverting output be 0 Volts. The resistor and input voltage sets the current running through the LED. If the input somehow goes below 0 Volts, the diode protects the LED from reverse-biasing and possible breakdown. The same LED driver is also used in the Yusynth ADSR [7].

5 Measurements

Current draw from the power supply is 31.3 mA from +12 V and 26.1 mA from -12 V and it is the same when the EG is triggered.

A probe with 10x attenuation was used to measure the output in all the images. Output with arbitrary settings in Figure 10. The blue trace is the gate signal. Traces are also offset to fit in the picture. The smooth edges at the end of decay and release phase are results of the JFET's operating at the ohmic region.

Figure 10: Envelope generators full cycle measured with an oscilloscope

With the 10 uF capacitor, minimum attack time is approximately 52 ms and minimum release time from 8 V to ~0 V is 64 ms

5.1 CV Modulation

The next series of images will give an example of the effects of an external control voltage to the four parameters. The sine wave signal from a function generator is seen in blue. When the controlling sine wave is high, the slope of the output is decreased and vice versa.

Modulating the attack parameter with a sine wave yields results seen in Figure 11.

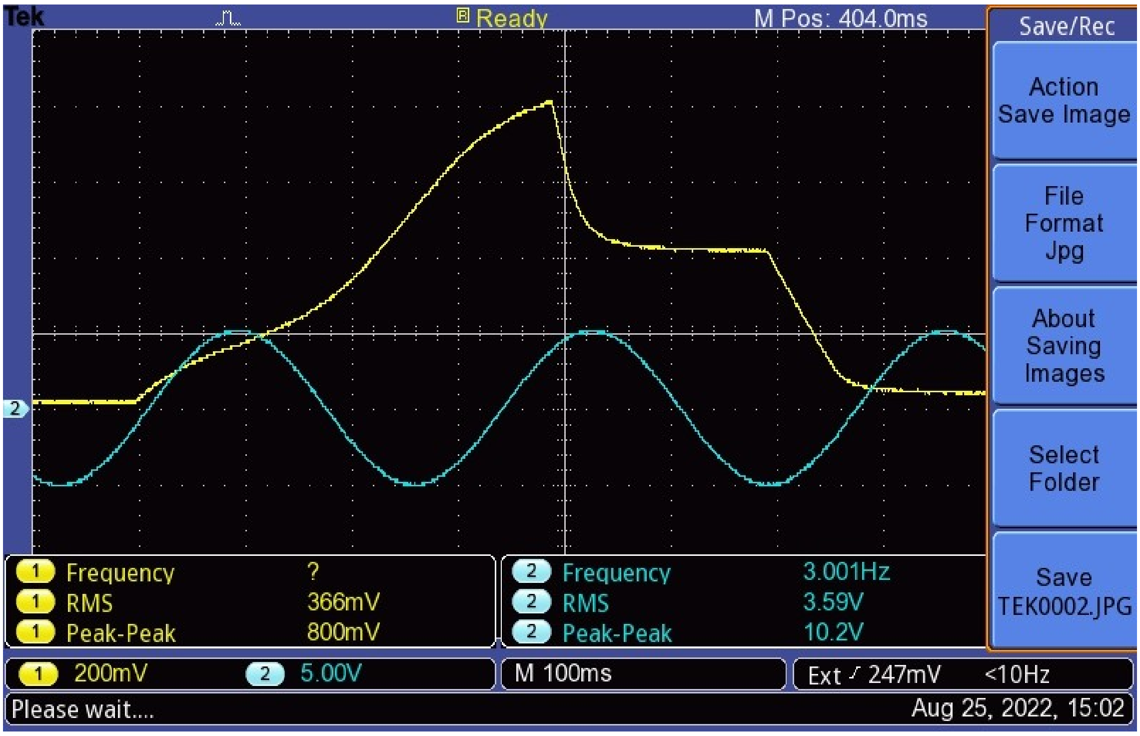

Figure 11: A sine wave oscillator modulating the attack parameter

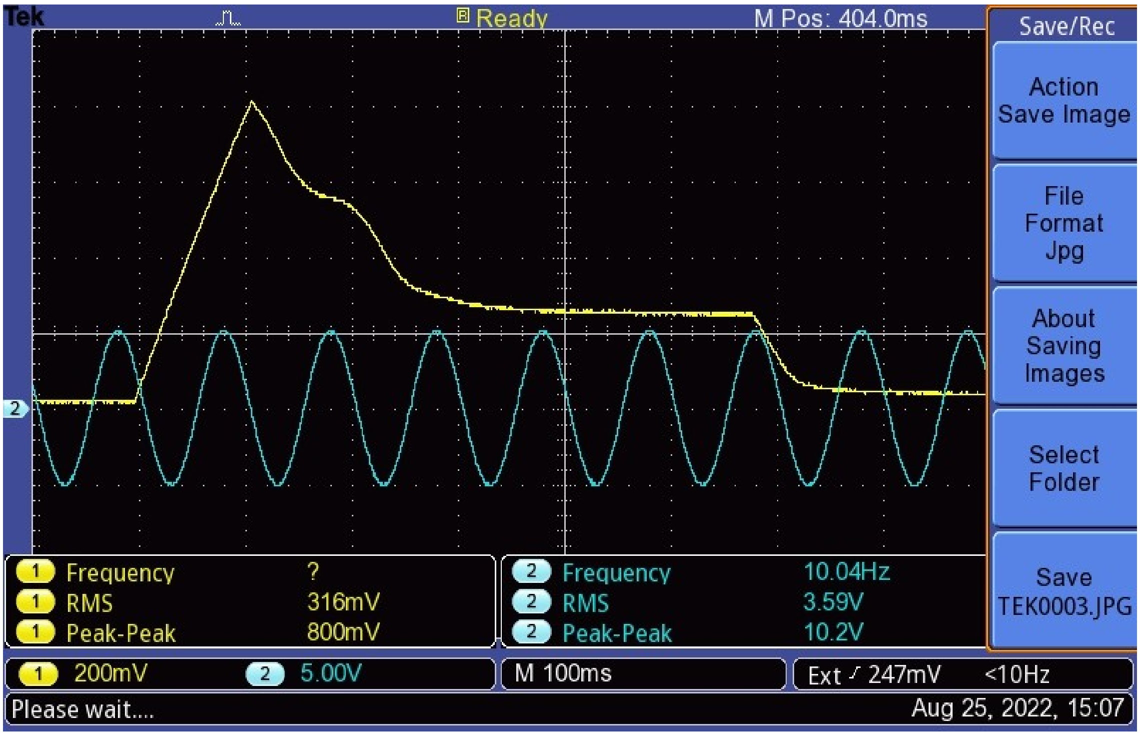

Figure 12: A sine wave oscillator modulating the decay parameter

In figure 12 a 10 Hz sine wave is modulating the decay parameter.

The sustain level is modulated in Figure 13. The cycle can be seen to consist of attack and three decay and three sustain phases instead of the regular ADSR composition. The release phase is basically non-existent because the sustain level goes down to zero. Using some type of control circuit the behaviour of the EG can be set to have a hold phase.

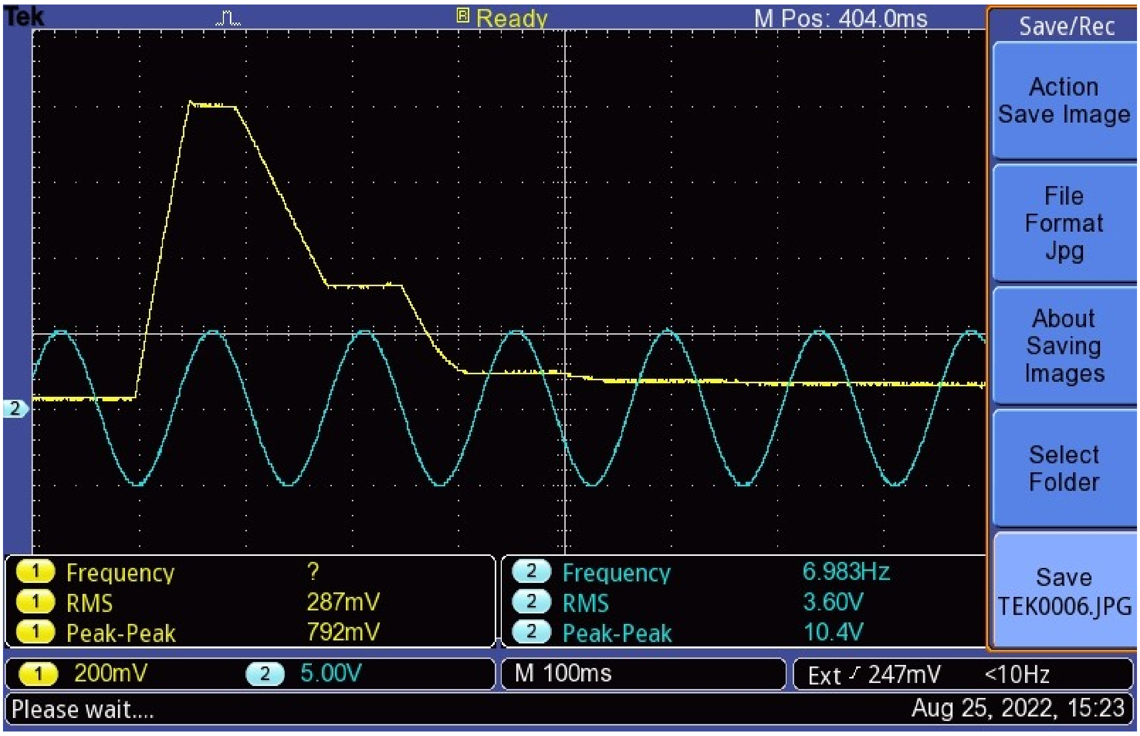

Figure 13: A sine wave oscillator modulating the sustain level

Figure 14 shows the release time modulated by a sine wave.

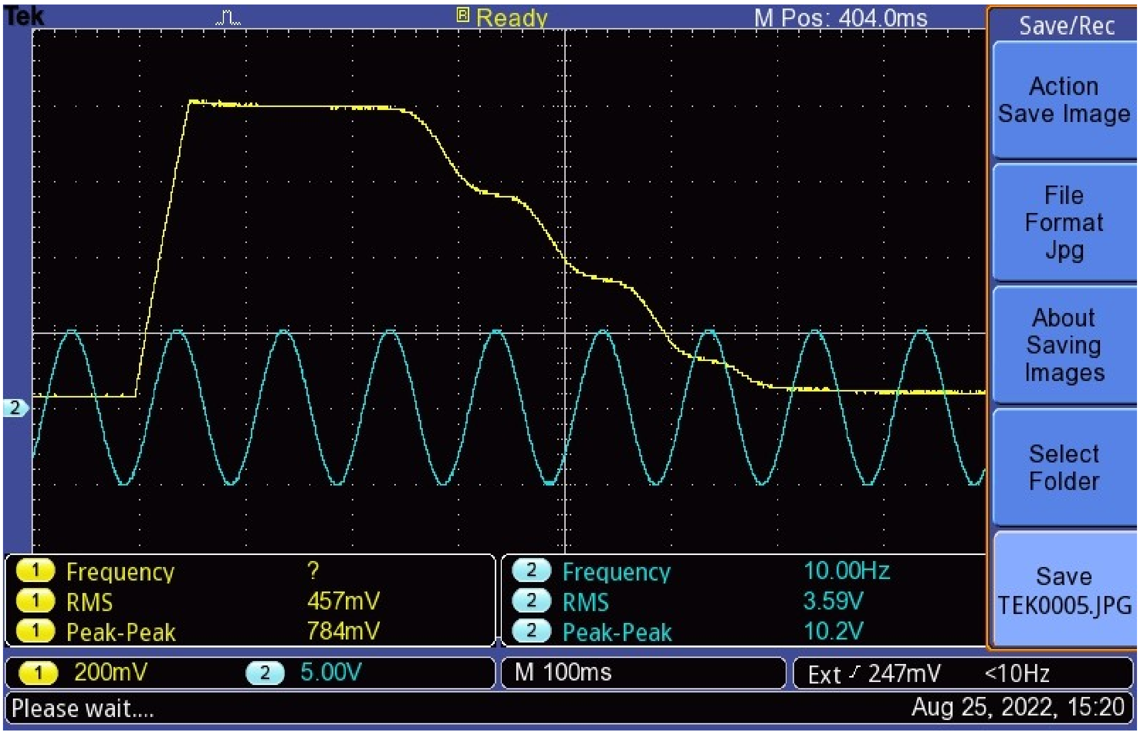

Figure 14: A sine wave oscillator modulating the release parameter

6 Conclusions

Purpose of the project was to design an envelope generator circuit. The output of the device was measured with an oscilloscope, but the possibilities and worth of the results can only be fully understood after building and adding it to the synthesizer and making sound with it.

The design could be further improved and I probably will do that before building it. Repurposing the output buffer op-amp to redesign the schmitt trigger could save room from the circuit board.

Designing a part of musical instrument is probably more forgiving than many other devices when considering stability. Noise or distortion is usually considered unambigously unwanted in electronics. In music certain type of noise can yield interesting results. It all comes down to how the instrument sounds like.

References

1 Frequency Synthesizer [Internet]. [cited 2022 Oct 15]. Available from: https://en.wikipedia.org/wiki/Frequency_synthesizer

2 Pinch TJ, Trocco F. Analog days. Cambridge (US), Massachusetts (US) and London (UK): Harvard University Press; 2002. 368 p.

3 Modular Grid [Internet]. [cited 2022 Oct 15]. Available from: https://www.modulargrid.net/e/modules/home

4 Eurocard [Internet]. [cited 2022 Oct 15]. Available from: https://www.techopedia.com/definition/19207/eurocard

5 Technical Details A-100 [Internet]. [cited 2022 Oct 15]. Available from: https://doepfer.de/a100_man/a100t_e.htm

6 Electronics Magazine [Internet]. [cited 2022 Oct 15]. Available from: https://worldradiohistory.com/Archive-Electronics/80s/80/Electronics-1980-09-11.pdf p 137.

7 Yusynth ADSR [Internet]. [cited 2022 Oct 15]. Available from: http://www.yusynth.net/Modular/EN/ADSR/index_latest.html

8 2n5457 Datasheet [Internet]. [cited 2022 Oct 15]. Available from: https://www.onsemi.com/pdf/datasheet/2n5457-d.pdf

9 Fluke 75-3 Multimeter [Internet]. [cited 2022 Oct 15]. Available from: https://www.tequipment.net/FlukeDigital75Multimeter.html#tech-specs

10 Floyd TL. Electronic devices. 9th edition. Harlow (UK): Pearson Education Limited; 2014. 942 p.

11 Theremin [Internet]. [cited 2022 Oct 24]. Available from: https://120years.net/wordpress/the-thereminleon-termensoviet-union1922/.

12 Moog Theremini [Internet]. [cited 2022 Oct 24]. Available from: https://www.moogmusic.com/products/etherwave-theremins/theremini

13 The ‘Sound Processor’ or ‘Audio System Synthesiser’ Harald Bode, USA, 1959 [Internet]. [cited 2022 Oct 24]. Available from: https://120years.net/wordpress/the-sound-processor-harald-bode-germany/.

Schematic Diagram