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Microprocessor control of power factor correction

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Bachelor’s | Abstract

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Microprocessor control of power factor correction

The primary aim of this thesis was to explore the transition from an analog-controlled power factor controller to a digitally controlled one and identify suitable microcontroller attributes for this digital implementation.

The approach began with a theoretical analysis of the power factor, including its definition, computation, and effects. Subsequent review covered prior research on power factor correction and studied the fundamentals of control systems. The implementation phase commenced with a simulation of an analog-controlled power factor correction system, based on a chip manufacturer’s reference design. The process of digitalization incorporated elements that emulate analog-to-digital conversion in all measurements. By adjusting the parameters of these components, the impact of different microcontroller properties on the power factor was evaluated.

The findings led to a set of recommendations for appropriate microcontrollers. Additionally, a simulation model for a digitally controlled power factor controller was established.

This research not only identifies the ideal microcontroller properties for digital power factor correction but also provides a foundational simulation model that can be instrumental for future algorithm development in digitally-controlled power factor systems.

Keywords:

Power factor, power factor correction, microcontroller, digital control.

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Eelis Pyörre

Mikrokontrolleriohjattu tehokertoimen korjaus

Tehokerroin on tärkeä energiatehokkuuden mittari nykymaailmassa, kun sähköverkkoon kytketään entistä enemmän sähkölaitteita. Tehokerroin ilmaisee kuinka suuren osan sähköverkosta syötetystä tehosta laite käyttää hyväksi. Jotta sähkölaitteen tehokerroin ylittäisi viranomaisten asettaman rajan tulee tehokerrointa korjata korjainkytkennällä.

Tämän opinnäytetyön tavoitteena oli tutkia tehokertoimen korjaimen ohjauksen muuntamista analogisesta digitaaliseksi. Keskittymispisteenä oli digitaalisena ohjaimena käytettävän mikrokontrollerin tarvittavat ominaisuudet.

Teoriaosuudessa perehdyttiin, mistä tehokerroin muodostuu, kuinka se lasketaan ja mikä on sen vaikutus. Lopuksi keskityttiin ohjauksen perusteisiin.

Toteutusvaiheessa simuloitiin ensin vertailukohteeksi analogisesti ohjattu tehokertoimen korjain. Simuloidun kytkennän pohjana toimi ohjainpiirin valmistajan viitekytkentä. Ohjauksen digitalisointi toteutettiin lisäämällä analogi-digitaalimuuntimia simuloivat elementit jokaiseen mittaukseen. Näiden elementtien parametrejä muuttamalla tutkittiin mikrokontrollerin ominaisuuksien vaikutusta tehokertoimeen.

Opinnäytetyön tuloksena koottiin ehdotus sopivista mikrokontrolleri-vaihtoehdoista. Lisäksi valmistui digitaalisesti ohjatusta tehokertoimen korjaimesta simulaatiopohja, jota voisi tulevaisuudessa hyödyntää algoritmien kehittämiseen.

Asiasanat:

tehokerroin, tehokertoimen korjaus, mikrokontrolleri, digitaaliohjaus.

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List of abbreviations and symbols

AC-DC	Alternating Current to Direct Current
ACM	Average Current Mode
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuits
CrCM	Critical Conduction Mode
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
CM	Current Mode
DPF	Displacement Power Factor
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOL	End Of Life
FFT	Fast Fouerier Transform
IC	Integrated Circuit
PCM	Peak Current Mode
PFC	Power Factor Correction
PWM	Pulse Width Modulation
RMS	Root Mean Square
SMPS	Switched Mode Power Supply

THD_i	Total Harmonic Distortion of current
TPF	True Power Factor
uC	Microcontroller
VCM	Valley Current Mode
VM	Voltage Mode
D	Distortion Power
Q	Reactive Power
P_1	Fundamental Active Power
S_1	Fundamental Apparent Power
φ	Displacement angle

1 Introduction

Electrification is currently a topic of huge interest in a variety of sectors and it is resulting in, among others, an increased load demand on power grids. This increase means that even more attention is being paid to the efficiency of grid connected devices.

A key indicator of efficiency in grid connected applications is power factor which symbolizes how much of the power delivered from grid is actually utilized. Therefore, countries require a certain level of power factor and often manufacturers aim for a power factor close to unity for a business advantage.

The commissioner of this thesis is one such manufacturer, Micropower Ltd. They mainly manufacture single phase battery chargers. The chargers incorporate power factor correction (PFC) circuitry. This thesis aims to explore replacing an analog PFC controller of a charger, which is essentially a switched-mode power supply (SMPS), with a microcontroller (uC).

Chapter 2 covers basic background information and theory of power factor, including how it is calculated. Chapter 3 addresses how power factor can be corrected and some of the different correction techniques. Chapter 4 focuses on control schemes used to control a boost PFC and the simulation of an analog example in LTSpice.

Chapter 5 covers porting the analog example from LTSpice [1] into an equivalent model in Simulink and steps to digitize it.

In Chapter 6, the requirements for a uC suitable for future implementation are set. Parameters in the Simulink simulation are used to explore the minimum values for key uC properties that fulfil the requirements described in 2.4.

Finally in Chapter 7, the current solutions from manufacturers are evaluated to identify products that match the set requirements.

2 Power factor

Power factor describes how effectively power is utilised [2]. It is a key factor in reducing transmission grid stress and transmission line losses and increasing grid capacity [3], [4]. Power factor can be expressed as a percentage or as a ratio of power utilized in the range of 0 to 1. Power factor of 0 represents a situation where no delivered power is utilised by the load. Power factor of 1, also called unity power factor, describes a system that utilises all of the power delivered from the source. This means that there is no distortion, or oscillating power, also known as reactive power.

Reactive power is produced by non-linear elements in a power system. A reactive load can be inductive or capacitive, resulting in reactive power. Typical example of a non-linear element that acts as an inductive load is an electric motor, or choke inductors found in fluorescent lamp ballasts. Hence reactive power in industrial applications is generally inductive, due to use of electric machines in automation and large quantities of fluorescent lighting [4]. An example of a capacitive load are capacitor banks, that are sometimes used to balance the reactive load of industrial premises.

2.1 Displacement power factor (DPF)

Definition of power factor is dependent on the shape of voltage and current waveforms. When they are purely sinusoidal, power factor is defined by the displacement angle between the voltage and current waveforms. Hence it is called displacement power factor (DPF) [5]. The displacement angle is the angle between the fundamental voltage and current phasors. It represents the mismatch of voltage and current in time domain. The displacement is caused by either inductive loads, capacitive loads or both. An inductive load results in the voltage waveform leading the current waveform. A capacitive load in turn results in the voltage lagging behind the current waveform. When both types of elements are found in a system, the type of load depends on which is more

dominant. Different types of loads and their respective phasor diagrams are illustrated in Figure 1. Note that the voltage in a resistive load is in phase with the current and hence the overlap.

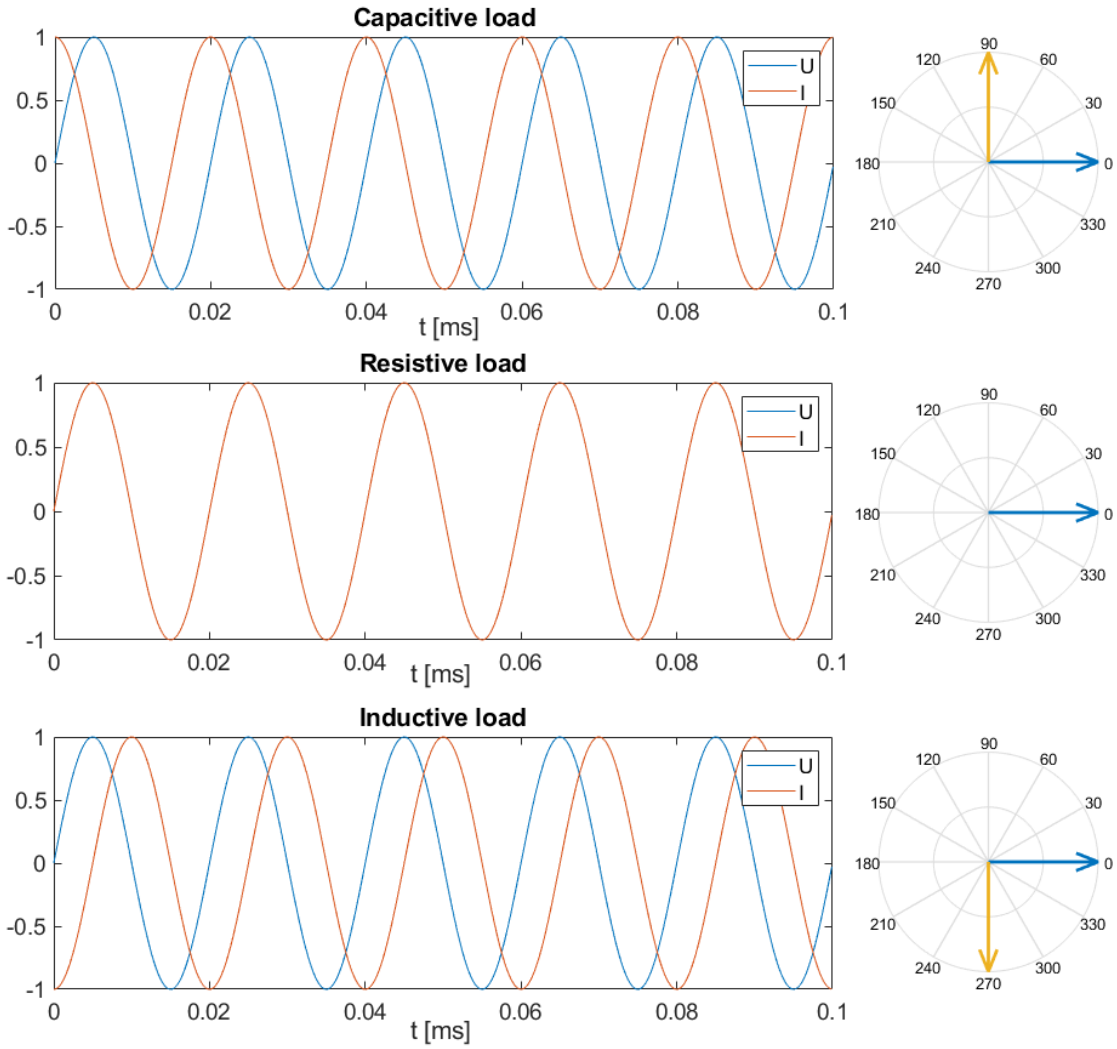


Figure 1. Different types of loads and their respective phasor diagrams.

Reactive power does not transfer energy to the load, but it adds additional stress on the transmission lines, increases losses in the transmission lines due to higher required root mean square (RMS) current to deliver the same power to the load, and increases costs for both the utilities and customers [4].

2.2 Harmonics

When the waveforms are non-sinusoidal the distortion of the waveforms must be included in the definition. This distortion is called harmonics.

Any periodic signal can be expressed as a sum of trigonometric functions [6]. The fundamental frequency, also known as first order harmonic signal is the lowest frequency signal, from which also the period is derived.

The fundamental frequency in power systems is the 50 or 60 Hz line frequency of a distribution grid depending on country. The frequencies of the harmonic signals are integer multiples of the fundamental frequency. [7]

The harmonic waveforms distort the fundamental waveform reducing the amount of true power utilized. Harmonics are depicted in the following figures.

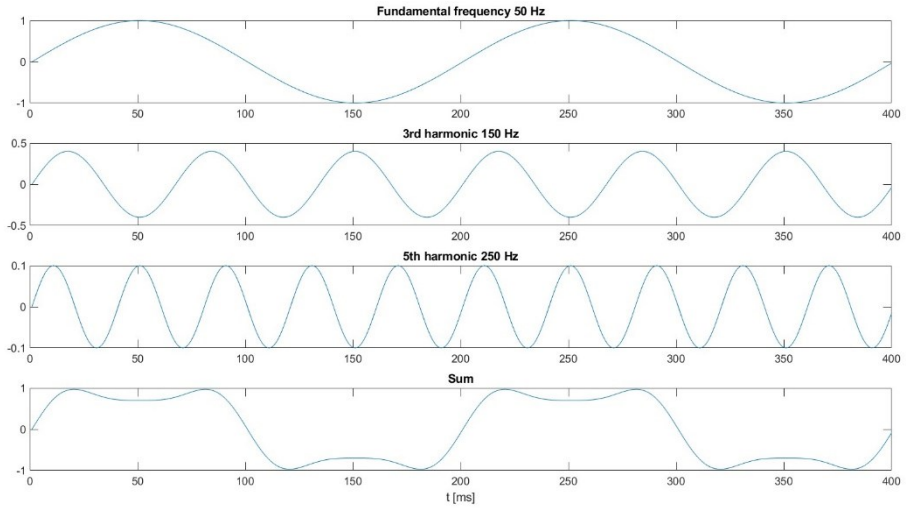


Figure 2. Example of harmonic sinewave composition. Note the amplitude scale.

The first 3 sine wave components in Figure 2 are the fundamental 50 Hz waveform and its 3rd and 5th harmonics. The 4th waveform, illustrates their

summation, and the resulting distortion.

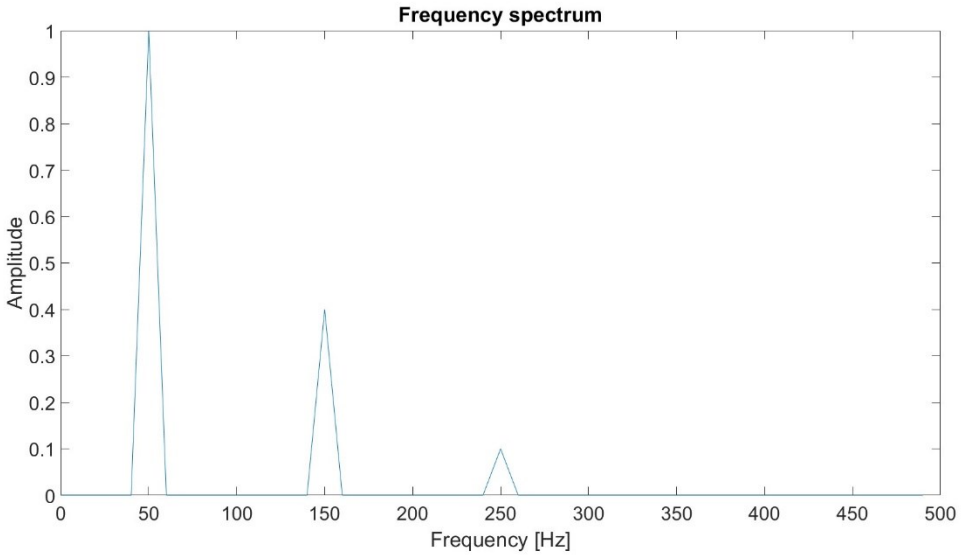
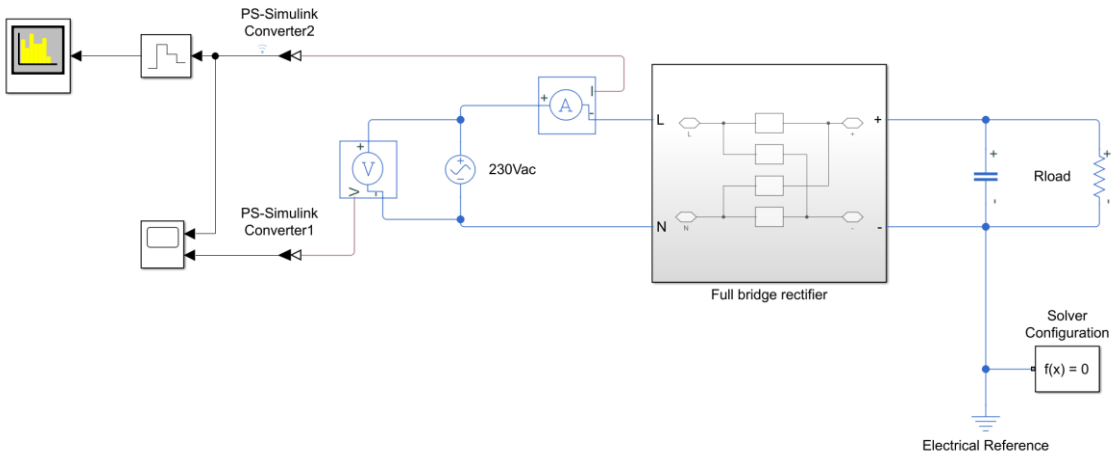


Figure 3. The frequency spectrum of the summed waveform in Figure 2.

Figure 3 is the 4th waveform displayed in frequency domain after performing a fast Fourier transform (FFT). It demonstrates that FFT can be used to extract the frequency components and their amplitudes from a periodic signal.

Harmonics are also a result of non-linear loads. Example sources of harmonics include electromagnetic interference (EMI) from other devices or appliances, and the switching action or full bridge rectifier of an SMPS pictured below.



Block diagram 1. Example of a full bridge rectifier and a DC-link as an AC-DC converter.

Block diagram 1 demonstrates a common topology used to rectify AC line voltage with a full bridge rectifier and smoothing it into a DC voltage for use in later DC-DC stages by using a DC-link capacitor. [8]

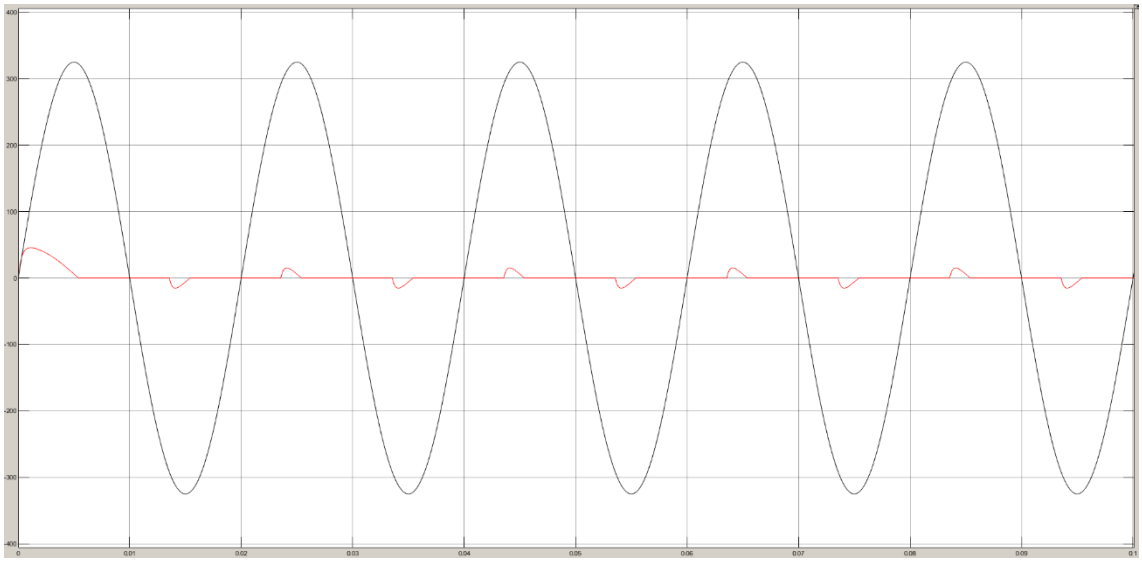


Figure 4. Input voltage and current waveforms of the full bridge rectifier in Block diagram 1.

Figure 4 illustrates the line voltage and current drawn from the source. It can be seen that the current is near in-phase, but very distorted. This occurs due to the operating principle of a full bridge rectifier. It works by alternating between conducting through two pairs of diode. Since this happens only near line peaks, current is only drawn for a short time. This combined with a capacitor's current characteristics results in short but large amplitude current pulses that are rich in

harmonics, being drawn from the source.

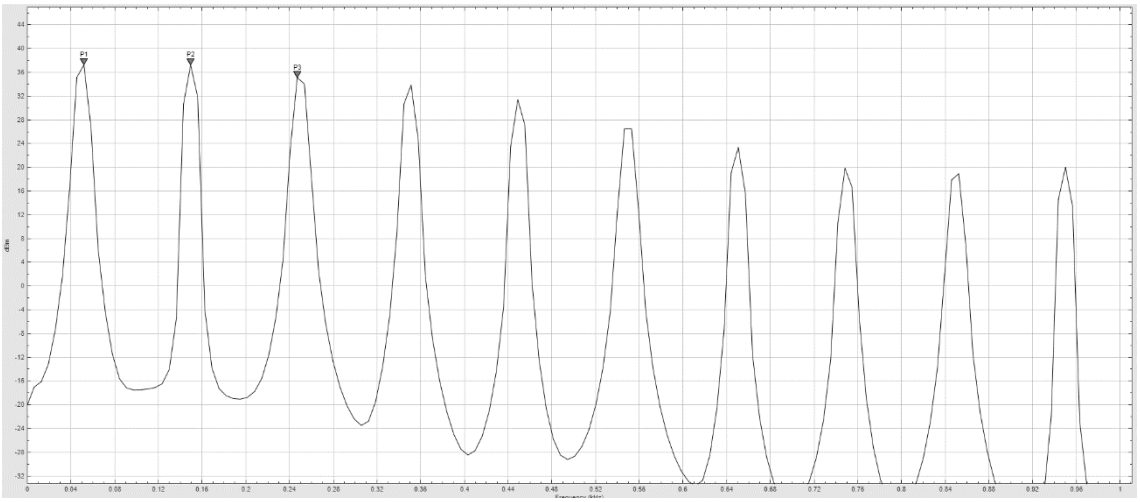


Figure 5. The current waveform of Figure 4 in the frequency spectrum.

Figure 5 displays the frequency spectrum of the drawn current. In this case the line voltage and current have a fundamental frequency of 50 Hz, and it can be seen as the first and the largest peak. Next peaks are 150 Hz and 250 Hz, which are the 3rd and 5th order harmonics of the fundamental, respectively.

When both, the waveform displacement and distortion are considered, power factor is called true power factor (TPF). It is a more accurate representation of power quality.

2.3 Calculation of power factor

Calculation of DPF and TPF is different. Calculating DPF is simpler, because it only depends on the phase angle between the voltage and current waveforms. The formula for DPF is:

$$DPF = \cos(\varphi) = \frac{P_1}{S_1}[2], [5],$$

where φ is the displacement angle between voltage and current, P_1 is the fundamental component of the active power and S_1 is the fundamental component of the apparent power.

Figure 6 demonstrates the relationships between apparent power, active power and reactive power. They can be drawn as triangle by shifting the vector of reactive power. Therefore, the relationships can be defined and calculated using trigonometric functions sine and cosine.

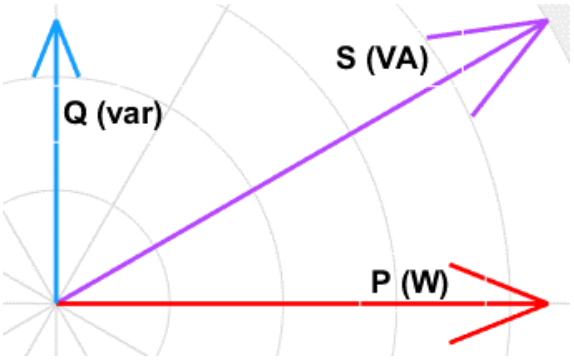


Figure 6. Power triangle.

The equation for TPF is more complicated. The equation accounts for the harmonic distortion:

$$TPF = \frac{P}{S} = \frac{P}{\sqrt{P^2+Q^2+D^2}} [2],$$

where P is the active power, S is the apparent power, Q is the reactive power, and D is the distortion power resulting from harmonics.

TPF can also be calculated by calculating DPF and how much harmonic distortion of current (THD_i) affects power factor and multiplying these.

$$TPF = \cos(\phi) * \sqrt{\frac{1}{1+THD_i^2}} [2]$$

This is the method used to calculate power factor in simulation later on.

2.4 Standards and technical specifications regarding power factor

Commissioner's products are subject to national and European laws and standards that govern appliance safety and electromagnetic compatibility (EMC).

Since this thesis focuses only on the PFC preregulator and more specifically it's control, only the standard(s) with requirements for power factor and injection of harmonic currents into the input line are considered. Harmonic current limits, for

total and individual orders, are set by European standard EN 61000-3-2. Minimum power factor of 0.98 is set by commissioners own datasheet.

3 Power factor correction

Power factor correction methods are split into 2 main categories based on the type of components and techniques used, passive and active.

3.1 Passive vs. active correction

Passive PFC uses passive components, ie. resistors, inductors and capacitors. This means that it does not use semiconductors.

Generally passive PFC is used to correct DPF by reducing the phase angle between line voltage and current. This is achieved by introducing an opposite reactive load to the ones already in the system. For example, if current is lagging behind voltage due to an inductive load, it can be compensated by adding a capacitor. It will oppose the inductive load in the system and increase the DPF.

Passive PFC can also be used to compensate harmonics to improve TPF using resonant shunt filters. They work by attenuating specific frequencies and the component values must be calculated beforehand based on the targeted frequency. [9]

Passive PFC has multiple drawbacks. The first one is its static compensation frequency. Another drawback is that since each shunt filter targets a single frequency, each harmonic order needs an individual filter. This increases component count, and therefore design complexity and cost. In some cases, the size of filter components can also be undesirably large.

Simplicity is the main advantage of a passive PFC. It does not require control and generally uses few components. Therefore, passive PFC is a good choice when reactive power in a system is fairly static and there are not many orders of harmonics that need filtering.

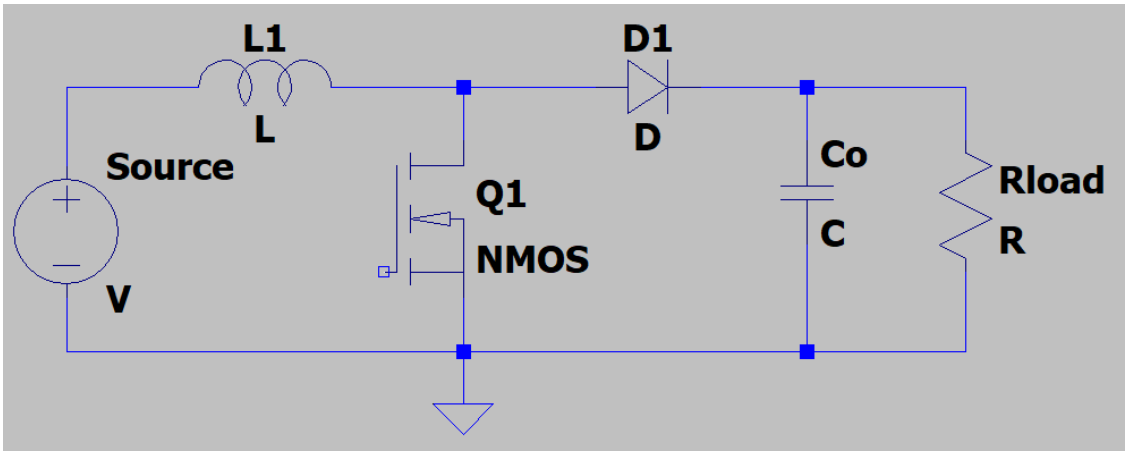
Active PFC uses active components i.e., semiconductor switches and control chips. It is used to achieve a higher power factor and enables dynamic compensation.

A common example of an active PFC is adding a boost converter between the full bridge rectifier and DC-link in Block diagram 1, to compensate their non-linearity. The shape of the boost inductor current waveform can be shaped with control as demonstrated later. Therefore, by controlling the inductor current, a more sinusoidal current can be achieved. [10], [11]

Other converter topologies, like interleaved boost or totem pole, can also be used for power factor correction [12]–[14]. In addition, active power factor correction includes using semiconductor switches to switch reactive loads and harmonic filters [15].

3.2 Active PFC using a single phase boost topology

A boost converter is a step-up converter that consists of a boost inductor, switch, secondary switch (generally a diode) and output capacitor. It is a step-up converter because it produces an output voltage that is higher than the input voltage. The basic topology is depicted in Schematic 1.



Schematic 1. A boost converter.

The basic operating principle of a boost converter Is the following: when the switch Q1 is closed, it shunts the inductor L1 to ground, therefore, all the current is flowing through it and building up a magnetic field around the inductor. Since Q1 is closed, the anode of D1 is grounded and therefore D1 is backwards biased.

When Q1 is opened, the magnetic field of L1 starts collapsing and this flips the polarity of the voltage across L1. So instead of subtracting from the source voltage, it is instead applied to the rest of the circuit in series with the source voltage. This is why boost converter produces a higher output voltage. The diode D1 will be forward biased and current flows to the rest of the circuit. If lower secondary switch losses are desired, the rectification can be synchronized by replacing the diode with a semiconductor switch. The purpose of Co is to maintain the output voltage and current when switch is closed.

A boost converter works as a PFC by shaping the average boost inductor current because the inductor is in the input. As can be seen from the operating principle of a boost converter, in both the on and off cycles of switching, the current flows through the boost inductor. Therefore the shape of the input line current can be controlled to achieve a more sinusoidal input current - as opposed to the spiking and largely distorted current of a capacitor only.

A clear disadvantage of a boost PFC is the inclusion of an additional power stage in the system, as compared to passive PFC. This increases component count, design complexity and can reduce efficiency. However, there are many integrated circuit (IC) solutions that integrate a large portion of the circuitry in a single chip. This counteracts the increased complexity and component count.

An active PFC using a boost converter presents many advantages over a passive PFC. The same design can react to different power quality and load scenarios using adaptive control algorithms and allows for universal input, ie. 110/240V and 50/60Hz. It can also provide additional features like power fault detection. These advantages make a boost PFC a good choice.

3.3 Conduction modes

Boost converters can be classified into 3 different categories based on the continuity of inductor current: continuous conduction mode (CCM), critical conduction mode (CrCM) also known as boundary conduction mode and discontinuous conduction mode (DCM). Out of these 3 CCM is used in higher power applications due to it's properties.

In CCM the inductor current never reaches zero under steady state operation, ie. the inductor is constantly conducting current [11]. This provides the lowest ripple current of all conduction modes which makes it best suited for a PFC application.

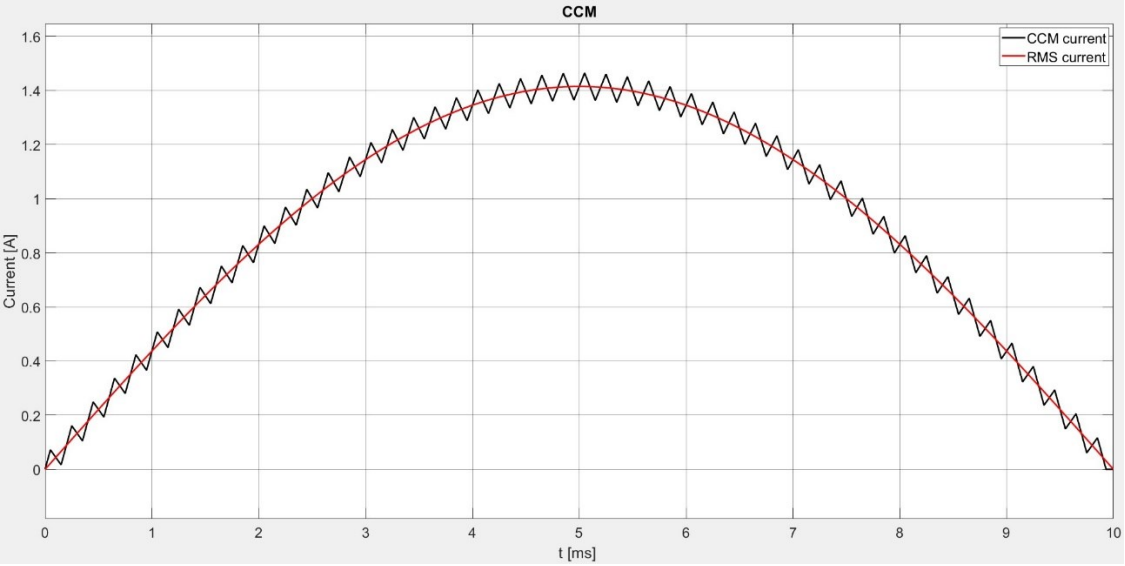


Figure 7. Inductor current in CCM.

In DCM the current flowing through the inductor is zero for a period of time each cycle [11]. DCM is easier to control, but requires much higher peak currents to achieve the same average current as in CCM. This translates to higher ripple current, which is not desired. A DCM boost converter is valid choice for small and simple step-up conversion applications, but is not a good choice for a power quality applications. It should be noted that even a converter designed to operate in CCM will enter DCM when the average inductor current is less than

half of the ripple current due to low load or during line crossover. Accounting for this with an adaptive algorithm would improve PFC performance.

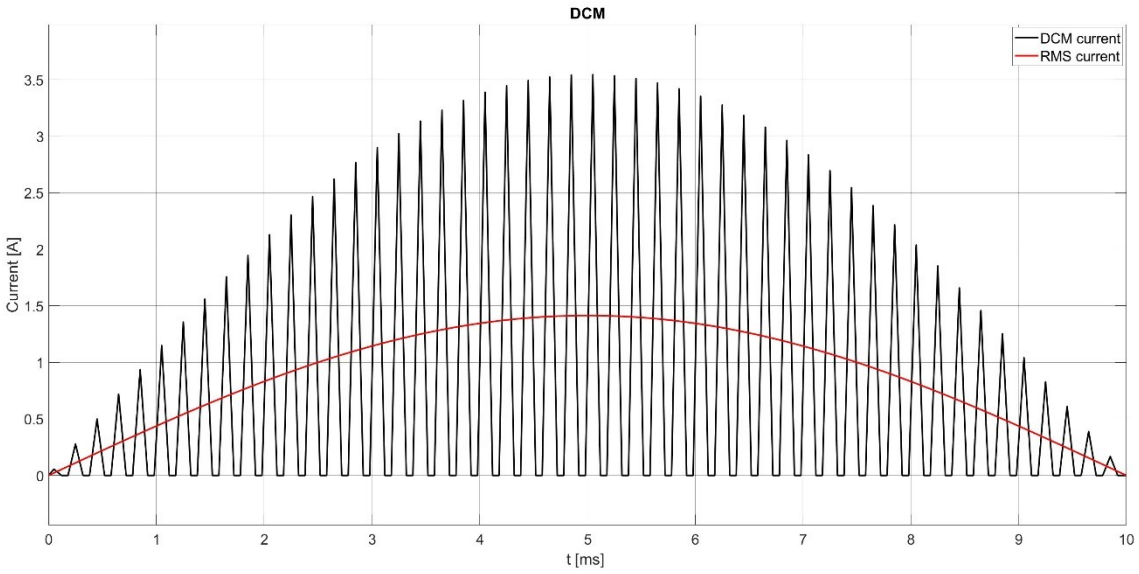


Figure 8. Inductor current in DCM.

CrCM is a middle ground solution between CCM and DCM. In CrCM, the switching is performed so, that once the inductor current approaches zero and it's magnetic field is about to collapse entirely, the switch is closed so the magnetic field starts building up again [11]. CrCM lowers the required peak currents as compared to DCM, but is not as complex to control as CCM. A disadvantage of CrCM in PFC applications is that it works by modulating the period and inversely frequency. The variable frequency results in increased EMI, which is undesired.

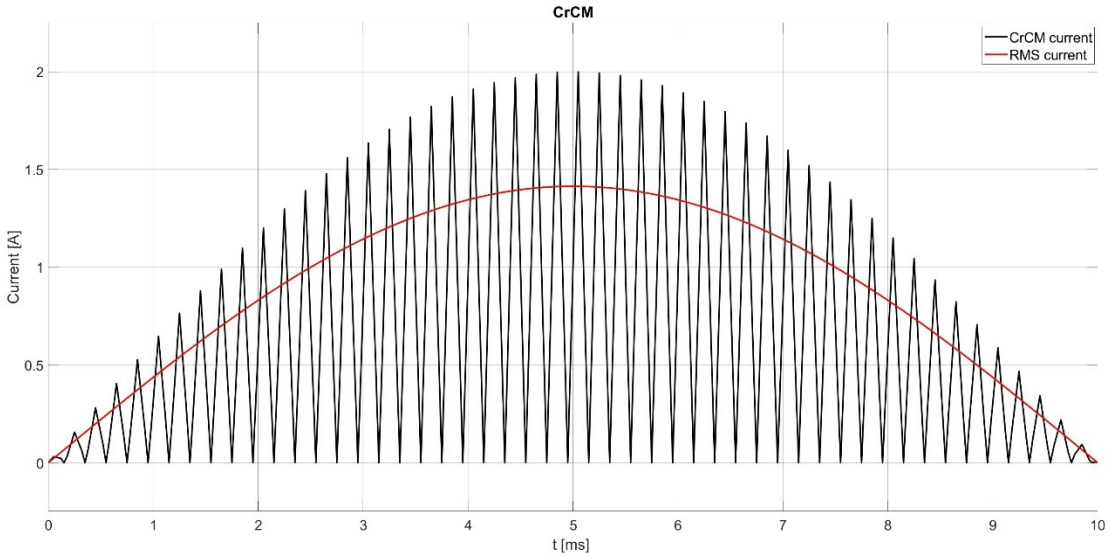
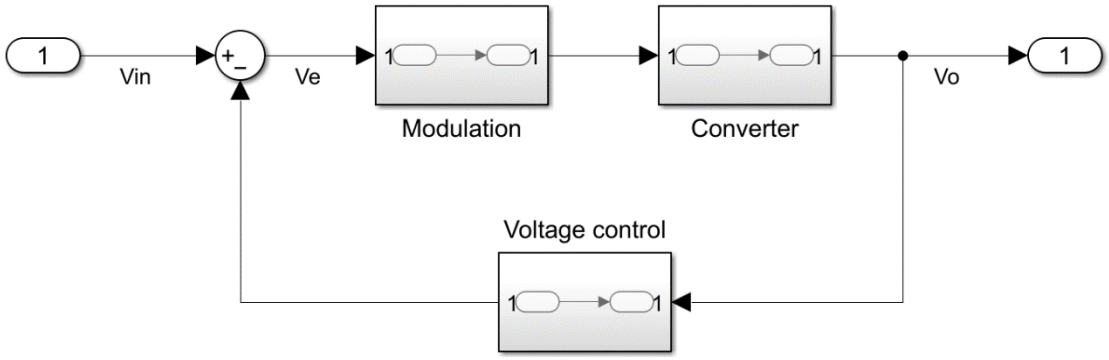


Figure 9. Inductor current CrCM.

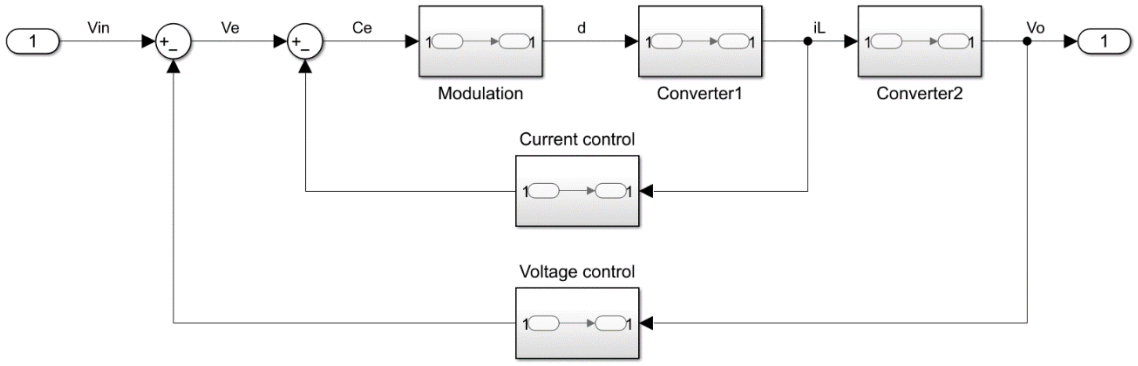
4 Control of a single phase boost PFC

There are two main control methods for converters: voltage mode (VM) or current mode (CM). Like the name implies, in VM only the output voltage is fed back and used to generate a control signal. Block diagram 2 illustrates a voltage control loop. In VM the control loop gain/crossover frequency has to be low to achieve low steady state error due to converter ripple. This leads to poor transient response.



Block diagram 2. Voltage control.

CM builds upon voltage mode, by using the voltage error signal instead as a current reference, and generates a control signal based on inductor current error, in reference to the voltage error. Block diagram 3 highlights why the voltage loop is often considered an outer loop and current loop an inner loop. In a boost PFC the main goal is to control the current waveform, therfore CM is used.



Block diagram 3. Current mode.

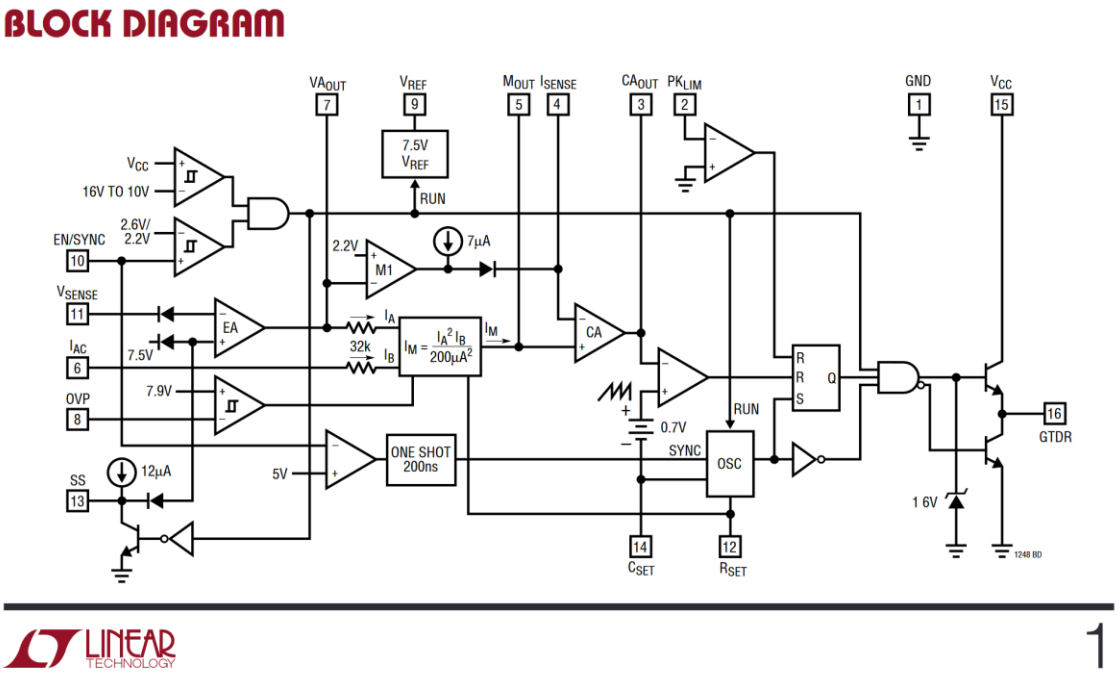
CM control of a boost converter can in turn be implemented in a lot of ways depending on the design objective. Control methods include among others peak current mode (PCM), valley current mode (VCM) and average current mode (ACM).

PCM and VCM operate by detecting either the maximum or minimum current per switching cycle, ie. the current peaks and valleys like the names imply. They are simple to implement, but result in some steady state error unless compensated for and can be susceptible to switching noise.

ACM is more complex, but results in the lowest ripple, which translates to lower EMI emissions and is therefore desirable in a PFC [11]. Due to these reasons ACM is a good choice for a boost PFC control method. It is also the operating principle of the currently implemented PFC controlled, so ACM is chosen as the control method to implement.

4.1 Example analog power factor controller's operating principle

LT1248 is a line current averaging power factor controller [16]. This means that the converter works in CCM and is controlled with ACM. LT1248 incorporates a voltage control loop, current control loop, overvoltage protection, line peak current limiting, soft-start, and an integrated gate driver.



Block diagram 4. Block diagram of the internal circuitry of the LT1248 power factor controller [16].

The basic operating principle of the IC is that the error amplifier EA compares a portion of output voltage on pin V_{SENSE} against the 7.5V reference voltage and produces an amplified error signal. A portion of the rectified mains voltage is applied in the Iac pin. The multiplier I_M found in Block diagram 4 uses these two signals to produce a rectified full wave current reference.

This current reference is then compared against the inductor current from pin I_{SENSE} in the current amplifier CA to produce a control signal.

The control signal is modulated into a pulse-width modulated (PWM) signal by comparing it against an oscillating ramp. The ramp has an ascending slope, and when it starts ascending from it's lowest value, it sets the set-reset flip-flop (SR-FF) to output a high signal. This pulls GTDR to V_{CC}. When the control signal exceeds the ramp voltage, the SR-FF is reset and GTDR is pulled to ground. This produces a square wave voltage that is used to drive the boost converter switch, generally a MOSFET.

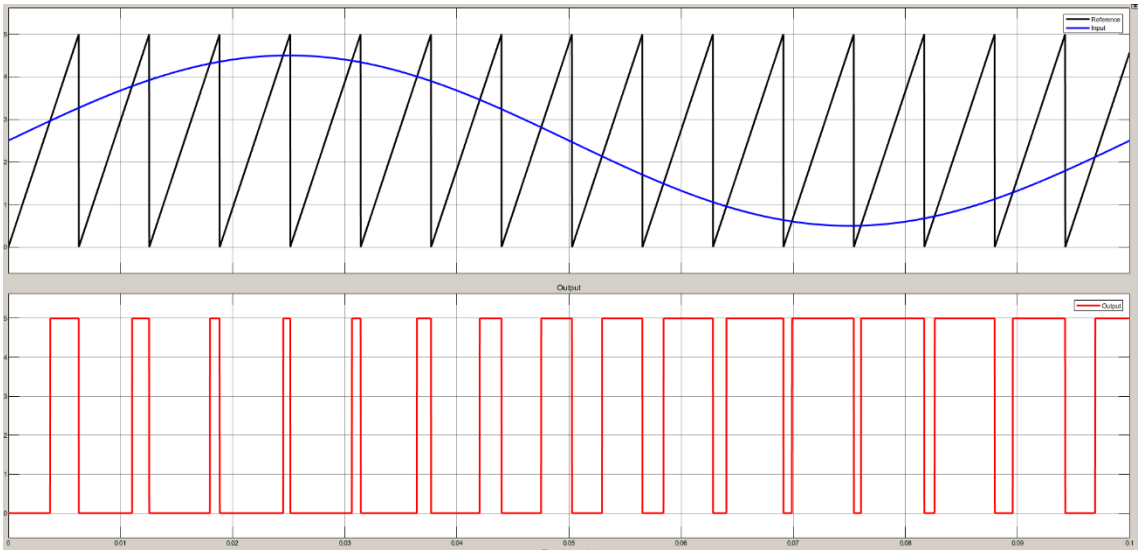
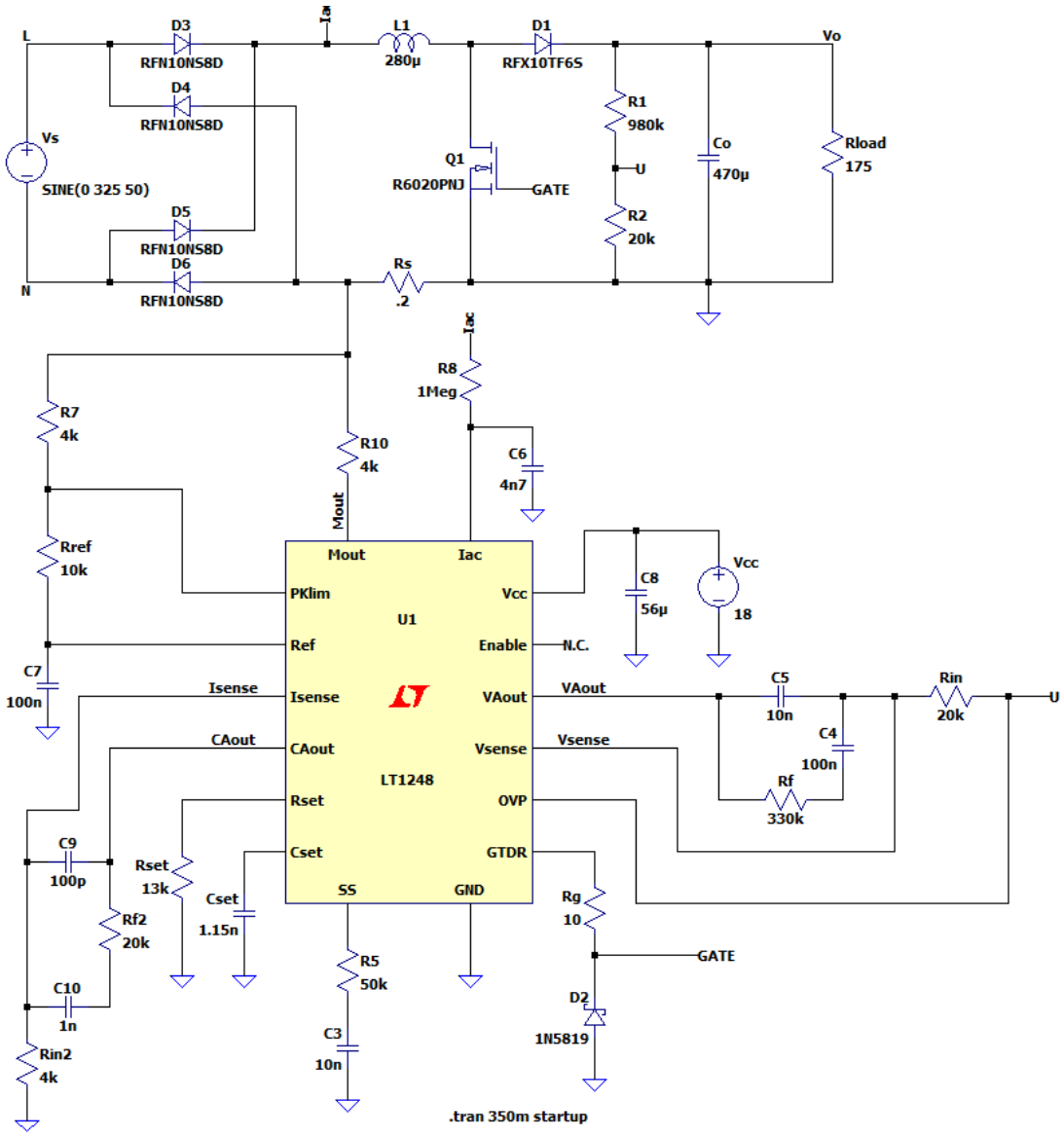


Figure 10. PWM example.

The amplitude of the PWM signal (in red) is V_{CC}, frequency f_{sw} is set by C_{SET} and R_{SET}, and duty cycle is set by the amplitude where the control signal (in blue) and ramp (in black) cross, like in Figure 10.

The LT1248 does provide functions that are beneficial in an actual device, but are not considered in this thesis. This includes features like soft starting and external syncing, line peak current limiting and output voltage protection.

An LTSpice simulation of a slightly modified variation of the chip manufacturers' example of a typical application is used to validate the Simulink-simulations in this thesis. It is depicted in Schematic 1.



Schematic 2. A 375V 800W preregulator.

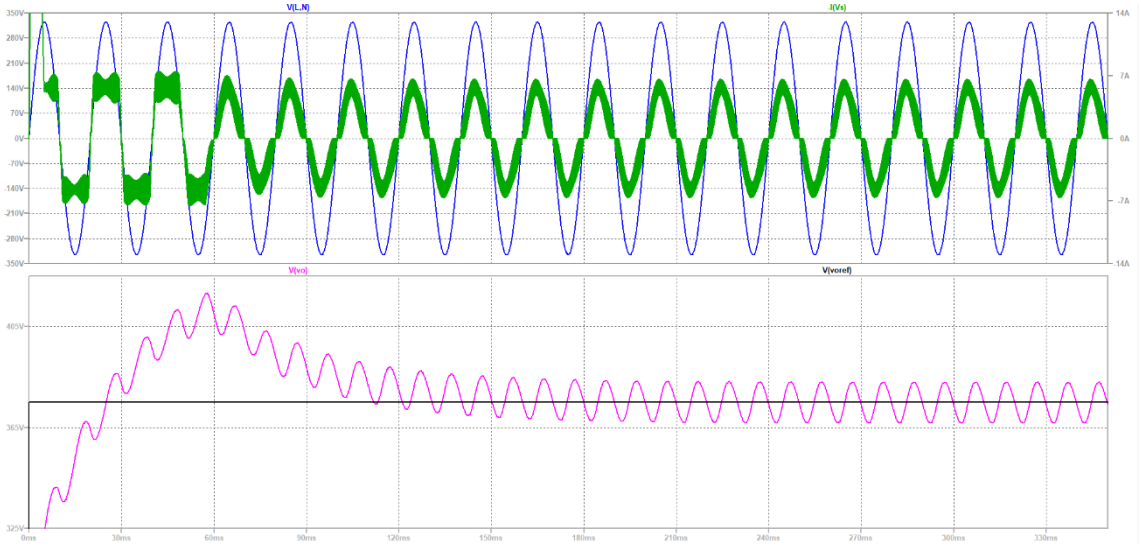


Figure 11. LT1248 PFC waveforms.

The simulation displays good steady state performance. The current and voltage in Figure 11 are in phase, the current is sinusoidal and output voltage is well regulated. Simulated converter efficiency is 97%.

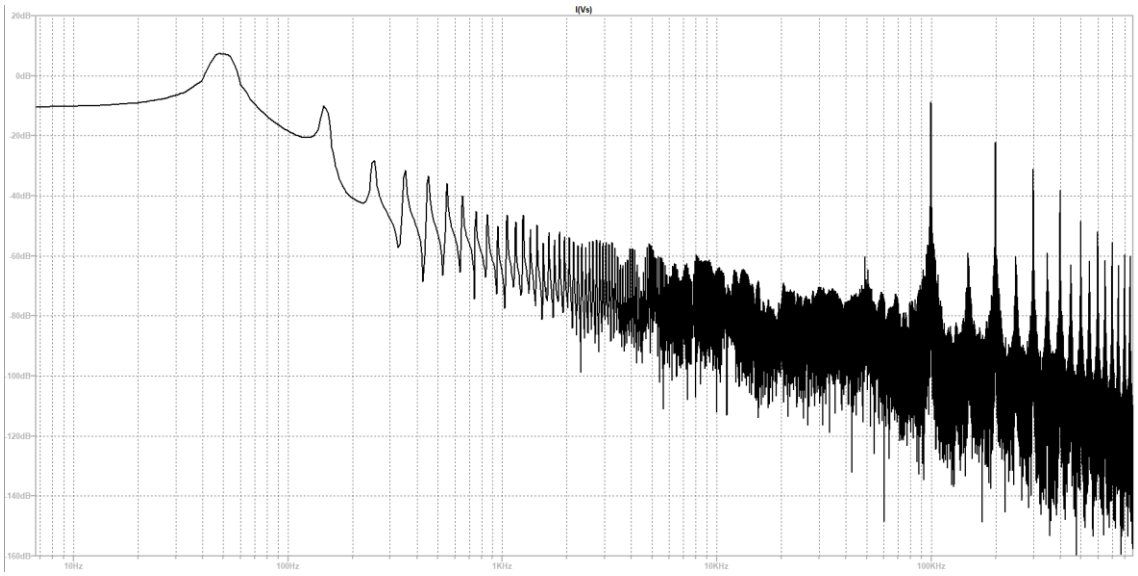


Figure 12. LT1248 PFC input current in the frequency spectrum.

Performing FFT on the steady state current displays that the harmonic currents and switching frequency are both in check as expected. Harmonic current levels

and their limits are listed in Table 1. Power factor of this simulation is not calculated, but based on these waveforms it is estimated to be acceptable.

Table 1. IEC 61000-3-2 limits for equipment with current <16A per phase.

Harmonic order	Maximum harmonic current [A]	Result [mA]
3	2,30	410
5	1,14	50
7	0,77	35

4.2 Analog vs. digital control

The power stage of a converter operates in the real world and produces analog signals. An analog signal is continuous in time and infinite in resolution. In analog control, the input signal is processed as an analog signal to produce a control signal and thereafter a driving signal. In practice, analog control is implemented with with a combination of operational amplifiers, comparators and latches which all work with voltage signals.

In digital control an analog signal has to be converted to digital for processing, eg. with a uC. This is done by sampling the input signal at discrete time intervals and comparing it against a known reference voltage to produce an integer of n-bits. This is known as analog-to-digital (A/D) conversion and is done with an analog-to-digital converter (ADC). ADC is a common peripheral in uCs. The equation below represents how A/D conversion is performed.

$$U_{int} = \frac{V_{in}}{V_{ref}} * (2^n - 1)$$

Where U_{int} is the resulting integer, V_{in} is the measured voltage, V_{ref} is the reference voltage, usually the microcontrollers supply voltage, and n is the number of bits of the A/D conversion.

The driving signal can also be produced digitally with a PWM peripheral commonly found in uCs. It works with a similar principle as in Figure 10 by running a counter with a fixed frequency clock and comparing another value against the counter, toggling an output pin based on which is greater.

Digital control logic is implemented in software with algorithms between A/D conversion and PWM. This provides flexibility in design, but digital control has a couple of drawbacks. The sampling frequency limits the frequency of signals that can be measured. Furthermore, the finite ADC resolution results in quantization error where values that fall between 2 adjacent voltage steps get rounded. Frequency and resolution are also a limiting factor when generating the driving signal with a PWM peripheral, for similar reasons.

4.3 Drawbacks of an analog PFC controller

Analog PFC controllers are a tried and tested way of controlling a boost PFC. However using application specific integrated circuits (ASIC) leaves a manufacturer vulnerable to a component’s end of life (EOL) and component shortages. ASICs rarely have pin compatible replacements, and even then would most likely require retuning of surrounding circuitry.

Another drawback of analog PFC controllers is their rigidity. Tuning and configuration is done with components and can only be done during the design process. Any additional features also require adding components. Using a uC instead allows the use of parameters, which are easier to modify, add or remove afterwards requiring no hardware changes.

Lastly they lack communication capabilities that uCs have. Those can be helpful to increase overall system performance by enabling more holistic system control, especially during fault conditions.

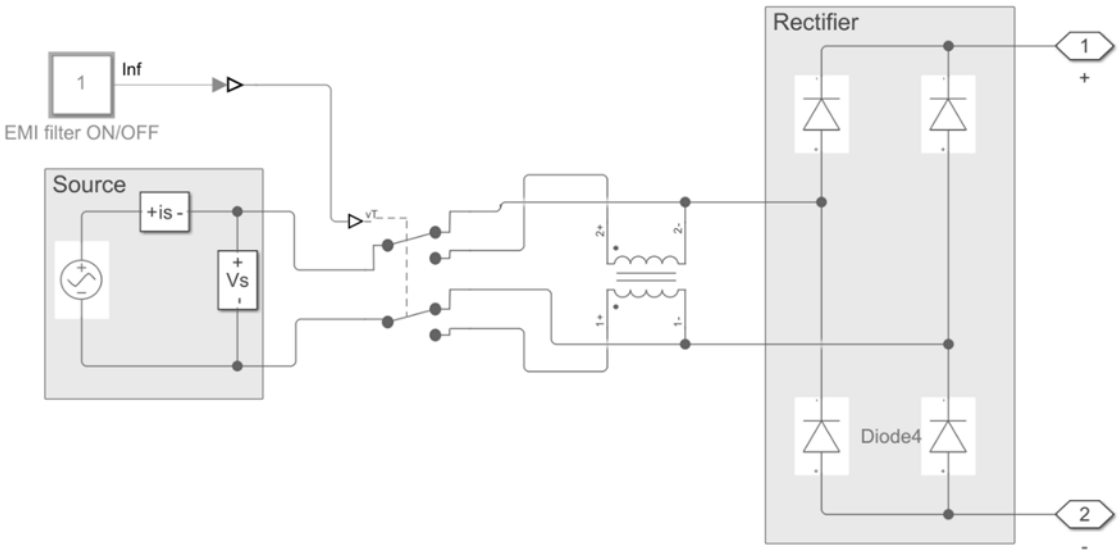
5 Simulation in Simulink

Bulk of the work for identifying key properties of a possible uC for digital PFC control is done via simulation in Simulink® using Simscape electrical [17], [18]. Simulink is a block diagram environment for performing MATLAB® simulation. It works on top of MATLAB, a MathWorks product, but provides an easier to work with block diagram user interface. Simscape is an additional set of building blocks on top of Simulink that provides blocks for simulating physical systems in multiple domains. The domain of interest here is electrical.

5.1 A modified CCM boost PFC example

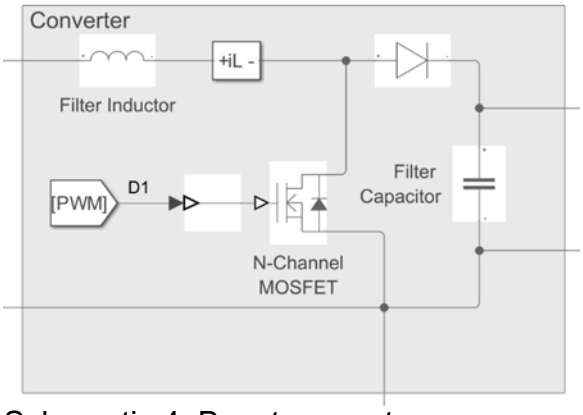
Simscape electrical comes with examples. One of these examples is a CCM boost PFC example, [19] that implements the chosen control scheme of ACM. This example was used as a starting point and modified to include power quality measurements for later comparison, component values were changed and some of the control algorithm was adjusted while maintaining the same control scheme.

The simulation is structured into 5 parts; source, converter, load, controls and measurements. The first part is the voltage source, pictured Schematic 3. A toggleable common mode choke for EMI filtering is included to more accurately represent an actual PFC converter’s operation. The source voltage and current waveforms are measured to validate the effectivity of the PFC. The input voltage measurement used in the control is done after the rectification. The full wave rectified input voltage is used for adjusting for universal input, and creating the current reference.



Schematic 3. Voltage source and full bridge rectifier.

The converter portion is a basic boost topology converter pictured in Schematic 4. The input current is sensed from the high side here. In practice, the current sensing would be done low side for simplicity's sake. The converter's component values are based on the LTSpice implementation for result comparison.



Schematic 4. Boost converter.

The load in Figure 13 is a simple resisitive load with resistance calculated from nominal power and reference output voltage. Resistive load is selected to easily compare results to the LT1248 controlled PFC implemented in LTSpice.

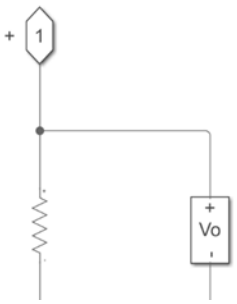
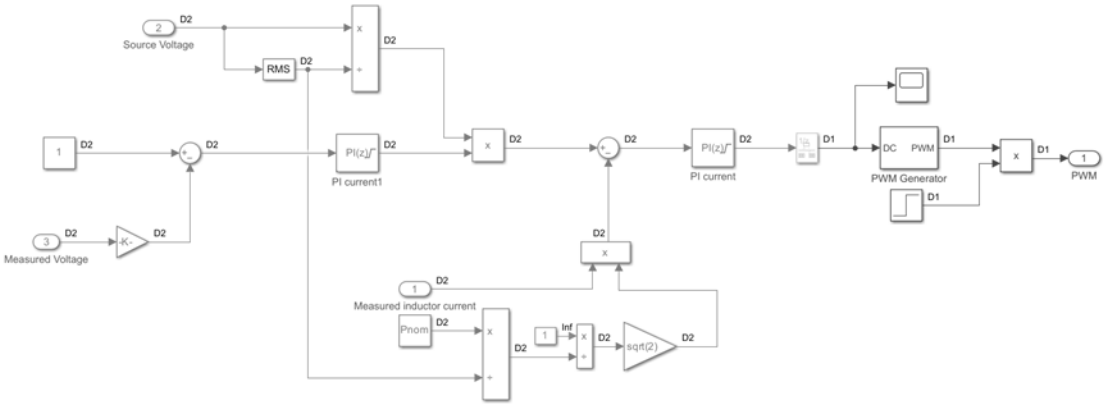


Figure 13. Resistive load with output voltage sensing.

The main focus of this thesis, the control logic, is depicted in Block diagram 5. It consists of input voltage normalization, voltage error, voltage

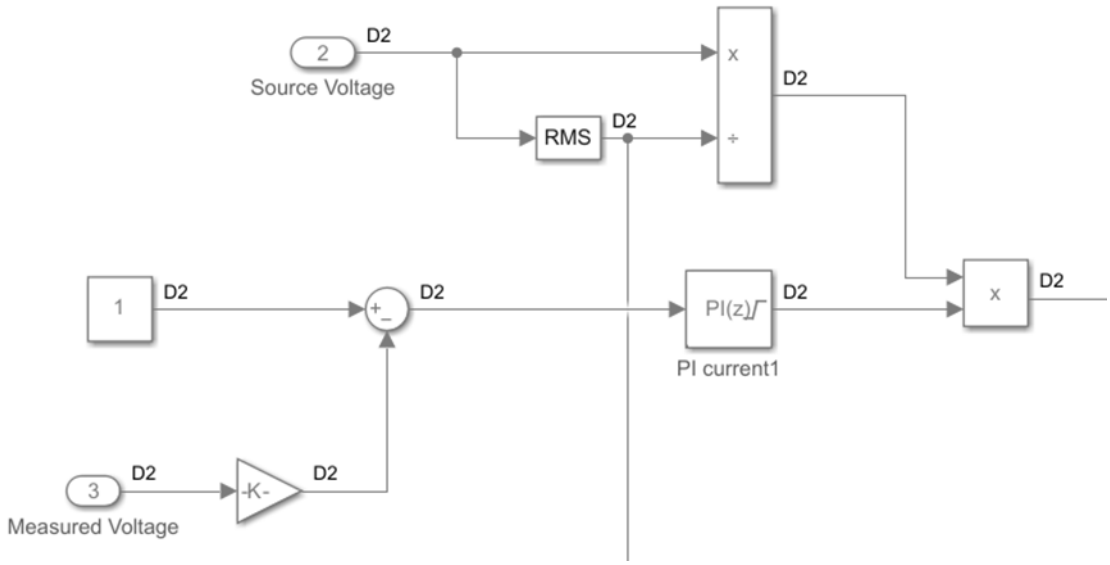
controller, inductor current normalization, current error and control and finally a PWM generator.



Block diagram 5. Control diagram.

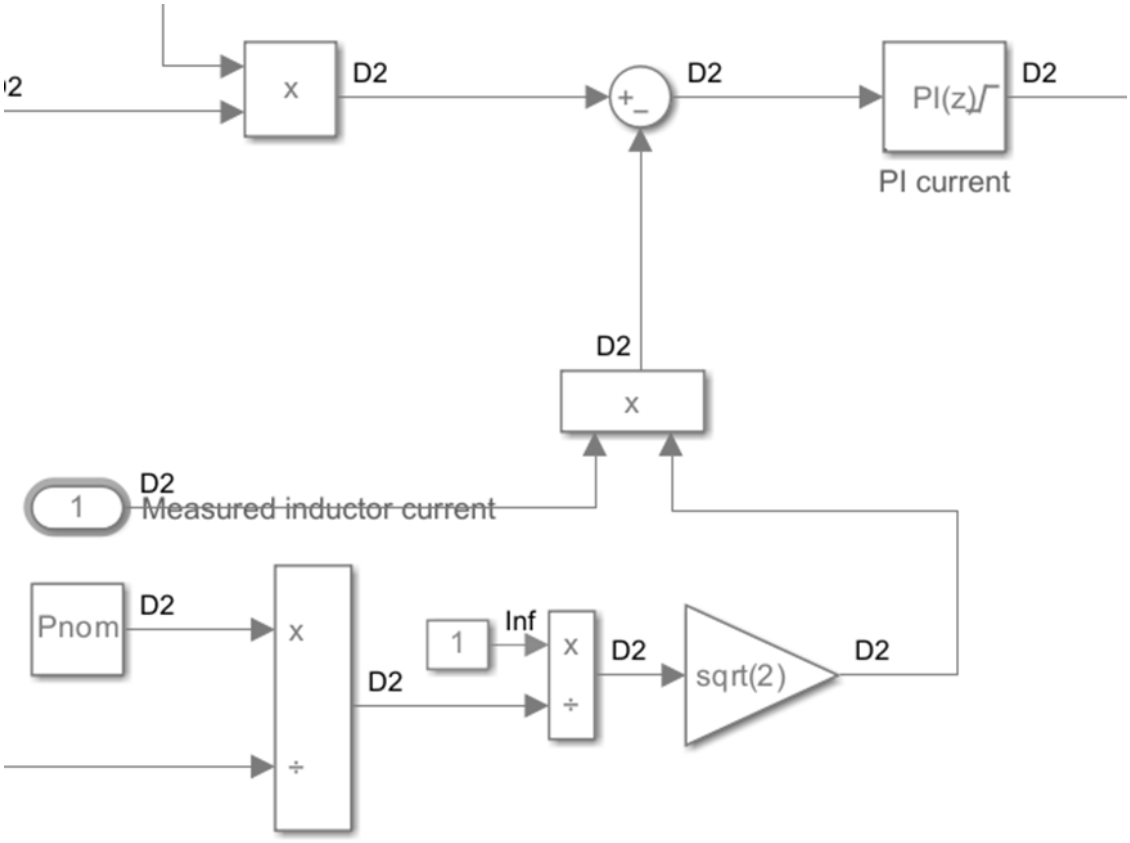
The voltage control is depicted in Block diagram 6. It starts by sensing the output voltage, converting it into per unit (P.U.), where the desired output voltage is used as a reference level, and comparing the result to a reference of 1 P.U. to produce a voltage error signal. The voltage error is fed to the outer loop voltage proportional-integral (PI) controller that produces the steady state current reference.

The input voltage RMS is calculated and used to divide the instanenous input voltage to produce a normalized full wave rectified reference signal with an amplitude of square root of 2 regardless of line level. The steady state current reference is multiplied by the full wave rectified reference signal to produce the current control signal that follows the input voltage.



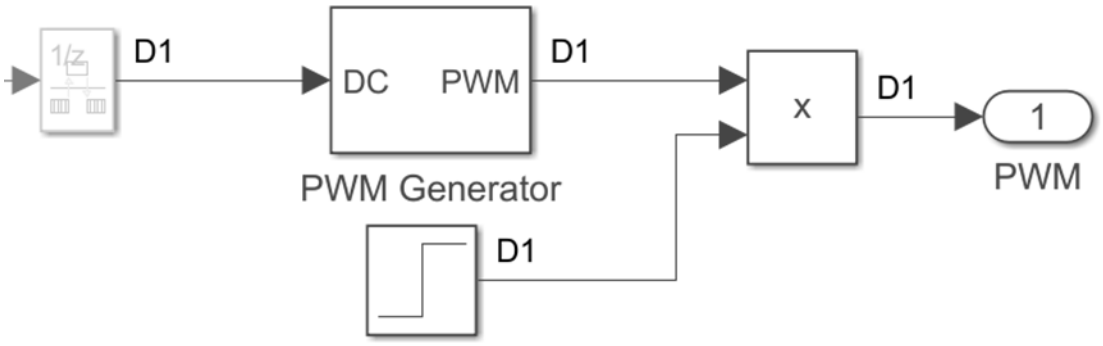
Block diagram 6. Voltage control.

The RMS input voltage and a predetermined nominal power P_{nom} is used to normalize and convert the sensed current into P.U. This is to allow the converter to work irrespective of line level without retuning. After normalizing the current, it is compared against the current reference from the voltage control and fed to fast inner loop current PI controller.



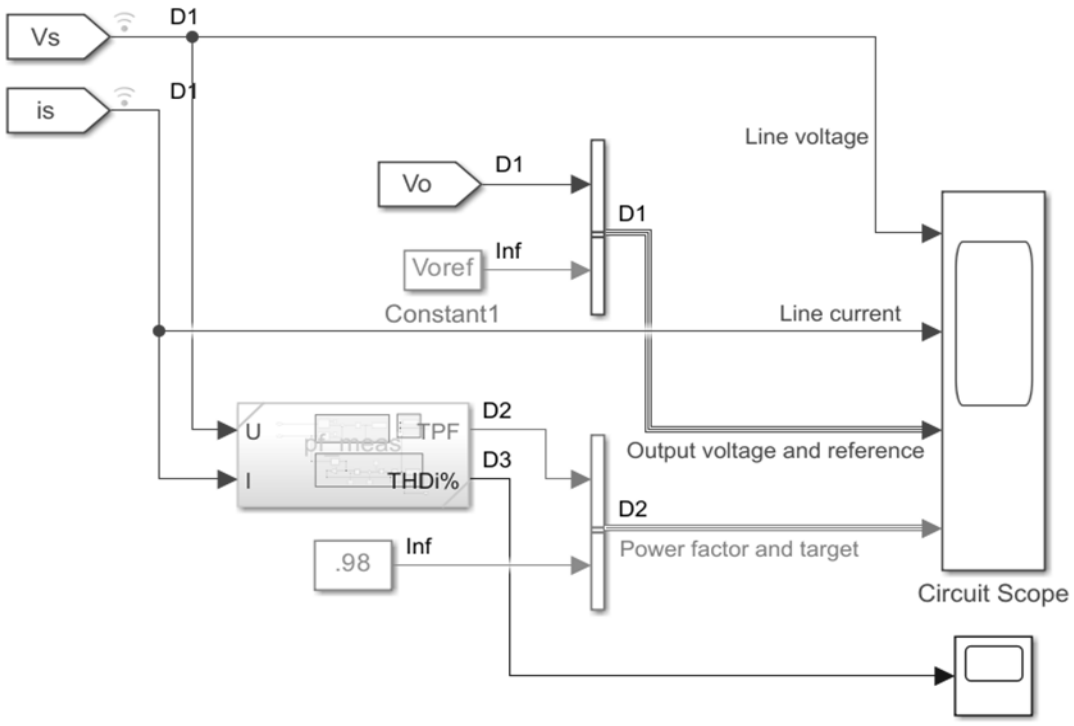
Block diagram 7. Current control.

Finally the control signal is fed to a PWM generator through a rate transition block. Purpose of the rate transition is to increase simulation speed by simulating the control logic in a slower domain. The PWM generator has a set switching frequency of 100kHz and the block accepts a duty cycle as its input. The generated PWM control signal is multiplied with a step function that acts as an enable signal.



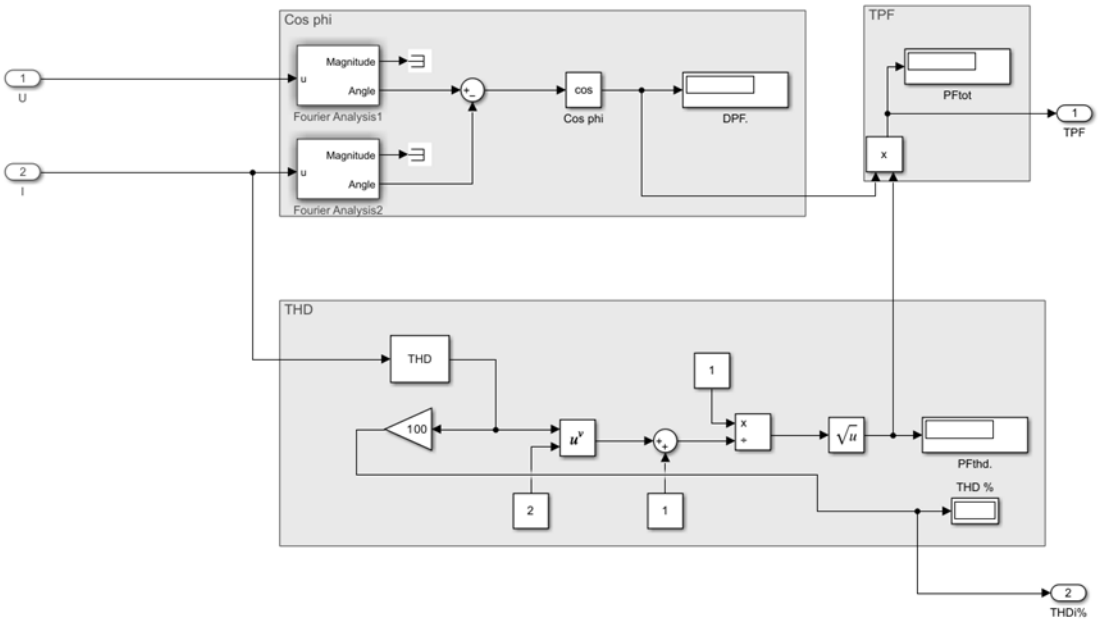
Block diagram 8. PWM modulator with enable.

The measurement block is mostly just combining all the main signals of interest and feeding them into a single oscilloscope view. It does however include a custom block that implements power quality measurements. It takes the source voltage and current as input and outputs a TPF that accounts for harmonic distortion.



Block diagram 9. Measurement block.

The power quality block calculates the TPF and THDi. The calculation is split into two separate sections, illustrated in Block diagram 10. The first one calculates DPF and another one calculates PF_{thd}, which is the distortion power factor.



Block diagram 10. Power quality measurement block used for validation.

Displacement angle is calculated by performing fast fourier transform (FFT) on both the voltage and current waveforms. Only the angle is of interest here, so magnitudes are ignored. DPF is calculated by taking the cosine of the displacement angle.

To calculate PF_{thd} a built-in block that calculates THD is used. Rest of the calculation is done with the following equation.

$$PF_{THD} = \sqrt{\frac{1}{1 + THD_i^2}}$$

Finally DPF and PF_{thd} were multiplied to calculate TPF.

The simulation’s operation waveforms in Figure 14 was compared to its LTSpice counterpart in Figure 11. The start up sequence is somewhat different, but the steady state operation of the two simulations match satisfactorily. Additionally, it was verified that the Simulink simulation achieves a power factor that fulfills the requirement of 0.98 in 2.4.

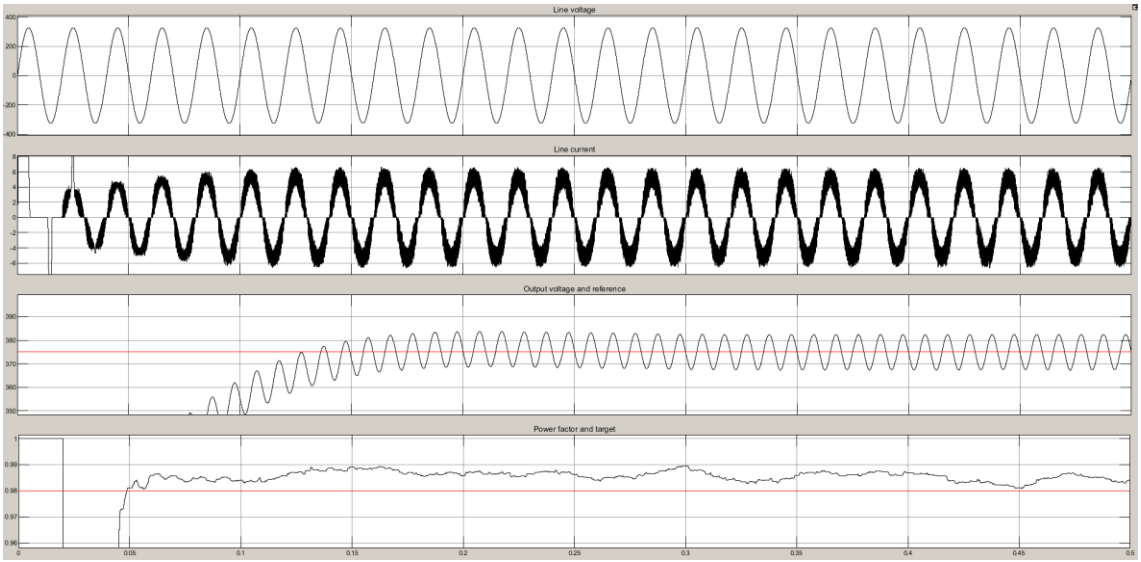


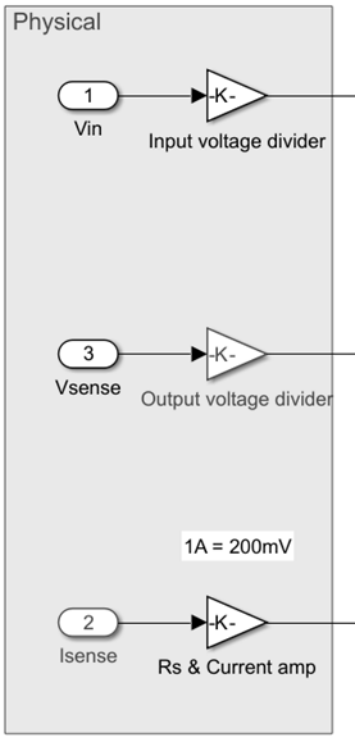
Figure 14. PFC operation waveforms.

The converter’s control is only enabled in the second line period, this results in a spiky input current during startup. In practice a soft-start sequence and or current limiting similar to one found in LT1248 should be implemented. However, the output voltage has a more desirable transient response in comparison.

5.2 Digitalization

Digital control usually requires a slightly different approach as opposed to analog. In this thesis the approach is to just implement A/D conversion at the control inputs, adjust the calculations to suit a microcontroller, and see the result. This means that the final result might not be optimal from control theory point of view, but as long as at least a similar level of performance is achieved, the solution Is acceptable.

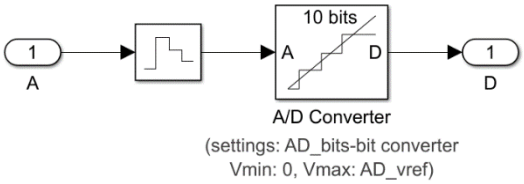
At the input of digitalized controls, gains are used to emulate the voltage and current sensing circuitry that an actual implementation would use. The goal of these circuits is to convert all measurements to a similar range with each other and the ADC reference voltage to maximize resolution.



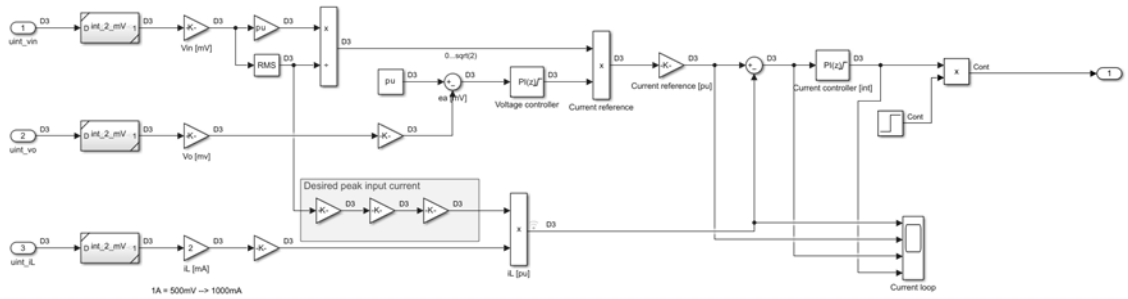
Block diagram 11. Gains representing physical sensing circuits.

An ADC subsystem is implemented by combining a sample and hold block with a built-in A/D converter block. The operating frequency of the sample and hold block is the sampling frequency. The A/D converter block has the following parameters: Number of bits, minimum and maximum reference voltages. A reference voltage of 10 volts was chosen. In an actual implementation this could be provided via a voltage reference.

The control logic depicted in Block diagram 13 is almost identical to the analog version. The key difference is that additional calculations are required because the values are stored and used in the algorithm as integers instead of decimals, because floating point arithmetic is considerably slower. So, to preserve resolution after A/D conversion, voltages and current are in millivolts and milliamps respectively, instead of volts and amps. The same applies to the per unit conversion. A reference unit of 1 would result in floating point numbers and thus won't work. So a reference unit of 1000 was chosen.

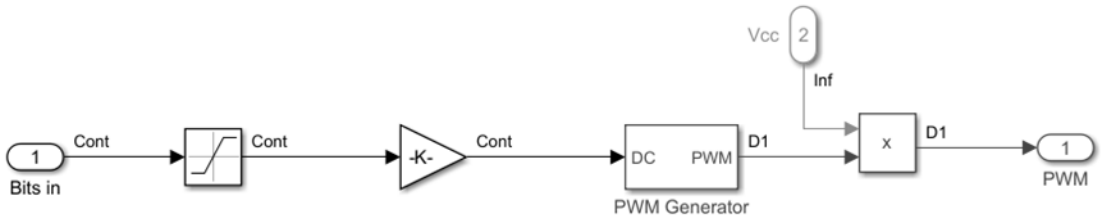


Block diagram 12. A/D conversion.



Block diagram 13. Digital control.

Finally, a PWM peripheral was emulated by converting the integer control signal into a duty cycle and fed into an identical block as in the analog version. Here the control signal which has an amplitude of 1 was additionally multiplied by a supply voltage to more accurately match the output of a PWM peripheral. In practice, the PWM output amplitude would be the uC supply voltage, which is then used to control a gate driver. In this simulation the gate driver is foregone for simplicity's sake. Instead, the PWM peripheral outputs an amplitude that the driver would output. In some purpose built uCs, the gate driver could also be built-in.



Block diagram 14. PWM peripheral emulation.

6 Requirements

This chapter tabulates the minimum requirements for the uC. This is done by experimentation to find the minimum values for key digital control parameters where the PFC converter performance is still acceptable.

Table 2 lists requirements for the PFC in a prioritized order. Power factor and harmonics requirements come from 2.4.

Table 2. Digital PFC requirements.

Requirement	**Priority**	**Criteria**	**Notes**
Power factor	Must	>0.98	Datasheet
Harmonics	Must	No order of harmonic shall pass their limit level	EN IEC 61000-3-2
Efficiency	Must	>95%	
Interconnectivity	Must	Communication to secondary control, eg. UART	
Cost	Should	Similar cost to LT1248	
Ease of implementation	Could	Minimal changes in circuitry	

6.1 Minimum requirement experimentation.

By examining the logic blocks and from previous experience, the key parameters relating to control that will affect uC choice were identified to be; the architecture bit count, the A/D conversion frequency and bit resolution, switching frequency and PWM bit resolution, and finally the clock frequency of the microcontroller core.

The latter of which for a required level is hard to estimate based on simulation due to varying instruction sets and implementation. For the simulation A/D conversion frequency was also used for the control logic blocks, with the

assumption that the uC manages to perform the required calculations each cycle.

There is also the choice to be made between 16-bit and 32-bit uCs. The control algorithm was designed with a 32-bit uC in mind. Generally speaking a 32-bit uC would be an obvious choice, they can run the algorithm with fewer cycles compared to a 16-bit uC and generally are designed to run with higher clock frequencies. This means that a 32-bit uC would have a lot more overhead and enable expansion. A 16-bit uC also no longer holds a considerable pricing advantage. However, the 16-bit uC landscape is still explored incase they provide large enough use case specific advantages to consider implementation with a 16-bit uC. But the rest of the requirements are derived with the assumption fo a 32-bit uC.

The values for the A/D conversion and PWM peripheral were experimented with to find the minimums that still produced acceptable results. The switching frequency was fixed at 100kHz, but it does affect the required timer frequency of a possible uC, due to the relation of frequency and resolution in PWM.

16-bit AD conversion and PWM resolutions and 500kHz AD conversion frequency were chosen as the starting points to start reducing from step by step. The converter is simulated for a period of 0 to 500ms and steady state power factor is measured as mean over the last 100ms.

Table 3. Effect of bit resolutions on power factor.

ADC bits	**Avg PF t=0.4…0.5**	**PWM bit resolution**	**Avg PF t=0.4…0.5**
16	0.985	16	0.990
12	0.984	12	0.991
10	0.984	10	0.990
8	0.985	9	0.989
		8	0.991

Lowering the AD conversion and PWM bit resolutions do not have a huge impact on the PFC performance. So, the PWM bit resolution can be as low as 8 bits, but the highest that a possible uC can perform 100kHz switching with should be selected. For example, 8 bits would require a 25MHz timer or with a 48MHz timer with a top counter value of 48MHz/100kHz = 480 < 2^9 could be used.

The AD converter bit resolution also did not have a significant impact, therefore, anything between 8 and 16 bits could be used. The criteria affecting ADC resolution the most, could also be pricing with higher resolutions raising uC cost.

Next step was to find the combination with the lowest combination of these 3 parameters. Based on the earlier analysis, PWM resolution was set to 9 bits. For ADC bit resolution 10 bits were selected through the ubiquity, and the possibility of using a 12-bit resolution instead if need be.

The most critical parameter to lower was the ADC frequency because it also creates timing constraints for algorithm calculations.

The simulation is performed at 1MHz and the AD sampling time needs to be a integer multiple of the simulation sampling time. Therefore, the following AD frequencies were tested.

Table 4. Effect of A/D sampling frequency power factor.

AD frequency (kHz)	**Avg PF t=0.4…0.5**
250	0.992
125	0.985
100	0.990
62.5	0.977
50	0.975

According to Table 4 to keep power factor over 0.98, a sampling frequency of 100kHz or over should be used. This coincides with the switching frequency and indicates that a measurement per cycle is desired.

Effect of sampling frequency is not investigated further due to acceptable results, but there is a point to be made about the timing of the sampling within a switching cycle. By varying the timing, so that the current is measured at $T_{ON}/2$ each cycle, would result in the most accurate average current measurement. However calculating the time until next measurement from the current result, is problematic in such a realtime environment.

Other considerations include supply voltage, communication, isolation. The uC is situated in the primary side of the power supply, so the environment can be electrically noisy and a higher supply voltage is more immune to noise. The chip to be replaced LT1248 uses a higher supply voltage than most uCs. So the method of supplying voltage is an important factor to keep in mind when future work on implementation is done. As for this thesis, both 3.3V and 5V uCs were considered, but 5V is preferred when possible.

At least one built-in protocol capability should be available for communication with secondary side control. As for which ones, was not in the scope of this thesis as long as it can be isolated, even with external components. Generally all uCs can communicate using at least by using universal asynchronous receiver-transmitter (UART).

When it came to estimating the clock frequency, a brute method to obtain a rough estimate was used. The control algorithm was broken down into individual instructions and estimated number of cycles per instructions were used. The cycle per instruction estimates were based on the instruction set of Cortex M3. Addition, subtracting and multiplication were estimated to be completed in 1 cycle each. For division a worst case of 12 cycles was used.

The simulation algorithm also uses block that calculates the RMS line voltage. In practice the normalized sine voltage reference could be performed more efficiently, but code efficiency was not the main focus of this thesis, outside making sure that 32-bit integers can be used. To make the estimate conservative, it was estimated that the RMS calculations alone, would take a third of the total cycles. In other words, after tallying the other calculations the resulting cycles were multiplied by 50%. The final result was, that with the instruction set used by Cortex M3 the algorithm would take around 250 cycles to calculate.

As for how this translates into a clock frequency requirement, it was decided arbitarily that the algorithm shouldn’t take up more than 50% of the A/D sampling period. With a 100kHz sampling rate and therefore a sampling period of 10µs, this means that the calculation should be done in 5µs. This leaves 20ns per instruction, corresponding 50MHz clock frequency. With such a conservative estimation, even the common clock frequency of 48MHz could do.

Finally the two other PFC requirements that are must haves besides power factor, efficiency and harmonics were checked. Efficiency was around 95%, slighty lower than the 97% in LTSpice simulation, but this could be due to simscape not being very optimised for analyzing switching circuits. However it fulfills the requirement.

The harmonic levels were around double in magnitude when compared to the LTSpice simulation. They were however well below the required levels.

6.2 uC requirements

This subchapter defines the minimum requirements for uC properties including but not limited to, clock speed, analog-to-digital conversion resolution and channels, communication features, and so on.

Table 5. uC requirements.

Requirement	**Criteria**	**Notes**
AD channels	≥4	At least one per each measurement to do, including possible temperature measurements.
AD resolution	≥10-bits	A 10-bit resolution might be preferred over 12 in a SAR A/D converter for speed
AD conversion time/ksps	1.67µs/2,5µs 600ksps/500ksps	Depends on number of A/D peripherals.
PWM resolution @100kHz	≥10-bits	
Data width	32-bits with exceptions	
Clock frequency	≥48MHz	
Flash memory		No benchmark to base criteria on
Lifetime	Recommended for new designs	
Communication	≥1 supported protocol	
Supply voltage	3.3V-5V	5V preferred over 3.3V
Multiple sources	≥1 suppliers	

7 Exploring uC choices

7.1 Approach

With clearly listed requirements next step was to search for uC candidates. The approach was to browse through the offerings of reputable chip manufacturers. General uC families and ones specializing in digital power and motor control were mostly of interest.

From the suitable product families, the series' that best fit the requirements were picked out and compared in table format. Costs were mostly collected from Mouser's offerings and are all unit prices. They are however not entirely comparable, with order quantity ranging from single pieces to reels. Therefore the whole price range has been included in this comparison. It should be noted that Mouser's listing price for LT1248 in bulk is 6-7€.

7.2 Findings

Around a dozen suitable uC series were identified. They key columns were color coded to represent suitability.

From Microchip's product offerings the most suitable choice is single core dsPIC. They are designed for digital signal processing (DSP) purposes in real time environments. They have the most individual ADC units out of all the listed candidates, with a speed comparable to the fastest units. It is a 16-bit device but, has a high enough clock frequency and come with DSP accelerating instructions so that computational performance should not be an issue.

Texas Instruments has a F2800x family of realtime uCs. They have good analog peripherals with multiples units providing the ability to perform concurrent conversions, and satisfactory performance. The TMS320F280013x series is also relatively low cost. The only downside is the 3.3V supply voltage, but with it being a rare offering in general, it can be negated.

Infineon's lineup's only suitable products were the XMC4100 and XMC4200 series. They are generally very average overall, not a bad choice by any means.

STMicroelectronics STM32 uCs are essentially an industry standard in the 32-bit market. So it is not surprising that they have suitable offerings. F3 and G4 families are designed for mixed signal applications, e.g. digital power and motor control. They provide good ADC peripherals and the cost is very average. If the cost factor is heavily weighted, a lower cost G0 family, with slightly worse ADC peripherals could also be considered.

The last manufacturer whose products were explored is Renesas. They provide the only suitable families that could operate with 5V supply voltage. However, their ADC peripherals were bit lacking compared to others and the costs are generally higher.

Table 6. Explored microcontroller families.

Manufacturer	Family	Series	CPUf [MHz]	Flash [kB]	ADC units/channels	ADC resolution/speed [bits/ksps]	Designed application	Notes	# of sources	Cost €	Supply voltage [V]
Microchip	32MX		40-120	32-512	1/10	1100	General purpose		>1	3,08-12,71	3,3
	24EP		60	32-512	1/6-16	10-12/1100-500	General purpose	16-bits	>1	1,88-12,50	3,3
	dsPIC	dsPIC33CK	100	32-256	3 / 12-19	12 / 3500	DSP	16-bits	>1	1,85-4,92	3,3
Texas instruments	TMS320F280013x		100-120	64-256	2/ up to 21	12 / 4000	Industrial AC-DC, Motor control, others		1	0,79-1,29	3,3
	TMS320F28002x		100	32-128	2 / up to 16	12 / 3450	Real time applications		>1	3,40-6,93	3,3
Infineon	XMC4000	XMC4100/4200	80	64-256	2 / 16	12 / 4000	Motor control / Power supplies	Well stocked	1	3,43-8,04	3,3
STMicroelectronics	F3	STM32F334x4	72	16-64	2 / 10-21	12 / Up to 5000	Digital power	Well stocked	>1	3,20-7,39	3,3
	G4	STM32G431x	170	32-128	2 / 11-23	12/ 4000	Motor control / Digital Power		1	3,23-8,27	3,3
	G0	STM32G0B1	64	512	1 / 16	12 / 2000			>1	0,86-5,14	3,3
Renesas	RX26T		120	128-512	2 / 8	12 / 1100	Motor control	Not very well stocked	1	4,51-911	3,3/5
	RA	RA4M1 (CM4)	48	256	1 / up to 25	12-14 / 1000			1	3,18-6,39	3,3/5
	RX660		120	512/1024	1 / 24	12 / 1000			1	4,23-10,10	3,3/5

7.3 Recommendation

Based on exploration, the recommended first choice of manufacturer would be STM. They offer the best range of products overall for the purpose and allow to

choose between performance and cost while staying within a single manufacturers environment. Cost and performance wise both dsPIC and TSM320F280013x are both also good choices, but leave less room for alternatives. Infineons XMC4000 family has a similar issue of little to no alternatives without changing the development environment, while offering no large benefits compared to STM.

8 Conclusion

The aim of this thesis was to explore practical considerations when implementing a completely digital control loop with a uC and produce a chip recommendation. During this endeavour, multiple simulation environments that can be used to simulate such a preregulator were used to characterize the key parameters in a control loop, and how they limit the choice of a uC. This work resulted in the recommendation of choosing STMicroelectronics F3, G4 or G0 family of uCs to begin implementation.

The exploration of uC choices highlighted that the range of devices available today is vast and this allows a designer to balance cost with performance and features. However, a digital PFC at the moment is not necessarily a suitable solution when low cost is heavily emphasized. On the contrary, whenever performance is prioritized over cost, implementing a digital PFC is warranted and even a required step to achieve the highest possible performance due to its realtime adaptability.

In conclusion, in today's energy-conscious world, power factor correction plays a crucial role in modern power supplies. By utilizing the flexibility and performance of contemporary microcontrollers (uCs), we can achieve the highest possible efficiency in these devices.

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