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Parasitic Components in PCB Design

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Abstract

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Parasitic components are often unwanted circuit elements that can lead to performance issues in high-speed designs. The goal of this study was to provide an overview of parasitic components, their causes and effects with examples of commonly found issues.

The study was conducted through reviewing textbooks, application notes, and datasheets. Selected examples were provided on frequently encountered topics. Examples on parasitic resistance, parasitic inductance, and parasitic capacitance were identified.

Key findings highlight the impact of parasitic components to signal integrity issues, such as crosstalk. Additionally, parasitic components were found to contribute to power integrity issues and losses in power distribution networks.

This report highlights the need for understanding parasitic components in modern electronics design. The insight from this report aims to aid aspiring PCB designers spot and mitigate these issues, improving circuit reliability.

Keywords: PCB design, parasitic components, crosstalk

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Parasiittiset komponentit ovat usein ei-toivottuja komponentteja, jotka voivat vaikuttaa piirin toimintaan. Tämän opinnäytetyön tavoitteena oli tarjota yleiskatsaus parasiittisiin komponentteihin ja niiden vaikutuksiin esimerkkien avulla, jotka kuvaavat yleisimmin esiintyviä ongelmia.

Opinnäytetyö suoritettiin tarkastelemalla oppikirjoja, komponenttivalmistajien julkaisuja sekä datalehtiä. Esimerkit valikoituivat usein ilmenevistä aiheista. Esimerkkejä sisällytettiin parasiittisesta resistanssista, parasiittisesta induktanssista ja parasiittisesta kapasitanssista.

Keskeiset havainnot korostavat parasiittisten komponenttien vaikutusta signaalin eheyteen, kuten ylikuulumiseen. Lisäksi parasiittisten komponenttien havaittiin vaikuttavan tehonsyötön eheyteen ja aiheuttavan häviöitä.

Tämä raportti korostaa parasiittisten komponenttien ymmärtämisen tärkeyttä nykyaikaisessa elektroniikkasuunnittelussa. Raportti tarjoaa tietoa tukemaan tulevia piirilevysuunnittelijoita tunnistamaan ja minimoimaan parasiittisten komponenttien aiheuttamia ongelmia.

Avainsanat: piirilevysuunnittelu, parasiittiset komponentit, ylikuuluminen

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List of Abbreviations

DC: Direct Current.

HDMI: High-Definition Multimedia Interface.

IC: Integrated Circuit.

MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor.

PCB: Printed Circuit Board.

PCIe: Peripheral Component Interconnect Express.

PDN: Power Distribution Network.

USB: Universal Serial Bus.

1 Introduction

Parasitic components are often unwanted circuit elements, such as resistors, inductors, and capacitors emerging in printed circuit board (PCB) design. These parasitic circuit components arise due to the inherent properties and dimensions of the design. The addition of these undesired circuit components can alter the intended operation of the circuit. [4,29-33.]

Increasing frequencies and the decreasing rise-times in digital circuits drive the need for the designer to consider parasitic components to maintain signal integrity [4,10]. Delivering stable supply voltage to various integrated chips (IC) set design requirements for the power distribution networks (PDN) [13,263-265]. Understanding parasitic components enable the designer to better approximate and simulate the behaviour of the circuit.

The aim of this study was to investigate parasitic components in PCB design, identifying the different parasitic components and the contributing factors for their occurrence. The goal was to produce a report serving as an introduction to parasitic components and their effects while providing common examples of their occurrence in PCB design.

The structure of the report begins with the fundamentals of various circuit components in chapter 2, to provide basis for understanding how parasitic components are formed. Chapters from chapter 3 through chapter 5 explore the various parasitic components with examples of each.

The topic was chosen as it provided an opportunity to provide insight about a topic applicable to all future design projects and especially PCB layouts. The combination of personal interest in improving PCB layout skills and the general applicability of broadening the understanding on parasitic components led to the selection of the topic.

2 Fundamentals of R, L, C and Z

This chapter introduces the following electrical quantities: resistance (R), capacitance (C) and inductance (L). The quantities are discussed through approximations and practical rule of thumbs with a focus on printed circuit board (PCB) design. The electrical quantities are modelled by pure and linear, ideal circuit elements. The Impedance (Z) of each ideal circuit element is discussed in the related subchapter. In the following chapters, the knowledge of these ideal circuit elements is used to discuss parasitic components in PCB design.

2.1 Resistance

The resistance of a conductor depends on the physical dimensions of the conductor and the bulk resistivity of the material. Bulk resistivity is measured in ohm-metres and is commonly denoted with ρ . It is a result of atomic collisions converting electron motion into thermal motion. [1,377-378;2.] Table 1 shows the bulk resistivities of some common metals.

Table 1 Bulk resistivities of common metals [2;3].

Material	Resistivity (at 20°C) (Ωm)
Silver	$1.626 \cdot 10^{-8}$
Copper	$1.724 \cdot 10^{-8}$
Gold	$2.01 \cdot 10^{-8}$
Aluminium	$2.803 \cdot 10^{-8}$
Tin	$10.1 \cdot 10^{-8}$

Resistivity can be defined with respect to the electric field strength E and current density J, as shown in equation (1). Electric field strength is expressed in V/m and current density in A/m². In equation (1), l is conductor length and A is the cross-sectional area. [4, 38-39.]

$$\rho = \frac{E}{J} = \frac{V}{I} \cdot \frac{A}{L} \quad (1)$$

Resistance per length and sheet resistance are useful approximations in PCB design. The resistance of a trace on a PCB is proportional to its length, assuming it has a uniform cross section. The resistance per length of a conductor with uniform cross-sectional area (A) is given by equation (2). Where R_{sq} is the sheet resistance, w is the trace width. [2;4,39-41.]

$$R_L = \frac{\rho}{A} = R_{sq} \cdot \frac{1}{w} \quad (2)$$

The traces on a typical PCB are formed by etching a sheet of copper foil bonded to insulating substrate [5]. The copper sheet thickness is often expressed as copper weight in ounces, with one ounce and half ounce copper sheets being some common copper weights. Sheet with copper weight of one ounce weighs an ounce per square foot. Thickness of 1 oz copper is approximately 35 μm and the thickness of 0.5 oz copper is approximately 17.5 μm . The resistance of the sheet depends on the bulk resistivity of the sheet material and its thickness. Sheet resistance (R_{sq}) is a term used to describe the resistance of a square of the sheet material. If the sheet resistance is known, it can be used to calculate trace resistance per length of trace, shown in the right-hand side of equation (2). [2.]

Assuming fixed length and cross-sectional area, equation (1) gives resistance R as the ratio of voltage and current, as it is given in Ohm's law. Resistance is frequency independent for direct current (DC). Resistance forms the real component of impedance. The imaginary component of impedance is termed reactance (X). It is composed of capacitive and inductive reactance, both frequency dependent. These quantities are discussed in the following chapters on inductance and capacitance. [6.]

2.2 Inductance

Maxwell's equations describe the fundamental relations between magnetic fields and currents, as well as between electric and magnetic fields [7, 83-86]. Inductance (L) relates the ratio of number of magnetic field lines around the conductor to the current (I) through the conductor. Figure 1 illustrates the magnetic field lines around a current carrying conductor.

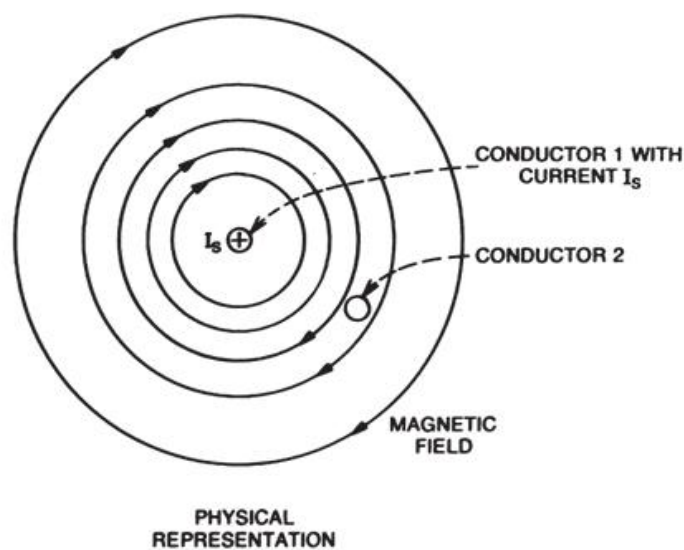


Figure 1. Magnetic field lines around a current carrying conductor. Image from [8].

The unit of inductance is henry (H), and it is the ratio of magnetic flux (ϕ) measured in webers (Wb) to current (A) through the conductor. [4,46-47;2.] The magnetic flux generated by the current can be expressed as [8,52]:

$$\phi_T = LI \quad (3)$$

The term self-inductance is used when the magnetic flux is caused by the current through the same conductor. Self-inductance of a conductor is given by equation (4) [8,52]. If the magnetic flux is caused by another conductor, term mutual inductance is used. Mutual inductance between circuits 1 and 2 caused

by current through circuit 1 is given by equation (5). [4,47.] Loop inductance is the inductance of an entire current loop [2].

$$L = \frac{\Phi_T}{I} \quad (4)$$

$$M_{12} = \frac{\Phi_{12}}{I_1} \quad (5)$$

An ideal inductor does not have resistance, its impedance is described solely by inductive reactance. Inductive reactance can be calculated using equation (6): [3.]

$$X_L = j\omega L = 2\pi fL \quad (6)$$

Where f is the frequency in Hz and L the inductance in H. Due to the frequency dependent impedance, inductors are commonly utilized in filtering applications. Inductors are also energy storing devices. As the current through an inductor increases, the energy (W) stored in its magnetic field increases. [3.]

$$W = \frac{1}{2}LI^2 \quad (7)$$

Decrease in current leads to the collapse of the magnetic field, releasing the stored energy. As the magnetic field changes, it induces a voltage across the inductor. This voltage causes the inductor to oppose changes in the current through it. [3.] Due to this property, power inductors are used to reduce ripple current in power supplies [19]. The relationship between the inductance, change in current and the induced voltage is described in equation (8) [3].

$$V = L \frac{dI}{dt} \quad (8)$$

In summary, inductance quantifies a conductor's ability to generate a magnetic field when a current flows through it and to resist changes in current by inducing a voltage. The inductive reactance is greater for increasing frequencies. Inductors are used as filters and energy storage applications.

2.3 Capacitance

Two parallel conductors with a voltage between them store charge.

Capacitance (C) is a measure of the charge stored between the conductors per voltage. Capacitance is measured in Farads (F). [9,18; 2.]

$$C = \frac{Q}{V} \quad (9)$$

Where Q is the total charge in Coulombs and V is voltage in Volts. The actual capacitance is dependent on the conductor geometry and dielectric material near the conductors. The parallel plate approximation illustrated in Figure 2 is a common approximation for capacitance. It approximates the capacitance of two parallel plates with area (A), separated by distance (d). In equation (9), ϵ is the permittivity of the dielectric separating the plates. [2;10,123.]

$$C = \epsilon \frac{A}{d}, \quad \epsilon = \epsilon_0 \cdot \epsilon_r \quad (9)$$

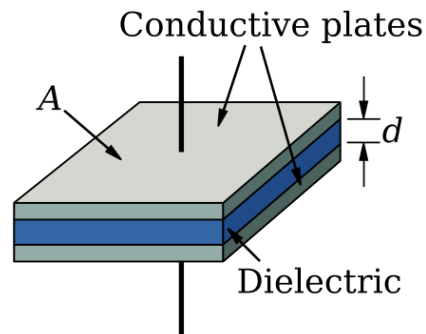


Figure 2. Parallel plate capacitor [11].

Dielectric materials are electrical insulators that polarize in an electric field [12,109]. From equation (8), increasing the dielectric constant or decreasing the separation of the plates will result in increased capacitance. Current through capacitor is related to the rate of change of voltage over it and its capacitance. It can be described by equation (10). [12,171-172.]

$$i = C \frac{dV}{dt} \quad (10)$$

Equation (10) states that current through a capacitor, requires a changing voltage. Impedance of an ideal capacitor is described by its capacitive reactance presented below. As expected, based on equation (10), the reactance is inversely proportional to the frequency. [3.]

$$X_C = \frac{1}{j\omega C} = \frac{-1}{2\pi fC} \quad (11)$$

The current flow through a capacitor, with insulating material separating the conductors, requires the introduction of a term called displacement current [2]. Displacement current is a concept found in the Ampère's law in Maxwell's equations. While conduction currents involve movement of charges, displacement current refers to a time-varying electric field that induces a magnetic field, like conduction current. It does not require physical charge movement through the insulating material of the capacitor. [12,286-287.] This concept has implications in PCB design, where traces on the PCB are separated by a dielectric material, essentially forming a capacitor. This capacitance between circuits is called mutual capacitance. [13,25.]

2.4 Impedance

Impedance (Z) is a complex quantity, combining resistance and reactance to describe the frequency dependent opposition of current. Resistance forms the real part of impedance while capacitive and inductive reactance form the imaginary part. [9,40-42.]

$$Z = R + jX \quad (12)$$

In PCB design, the term characteristic impedance is of importance. It relates the geometrical and material properties of the transmission line to the impedance seen by a signal as it moves along the transmission line [9,1116-1117]. Use of controlled impedance traces is common in various digital communications

standards such as Universal Serial Bus (USB), High-Definition Multimedia Interface (HDMI), and Peripheral Component Interconnect Express (PCIe) [14].

$$Z_0 = \sqrt{\frac{L'}{C'}} \quad (13)$$

Equation (13) calculates the characteristic impedance (Z_0) of a lossless transmission line. L' and C' are the inductance and capacitance per unit of length, respectively. From earlier chapters on inductance and capacitance, we can tell that the characteristic impedance is affected by factors such as the dielectric thickness in the PCB and trace geometry. [13,143-144.]

3 Parasitic Resistance

Parasitic resistance occurs on the PCB due to material properties. For example, traces on the PCB have series resistance per unit of length. As discussed in chapter 2.1, this series resistance depends on the physical dimensions of the trace. [2.] As traces have resistance, any current through a trace will result in a voltage drop across the trace. This leads to conduction losses, and heating of the trace [15,27-29]. Resistivity of traces increases with temperature [15,21]. This has implications particularly when designing power distribution networks (PDN). Figure 3 illustrates the DC resistance of 1 oz and 0.5 oz traces.

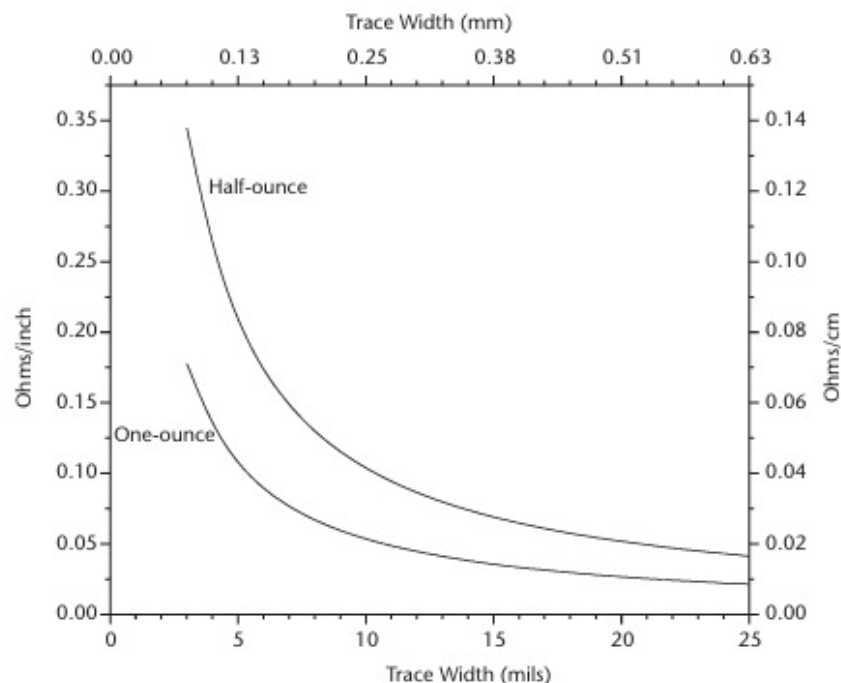


Figure 3. DC trace resistance per length of 1 oz (35 μ m) and 0.5 oz (17.5 μ m) traces. Image from [22].

Although resistance is not frequency dependent, the resistance of a PCB trace is when high enough frequencies are reached. The frequency dependence of trace series resistance is caused by the skin effect. For PCB traces with 1 oz copper weight, skin effect starts to take hold around 10 MHz. [13,151-154.] This is illustrated in Figure 4 below.

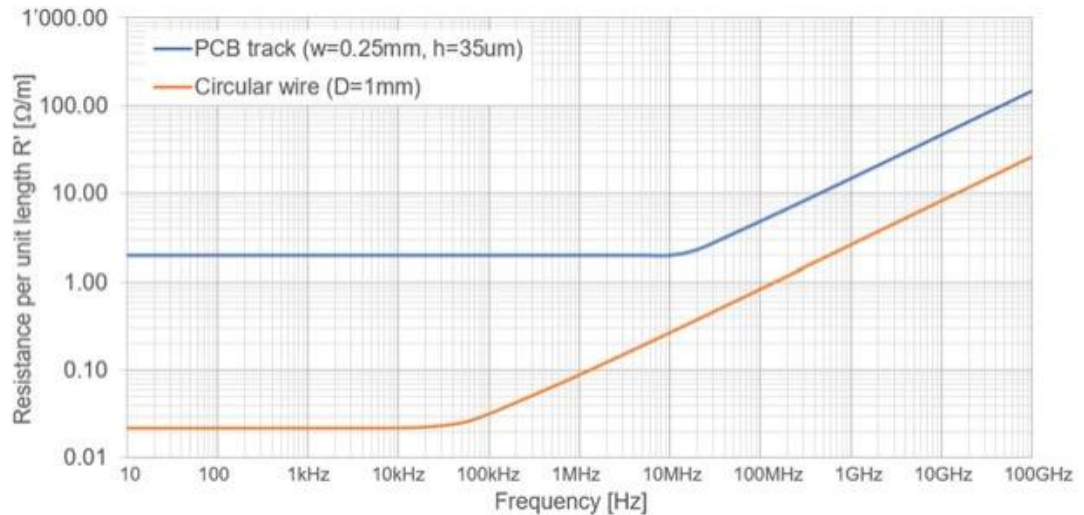


Figure 4. Frequency dependence of resistance due to skin effect. Image from [17].

The skin effect is caused by eddy currents that form in the conductor due to the changing electric fields induced by the changing magnetic field around the current carrying conductor, according to Faraday's law. The direction of eddy currents is such that they oppose the changing magnetic field, which causes them to oppose the main current. [13,151-156.]

The self-inductance of the trace is larger near the centre of the conductor, which in turn causes the eddy currents to be stronger near the centre. This causes the current density to be higher near the edges of the conductor, effectively decreasing the cross-sectional area of the conductor. Higher frequencies result in stronger eddy currents, which makes resistance appear frequency dependent. [2;13,151-156.]

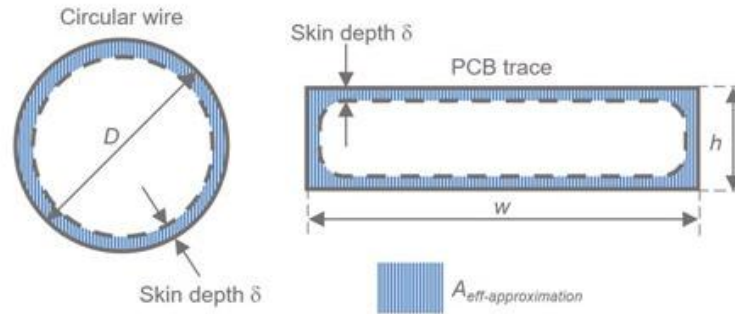


Figure 5. Effective cross-sectional area due to skin effect. Image from [17].

The effective cross-sectional area of a PCB trace illustrated in Figure 5 above, can be estimated using equation (14) below [17,140].

$$A_{\text{eff}} = 2\delta(w + h) - 4\delta^2 \quad (14)$$

Where δ , is the skin depth of the trace in metres, w is the width of the trace in metres, and h is the height of the trace in metres [17,140]. As discussed above, the current carrying capacity of a trace depends on the cross-sectional area. In this case doubling the height of the trace, would double the cross-sectional area. However, if frequency is high enough for skin effect to matter, doubling h in equation (14), would not double the effective area. Keeping the trace height the same while using two layers would yield in a higher effective area than simply doubling the height of the trace.

As a conclusion, parasitic resistance is frequency dependent due to skin effect and the resistivity of copper increases with temperature. It affects the circuit performance by attenuating signals, leads to heating of the traces, and degrading PDN performance. To mitigate the effects of parasitic resistance, the current carrying capacity of the traces should be considered.

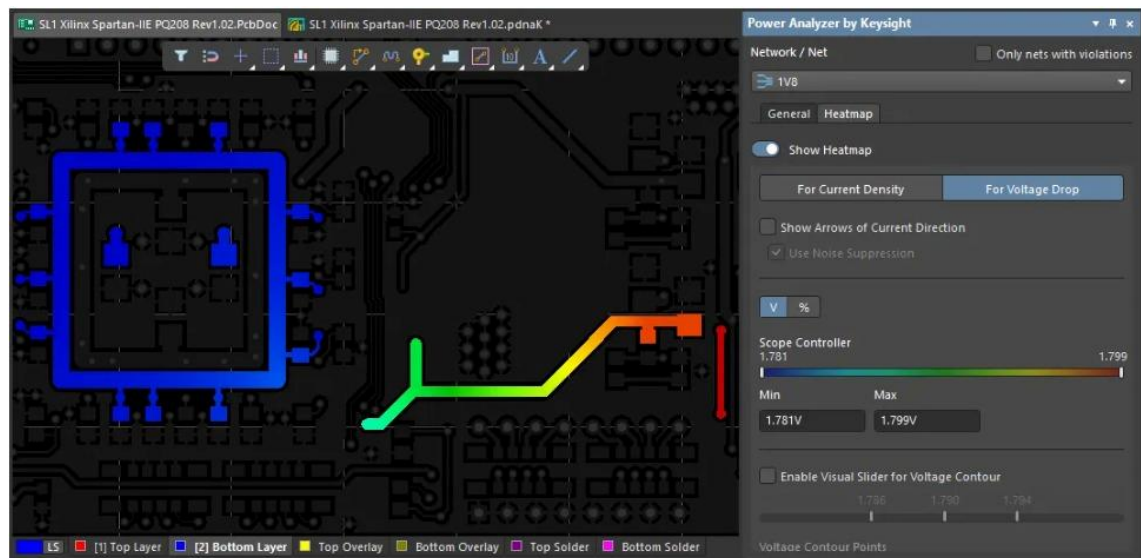


Figure 6. Heatmap of voltage drop on a 1.8V net, simulated on Power Analyzer by Keysight. Image from [23].

The IPC-2152 standard for determining current carrying capacity in printed circuit board design is a general guide that can be used to aid in determining conductor sizes for current carrying capacity and temperature change. The standard covers current carrying capacity of vias on multilayer PCBs as well. [16.] Various simulation tools exist to simulate PDN voltage drop, current densities and resistances from the PCB layout, such as Power Analyzer by Keysight for Altium Designer, presented in Figure 6 above, and HyperLynx by Siemens Digital Industries Software.

4 Parasitic Inductance

Traces on a PCB have series inductance associated with them. In a closed loop consisting of a signal conductor and a return conductor, the signal conductor part of the loop will have some partial self-inductance (L_a), which represents the number of magnetic fields around that part of the loop per Ampere of current through it. The return conductor will have its own partial self-inductance (L_b). [2;18.]. The partial self-inductances and their mutual inductance are illustrated in Figure 7.

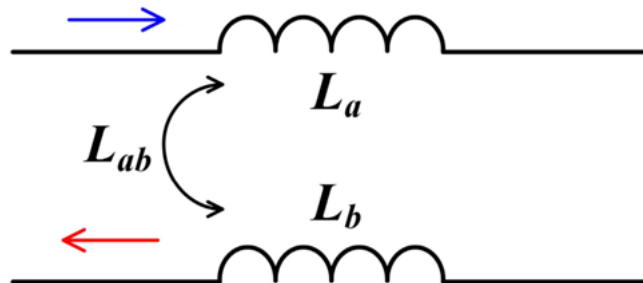


Figure 7. The partial self-inductances of the signal and return conductor and their mutual inductance. Adapted from [24].

As discussed in chapter 2.2, the amount of magnetic coupling between these two conductors determines their mutual inductance (L_{ab}). The loop inductance can be calculated with the partial self-inductances of the conductors and the mutual inductance between them. [2;18.]

$$L_{\text{loop}} = L_a + L_b - 2L_{ab} \quad (15)$$

The partial mutual inductance between two round conductors can be approximated using equation (16), which is a second-order model. M is the partial mutual inductance in nH, d is the length of the conductors, and s is the centre-to-centre separation. [2.]

$$M = 5d \left(\ln \left(\frac{2d}{s} \right) - 1 + \frac{s}{d} - \left(\frac{s}{2d} \right)^2 \right) \quad (16)$$

The equation can be simplified if the distance between the conductors is small compared to their length. This simplified, first-order model is presented in equation (17). [2.]

$$M = 5d \left(\ln \left(\frac{2d}{s} \right) - 1 \right) \quad (17)$$

If the length of the conductors is kept constant, and the separation between them is increased, the mutual inductance decreases. Figure 8 compares the above approximations against a field solver.

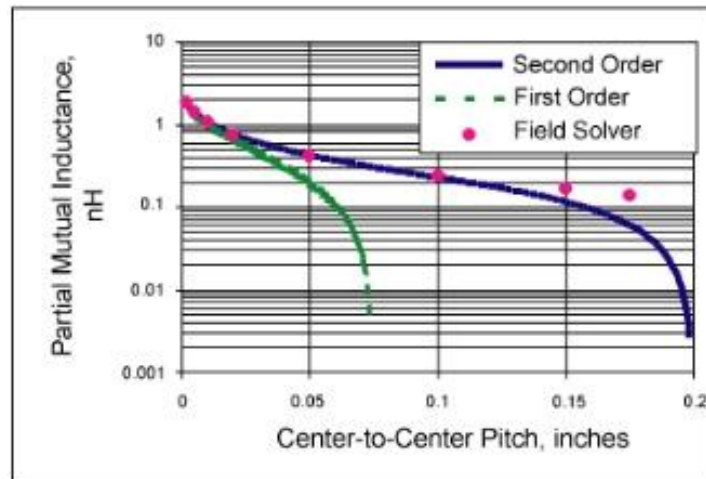


Figure 8. Partial mutual inductance between two round 0.1-inch conductors [2].

Two current loops with the same loop area can have a difference between their loop inductances. As expressed in equation (15), the loop inductance can be decreased by increasing the mutual inductance between the signal path and its return path. To decrease the mutual inductance, the separation between the signal and return paths should be decreased, as presented in Figure 8. [2;18.]

4.1 Ground Bounce

Ground bounce is a type of switching noise induced by the return current and the parasitic inductance in the return path [20,368]. From chapter 2.2., the voltage induced is proportional to the inductance of the current path and to the rate of change of the current. One occurrence of ground bounce can be found between the ground of an integrated chip (IC) and the ground of the PCB the IC is connected to. [21,1-2.]

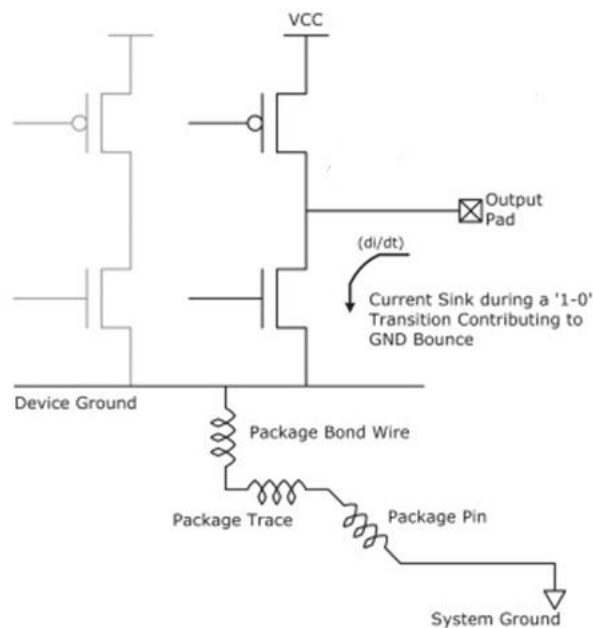


Figure 9. Parasitic inductances of an output buffer. Image from [21].

Figure 9 demonstrates the parasitic inductances between the IC ground and the system ground. The total parasitic inductance is the sum of the three inductances in the figure. The rate of the switching current, labelled di/dt , is the current the output buffer is sinking during a high-to-low transition. [21.]

From equation (8) in chapter 2.2, a voltage is induced with a changing current through an inductor. The voltage induced is greater for larger total parasitic inductance and for faster switching speeds. The induced voltage is also greater if the return path is shared by multiple simultaneously switching signals. To reduce ground bounce, either the total inductance, the number of signals

sharing the return path, or the rate of change of the current must be reduced. [2;21.]

Figure 10 demonstrates the effect of slew rate on the ground bounce. The slew rates in (a) and (b) are approximately 1.5V/ns and 0.75V/ns, respectively. The figure shows a reduction of around 75% reduction in ground bounce amplitude from (a) to (b) [21]. This demonstrates the effectiveness of decreasing slew rate in reducing ground bounce. However, it is always not possible to reduce slew rates of switching I/O pins. Then simultaneously switching I/Os should be spaced around the package if possible. Additionally, low inductance path to ground is optimal. [2;21.]

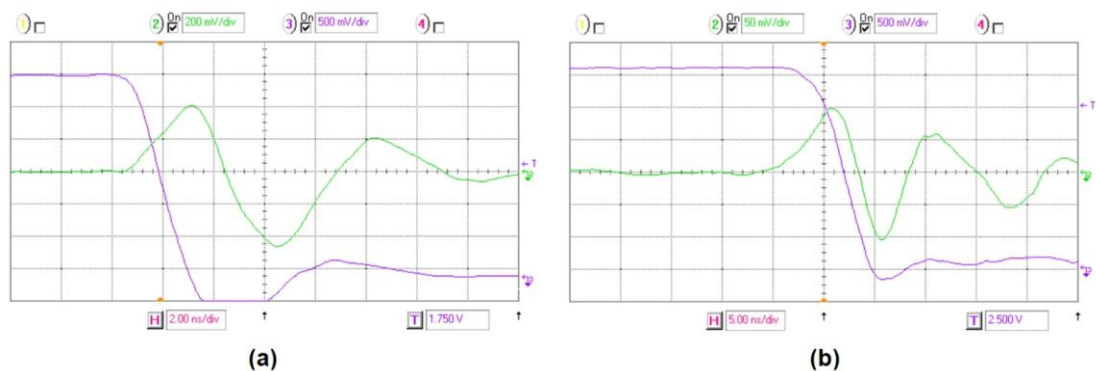


Figure 10. The effect of slew rate on ground bounce. Image from [21].

4.2 Inductive Crosstalk

Inductive crosstalk is a noise voltage induced on a victim line due to the changing current, or di/dt , on the aggressor line. It is often referred to as switching noise, as this inducing di/dt usually occurs at the rising or falling edges of a digital signal. [2; 22,107.] The induced noise voltage is dependent on the signal strength on the aggressor line and the mutual inductance per length between the conductors. It is also dependent on the velocity of the signal, as faster signal will occupy a longer region on the conductor spatially, resulting in increased coupling. [2.]

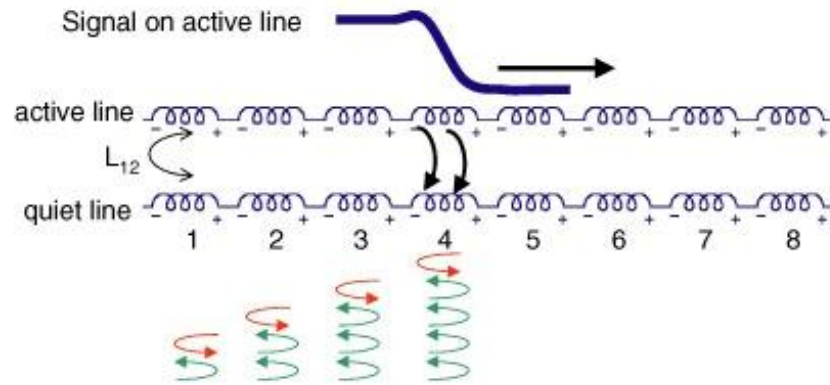


Figure 11. Inductive crosstalk. Image from [2].

Figure 11 presents the inductive crosstalk during a high-to-low transition on the active line. Partial self-inductances and the mutual inductance between the active and quiet line is shown. The induced currents travelling in both directions are displayed. The red current is induced to oppose the switching current in the active line. This current travels towards the near end on the quiet line and the noise seen is a longer lasting and lower amplitude pulse, rather than a short spike. As the edge propagates, the green currents are induced as the switching edge propagates. These currents are superimposed on top of each other and seen as a spike at the far end of the quiet line, in the case of inductive crosstalk, the far end noise has the opposite polarity to the aggressor [22,119]. The longer the coupling length of the active and quiet line, the larger is the induced spike at the far end. [2;4,113-114.] The inductively coupled crosstalk is presented in Figure 12.

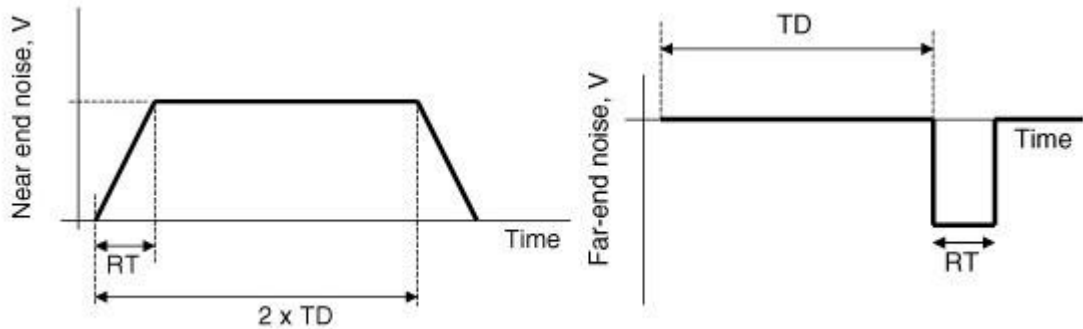


Figure 12. Inductively coupled crosstalk on a single-ended microstrip. Image from [2].

The effects of inductive crosstalk are combined with the effects of capacitive crosstalk in cases where there exists a wide, continuous return path. If the return path is not a wide continuous plane the effects of inductive crosstalk get stronger. For example, a slot in the ground plane under the traces, as presented in Figure 13 below. [4,112-114.]

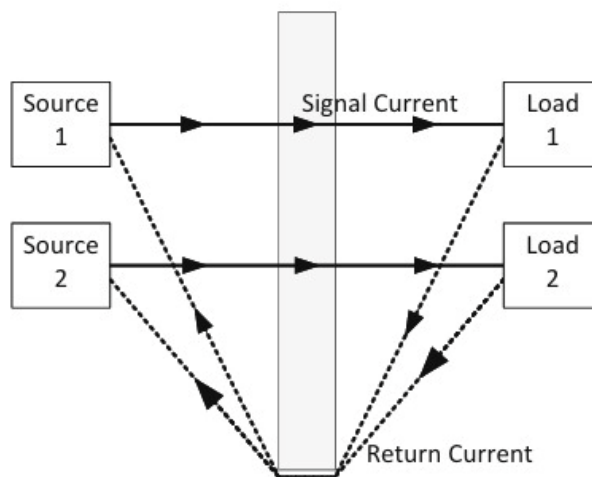


Figure 13. A slot in the ground plane alters the signal return path. Image from [4].

In the above figure, the self-inductance of all traces is increased, the loop mutual inductance between the two current loops is increased and the return currents are forced to share the return path. The increased self-inductances,

mutual loop inductances and sharing of the return path leads to increased inductive coupling and increased noise on the switching edge of the signal. [2;4,112].

To reduce inductive crosstalk, wide continuous planes should be used for return paths. Minimizing the coupling length of the adjacent traces aids in reducing the inductive crosstalk. The so called 3H rule of thumb stems from an approximation of 90% reduced crosstalk when the centre-to-centre spacing of traces is three times the height of the trace above the ground plane. [2;4,111-112.]

4.3 Decoupling Capacitors

Decoupling capacitors are used to stabilize the power delivery to devices. Capacitors store energy in their electric field, and they can act as a local energy storage for the high-speed devices when there are sudden changes in the current draw of the device. [9,633.] The capacitor's ability to respond to the transient currents of the device is limited by parasitic inductance which should be minimized [25,31]. Figure 14 shows the impedance of a capacitor modelled with equivalent series resistance (ESR) and equivalent series inductance (ESL).

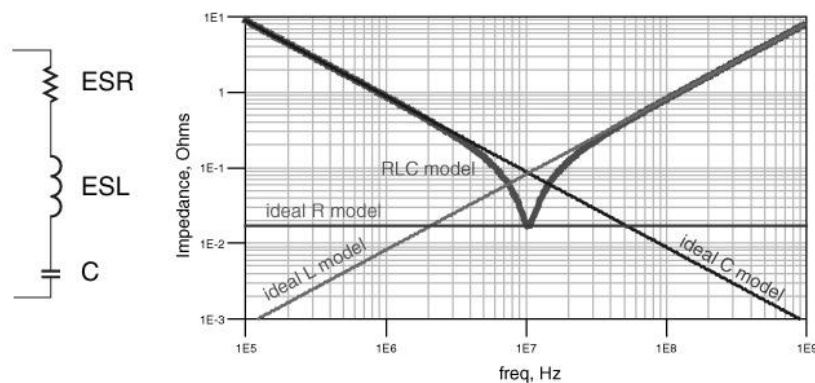


Figure 14. RLC model of a capacitor. Image from [2].

The parasitic inductance of the capacitors itself is determined by the package size of the capacitor [25,27]. In addition, large part of the parasitic inductance of the decoupling capacitor is due to the loop inductance on the PCB [2]. The loop inductance is highlighted in Figure 15 below.

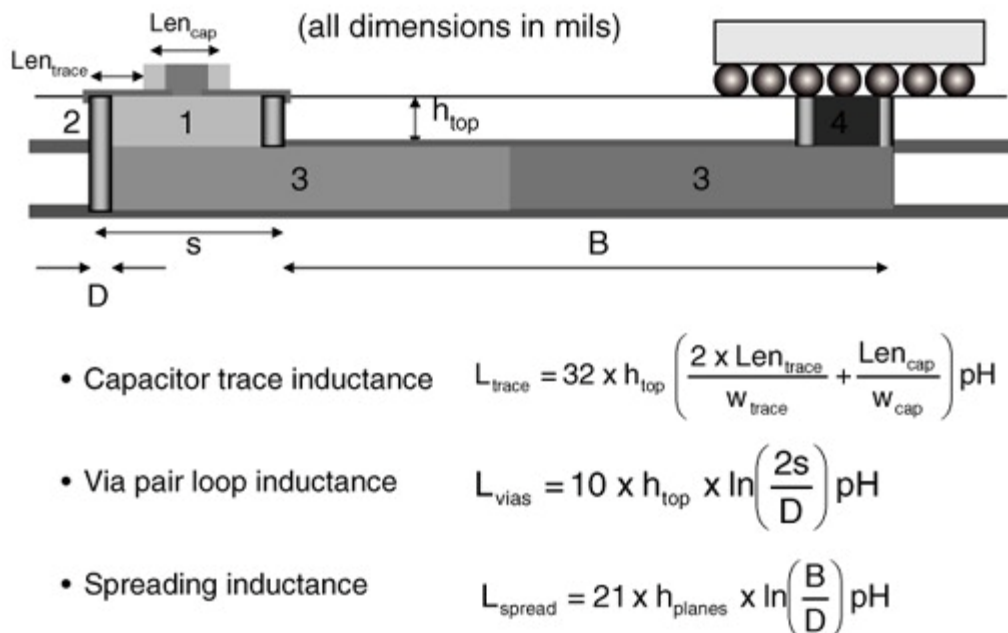


Figure 15. Estimating the parasitic inductance of a capacitor. Image from [2].

From the above figure, three different aspects of the layout can be minimized. Capacitor trace inductance can be reduced by bringing the planes closer to top layer, using shorter and wider traces, and using a capacitor with a shorter package length. Via pair loop inductance can be reduced by bringing the vias closer together, by using vias with larger diameter, and bringing the planes closer to the top. To reduce the spreading inductance, the inductance seen by the signal on a plane can be decreased by bringing the ground and power planes closer together by using vias with larger diameters, and placing the capacitors close to the component it is decoupling. [2.]

5 Parasitic Capacitance

As described in chapter 2.3, two parallel conductors have capacitance between them. Figure 16 pictures two adjacent conductors over a ground plane. The capacitances C_{1G} and C_{2G} are the capacitances of the individual conductors to the ground plane, C_{12} represents the mutual capacitance between the signal conductors.

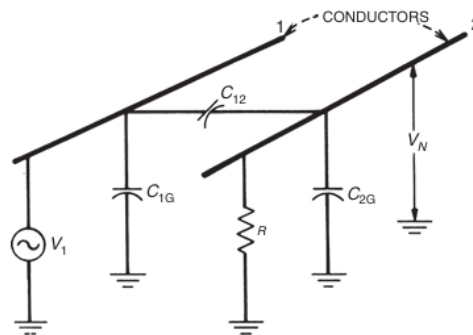


Figure 16. Capacitances between two conductors above ground plane. Image from [8].

As a reminder from earlier, capacitors store charge. The charge stored is proportional to the voltage across the conductors. When the voltage across the conductors changes, current flows through the capacitor. The impedance of a capacitor decreases as the frequency increases.

These parasitic capacitances contribute to negative effects such as crosstalk, delay and signal integrity issues. They can also be leveraged when tuning the characteristic impedance of uniform transmission lines [2;13,25.] Increasing plane capacitance between ground and power planes by bringing them closer together might be useful in reducing high frequency power supply noise [13,221].

If resistance is present with parasitic capacitance, it can add delay. The step response of RC circuits is presented in Figure 17. The product of R and C gives the time constant (τ) of the circuit. During one time constant, the circuit charges

up to 63% of V_{in} , and discharges down to 37% of V_{in} . [9,22.] Parasitic capacitances in MOSFETs together with internal gate resistance influence the switching performance of the transistor [26,1-4].

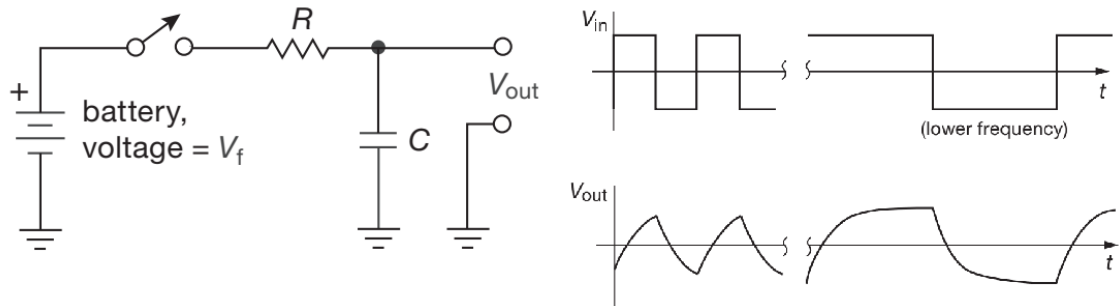


Figure 17. RC circuit with its charging and discharging behaviour. Image from [9].

The importance of minimizing inductance in decoupling capacitors to improve PDN performance was discussed in the previous chapter. The decoupling performance can be positively affected by the inter-plane capacitance between adjacent power and ground planes [13,221;25,34]. The plane capacitance can be approximated by the parallel plate approximation of capacitance given in equation (9). Using dielectric constant of 4 and area of 5 square inches, or 0.0161 square meters, and separation of 4 mils, or 0.1016 mmm the resulting capacitance is:

$$C = 8.85 \cdot 10^{-12} \cdot 4 \cdot \frac{0.0161}{0.1016} = 5.6 \cdot 10^{-9} = 5.6 \text{ nF} \quad (18)$$

If a particular application requires decoupling performance to be optimized, reducing parasitic inductances by bringing the ground and power layers closer to the PCB surface and increasing the inter-plane capacitance between ground and power layers by bringing them closer together might provide lower impedance across wider frequency range, thus reducing power supply noise. [2;25,34.]

Trace-to-plane capacitance is important to consider when designing microstrip transmission lines. A signal trace over a wide reference plane is called a microstrip line [140]. Figure 18 below illustrates how a current loop is formed on a microstrip through the capacitance to return path. [2.]

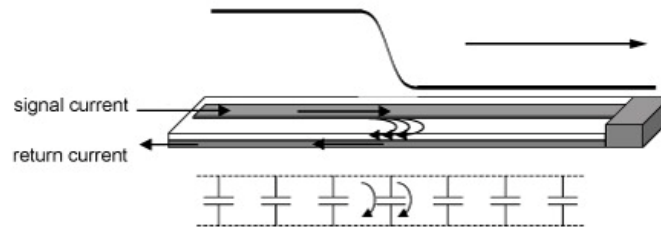


Figure 18. Signal edge propagating on a microstrip line. Image from [2].

The characteristic impedance of this uniform microstrip line is related to the ratio of inductance and capacitance of the microstrip line, as discussed in chapter 2.4. This capacitance between the trace and its reference plane is a convenient way to tune the characteristic impedance of the trace by adjusting trace thickness, dielectric thickness, or the dielectric material used in the PCB stack up.

5.1 Capacitive Crosstalk

Capacitive crosstalk is the result of the parasitic capacitance between two conductors [8,46]. Figure 19 below presents simulated electric field lines from a microstrip and the effect that the surrounding dielectric has on them. Embedded microstrip, a microstrip embedded in the dielectric, demonstrates stronger coupling between the reference plane and reduced electric field lines in the air. The surrounding dielectric influences the impedance of the trace. Increasing the dielectric constant surrounding the conductor lowers the characteristic impedance and increases the delay. [2.]

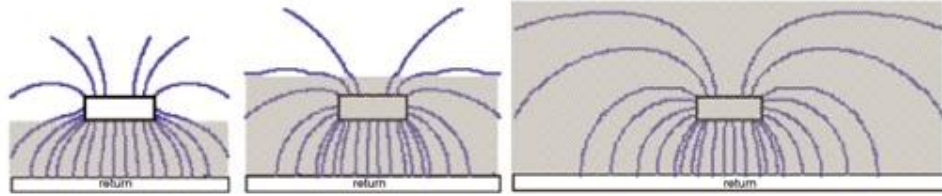


Figure 19. Fringe fields and the effect of dielectric around the trace. Image from [2].

The coupling between two conductors by these electric fields is called electric, or capacitive coupling [8,44]. Figure 20 demonstrates capacitive coupling between two conductors and the influence of spacing on the coupling.

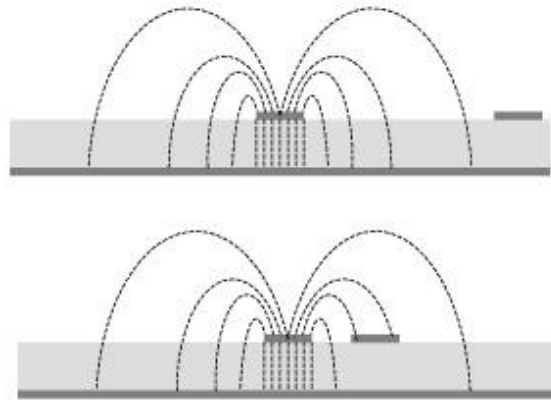


Figure 20. Fringe field strength and coupling with increasing distance. Image from [2].

The electric noise coupling mechanism is demonstrated in Figure 21. The current source represents the coupled noise current. The propagating edge depicted on the right-hand side of the figure acts as the current source for the noise as the edge propagates. The noise current is coupled through the distributed mutual capacitance within the spatial region the rise time occupies. [2;8,44-47.]

$$I_c = C_M \frac{dV}{dt} \quad (19)$$

Equation (19) describes the total current coupled through the mutual capacitance over the spatial extent of the rise time between the two conductors. The spatial region of the rise time depends on its propagation velocity, which in turn is dependent on the dielectric [13,118]. At higher velocities the rise time occupies a larger region [2].

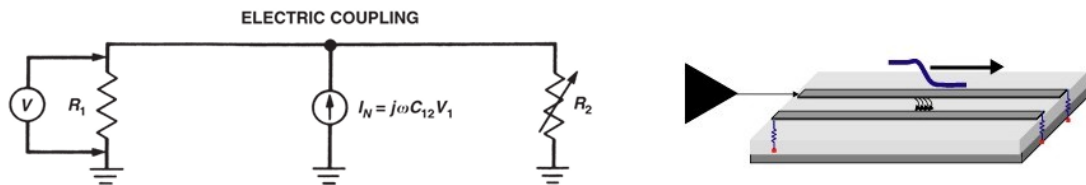


Figure 21. Capacitively coupled current on a single-ended microstrip. Adapted from [2;8].

Similarly to inductive crosstalk, the coupled noise propagates backwards and forwards. The forwards propagating noise from each distributed capacitance combine and contribute to the far-end crosstalk, proportional to the derivative of the signal causing the noise. The polarity of capacitively induced far-end crosstalk is the same as the inducing signal, opposite to the far-end crosstalk caused by inductive coupling. The backwards propagating noise is seen as a near-end crosstalk. Similarly to inductive crosstalk, it is seen as a longer pulse at the source end on the quiet line. Figure 22 illustrates the backwards and forwards propagating noise, the stacking green arrows indicate the forwards propagating noise adding together. [2;13,205-208.]

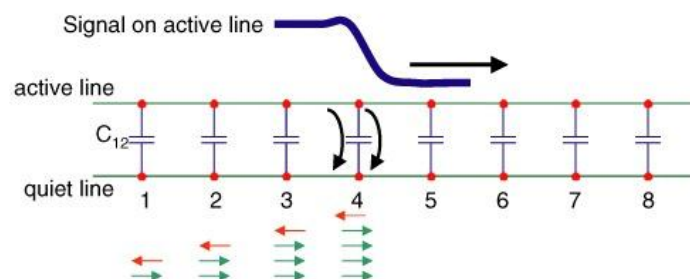


Figure 22. Capacitive crosstalk. Image from [2].

The far-end crosstalk components from capacitive and inductive coupling cancel, as they are opposite polarity. Inductive crosstalk dominates in cases where the traces are routed over slots in the return plane, as described in chapter 4.2. The near-end components have same polarity and get added together. [13,208-211.] Figure 23 illustrates the capacitively coupled crosstalk on both ends.

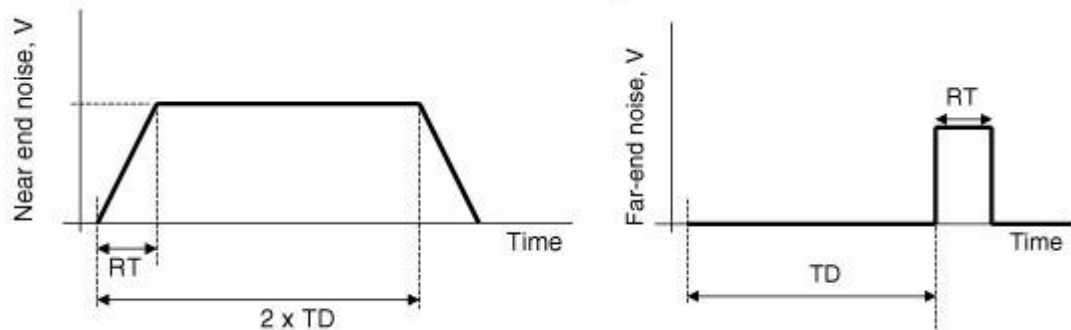


Figure 23. Capacitively coupled crosstalk on a single-ended microstrip. Image from [2].

When the crosstalk reaches one end of the victim line, reflections might occur, depending on the impedance the induced noise sees at the end. For example, near-end cross talk, upon reaching a low impedance driver of the victim line, will reflect with a reflection coefficient of close to -1. This means the wide pulse of near-end crosstalk is reflect with a reversed polarity. Source and load series termination strategies can be implemented to attenuate the reflections and eliminate ringing from these reflections. [13,205-207;2.] The crosstalk can be reduced by decreasing the mutual capacitance between the traces [2].

In summary, capacitive coupling couples noise from an aggressor to the victim line via distributed capacitance between the lines. The noise propagates to both ends on the victim line. The far-end noise accumulates as the signal edge propagates and is seen as a short pulse with the same polarity as the edge on the aggressor line. Often, when the traces are routed over a solid ground plane the far-end crosstalk is cancelled due to opposing polarities of inductive and

capacitive crosstalk. To reduce crosstalk, mutual capacitance can be decreased by increasing trace separation and bringing the ground plane closer to the trace.

5.2 Parasitic Capacitance in MOSFETs

Parasitic capacitances present in the transistor junctions influence the input characteristics of the MOSFET and set certain requirements for the gate driver circuit of a switching circuit. The various capacitances show nonlinear behaviour and are a function of voltage. Some manufacturers provide gate charge value in the component specifications to aid in designing gate drive circuits. The parasitic capacitances in MOSFETs are presented in Figure 24 below. [27,2-3.]

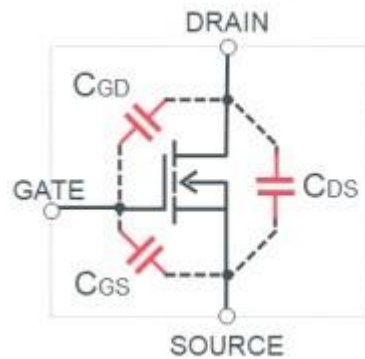


Figure 24. Parasitic capacitance in a MOSFET. Image from [27].

From the above capacitances, input capacitance (C_{iss}), feedback capacitance (C_{rss}), and output capacitance (C_{oss}) can be formed as shown below [9,197].

$$\begin{aligned}
 C_{iss} &= C_{GS} + C_{GD} \\
 C_{oss} &= C_{DS} + C_{GD} \\
 C_{rss} &= C_{GD}
 \end{aligned}
 \tag{20}$$

The current required by the input capacitance can be calculated using equation (10). C_{iss} requires a current proportional to the gate-to-source voltage. The current required by C_{rss} is proportional to the drain-to-gate voltage. In a common-source switch the capacitances are charged whenever the gate

voltage changes. This current is supplied by the gate driver. The combined effect of these capacitances is often given in the MOSFET datasheet as a plot of gate charge vs gate-to-source voltage. An example is shown in Figure 25 below. [9,197.]

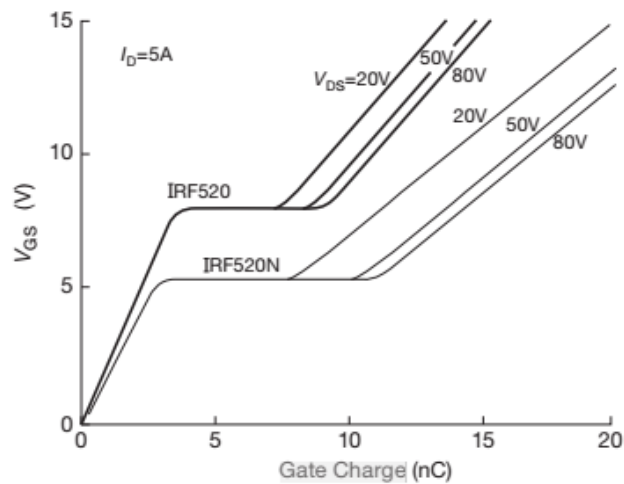


Figure 25. Gate charge vs gate-to-source voltage. Image from [9].

Three distinct regions can be observed in the above figure. The first slope region is charging the gate-source capacitance to increase the gate voltage. The second flat region occurs as the MOSFET is transitioning to the active region and the drain-source voltage decreases. It is known as the Miller plateau, during this region the gate voltage is constant, and the gate-drain capacitance is charged. During the last region drain-source voltage remains stable and gate voltage starts to increase. [9,197-198;27;28.]

The parasitic capacitances influence the switching characteristics of the MOSFET and the time to charge the input capacitances add to the switching losses [26]. As such, the designer should be aware of the parasitic components and how they influence the behaviour of the circuit.

6 Conclusion

This study investigated the parasitic components in PCB design. The goal was to provide an overview of the topic with examples of commonly faced issues arising from parasitic components. The various issues included increased losses, various forms of crosstalk, unwanted delay, and timing issues. Parasitic components were found to influence the transient response of circuits, particularly power distribution networks.

The findings provide an overview of the topic. However, no actual product or design was analysed for parasitic components. Future work could include designing a product, providing examples of how signal and power integrity issues are addressed in the design phase. This could further aid aspiring designers to understand the best practices for signal integrity.

In short, this overview on parasitic components in PCB design provided fundamentals on how to design electronics with signal integrity and power integrity in mind. These skills are increasingly important in digital electronics design due to decreasing rise times and increasing density of the designs.

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