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Design and Analysis of Planar Transmission Lines and Semiconductor Components for RF Switching Applications

Metropolia University of Applied Sciences

Bachelor of Engineering

Electronics

Bachelor's Thesis

28 May 2025

Abstract

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Title:	Design and Analysis of Planar Transmission Lines and Semiconductor Components for RF Switching Applications
Number of Pages:	28 pages + 5 appendices
Date:	28 May 2025
Degree:	Electronics
Degree Programme:	Bachelor of Engineering
Professional Major:	Electronics
Supervisors:	Heikki Valmu, Principal Lecturer

This thesis explores the characteristics of planar transmission (CPW) and semiconductor components. The objective is to evaluate their suitability for constructing a solid-state matrix switch aimed at high-throughput characterization of network elements using a two-port Vector Network Analyzer (VNA).

The operational bandwidth was specifically chosen to ensure that the transmission lines could be fabricated and verified using the available equipment in the electronics laboratory at Metropolia University of Applied Sciences. The simulated results were cross-checked with measurements from the fabricated PCBs to validate the accuracy and effectiveness of the design.

The experimental results confirm the feasibility of a 50-ohm semiconductor switch using P-HEMT GaAs FETs for microwave applications, due to their favorable high-frequency characteristics. However, optimal performance relies on proper impedance matching to minimize signal reflections. Discrepancies between simulated and measured data are attributed to uncertainties in the dielectric constant of the FR4 substrate, mechanical tolerances from PCB milling, and variability from manual soldering. These factors can cause impedance mismatches, increased insertion loss, and coupling effects. To improve performance, future designs should consider high-frequency substrates like Rogers RT/duroid 6002 and adopt assembly methods such as reflow soldering, which enhance consistency and reduce parasitics

Keywords: Solid state, matrix switch, transmission line, microstrip line, coplanar wave guide

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List of Abbreviations

AC: Alternating current.

AWR: Applied Wave Research. A suite of electronic design automation tools used for the design, simulation, and analysis of radiofrequency, microwave, and high-frequency circuits and systems.

DC: Direct current.

DUT: Device Under Test. The device is being tested to evaluate its performance.

FR-4: Flame Retardant 4. A substrate material made of woven fiberglass cloth with an epoxy resin binder that is flame resistant and used in the production of printed circuit boards.

HFSS: Ansys HFSS (high-frequency structure simulator) is a commercial finite element method solver for electromagnetic (EM) structures from Ansys.

MWO: Microwave Office.

PCB: Printed Circuit Board. A substrate plate on which electric components are connected to each other by metallized lines and patches.

RF: Radio Frequency. Frequencies spanning from 3 kHz to 300 GHz.

SMA: SubMiniature version A. A coaxial radio frequency connector.

TEM: Transverse electromagnetic wave propagation.

VNA: Vector Network Analyzer. Instrument used to measure reflection coefficients of electronic networks.

VSWR: Voltage Standing Wave Ratio. A measure of how efficiently radio-frequency power is transmitted from a power source into a load.

1 Introduction

This thesis explores the properties of planar transmission lines focusing on coplanar waveguides (CPW) and various semiconductor devices, including high-electron-mobility transistors (pHEMT). It combines background research with experimental work, probing the potential use case for the development of a solid-state switch matrix for radio frequency (RF) applications.

1.1 Background and Motivation

RF component characterization can be a heavy workload task with the increasing number of RF test components and connections. In addition, the varying testing conditions, such as temperature, humidity, or pressure often increases the overhead time and complicates the measurement cycles.

1.2 Objective of the Thesis

The main goal of this thesis is to look into how planar transmission lines are designed and tested, especially when used with semiconductor devices like RF switches. The work involves running simulations to check how well different lumped components perform and whether they are suitable for building a solid-state matrix switch with low signal loss. It also aims to make it easier to identify and understand how RF components behave by using transmission and reflection measurements in different setups.

1.3 Scope of the Thesis

This thesis starts with a basic overview of semiconductors and transmission lines to help readers, especially those new to the topic, get familiar with the subject and how it’s used. It doesn’t go deep into the complex math or physics behind how semiconductors are made or how transmission lines work. Instead, it focuses on general ideas within the field of RF. Some key equations are included to

highlight important points, but the main goal is to give a clear and simple understanding. The simulation methods explained are also designed to be easy to follow and repeat with the right equipment.

2 Semiconductor Theory

Semiconductors are materials that occupy an intermediate position between insulators and conductors. The former have very few mobile charges and, as a result, offer very high resistance to the flow of electrical current. The latter present very low electrical resistance due to their abundance of mobile charges. The resistance of semiconductors are in between the insulators and the conductors, which can further be tuned by various conditions. Semiconductors are usually insulators at very low temperatures and allow the flow of electrical current at room temperature. In addition. The conductivity of the semiconductors can be controlled by introducing atoms, different from those of the semiconductor into the material, these are called impurities.

When a semiconductor contains impurities, it is said to be doped. The most widely used semiconductor material in today's technology is silicon (Si), other semiconductors, such as gallium arsenide (GaAs) and compound semiconductors (like AlGaAs, InGaAsP, etc.), are also used in semiconductor devices.

2.1 Intrinsic Semiconductors

Intrinsic semiconductor, also called pure semiconductor, does not contain any significant dopant species. In other words it contains no foreign atoms and has a perfectly crystalline structure. An intrinsic semiconductor behaves as an insulator at very low temperature. The valence electrons are bound within covalent bonds, and the inner-shell electrons are tightly bound to the nucleus. When an electric field is applied, no current flows because there are no mobile charges, so the semiconductor acts as an insulator.

2.2 Extrinsic Semiconductors

An extrinsic semiconductor is a monocrystal that, in addition to the atoms of the base semiconductor, contains others known as impurities. These impurities are classified as donors and acceptors. Donor impurities give rise to an N-type extrinsic semiconductor, while acceptor impurities produce a P-type semiconductor.

2.3 N-type Semiconductor

In an N-type semiconductor, small amounts of pentavalent impurity atoms such as phosphorus are added to a pure semiconductor like silicon to enhance its electrical conductivity. These impurities, present in much lower concentrations than the host atoms, integrate into the crystal lattice by replacing some of the silicon atoms. Each impurity atom uses four of its five valence electrons to form covalent bonds with neighboring silicon atoms, just as silicon would. The fifth electron, however, remains free and contributes to electrical conduction. This doping process increases the number of free electrons in the material, making them the majority charge carriers, while holes remain as minority carriers.

2.4 P-type Semiconductor

A P-type semiconductor is formed when trivalent impurity atoms, such as boron, are introduced into a silicon crystal. These atoms have only three valence electrons, so when they replace a silicon atom in the lattice, they can form only three covalent bonds with neighboring silicon atoms, leaving one bond incomplete. This missing electron creates what’s known as a “hole,” which behaves like a positive charge carrier. The incomplete bond exerts an attractive force on nearby valence electrons, and if one of these electrons gains enough energy, it can move to fill the gap, completing the bond and negatively ionizing the impurity atom. However, this process does not generate a free conduction electron, as the electron remains bound to the impurity. Instead, the movement

of holes through the lattice becomes the primary method of electrical conduction in P-type semiconductors.

2.5 PN Junction Diode

Most diodes used in electronic circuits today are made from semiconductor materials and are built around a PN junction, which forms at the boundary between a P-type and an N-type semiconductor. In this junction, the P-type region contains an excess of positive charge carriers (holes), while the N-type region has an abundance of negative carriers (electrons). When a positive voltage is applied to the P-side relative to the N-side (forward bias), it allows a significant current to flow through the diode. In reverse bias, where the polarity is flipped, the current flow is minimal, almost zero unless the reverse voltage exceeds a specific value known as the breakdown voltage, causing the diode to conduct heavily in reverse. Real diodes differ from ideal ones in that they exhibit a small forward voltage drop (typically under 1 V for silicon diodes) and include effects like voltage-dependent capacitance. While the ideal diode model is often sufficient for basic applications, it becomes inadequate in high-speed circuits or when the diode operates near or within the breakdown region, where a more accurate representation of the diode's behavior is needed.

2.6 Bipolar Transistor

The bipolar junction transistor (BJT) is a three-terminal semiconductor device made up of two PN junctions arranged in either an NPN or PNP configuration. It was the first widely adopted three-terminal device in solid-state electronics and remains widely used in various applications, especially in digital and microwave circuits. The BJT operates by using a small input current at the base terminal to control a much larger current flowing between the collector and emitter terminals. This ability to amplify signals makes it valuable for both analog amplification and digital switching. Despite newer technologies, the BJT's design based on PN junctions provides reliable performance in many areas [2,355 – 373].

2.7 Field Effect Transistors

The field-effect transistor (FET) is a three-terminal semiconductor device that controls current flow using an electric field. Unlike the bipolar junction transistor, which relies on current flow through PN junctions, the FET operates by applying voltage to the gate terminal to control the conductivity of a channel between the source and drain terminals. This voltage changes the width of the conductive channel, allowing the FET to regulate a larger current with very little input current at the gate. FETs are widely used in digital and analog circuits due to their high input impedance and efficient switching capabilities.

2.7.1 MOSFET

MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) can be designed so that the current between the source and drain is carried by electrons in NMOS devices or by holes in PMOS devices. In complementary MOS technology (CMOS), both NMOS and PMOS transistors are used together, allowing for efficient operation. An NMOS transistor is typically built within a p-type well, which is formed by implanting or diffusing a p-type region into an n-type substrate. This p-well serves as the body or substrate for the NMOS device. To complete the transistor structure, highly doped n+ regions are implanted to form the source and drain terminals, enabling current flow controlled by the gate voltage [2,283-327].

2.7.2 GaAs FETs (Gallium Arsenide)

While silicon has traditionally been the dominant material for semiconductor devices, other materials such as gallium arsenide (GaAs), indium gallium arsenide (InGaAs), and various heterostructures like silicon/silicon-germanium (Si/SiGe) and gallium arsenide/aluminum gallium arsenide (GaAs/AlGaAs) have become increasingly important. Among these, pseudomorphic high electron mobility transistors (pHEMTs), which are based on GaAs and related heterostructures, have gained attention for their high-speed and high-frequency

performance. In recent years, gallium nitride (GaN) based devices have also emerged as particularly promising, offering new possibilities for advanced high-power and high-frequency applications [2,348.]

2.8 Parasitic Capacitance

Parasitic capacitance refers to the unintended capacitance that arises when two conductive elements are separated by an insulating material. This occurs naturally in electronic circuits due to the physical layout of components and connections. Although unintentional, parasitic capacitance can significantly affect circuit performance by causing unwanted coupling, especially at high frequencies. Understanding and minimizing parasitic capacitance is important in designing high frequency electronic devices.

3 Transistor Biasing

To use a transistor effectively as an amplifier or switch, it must be properly biased by applying a steady voltage and current. This sets its operating point within a specific region of its output characteristics, which describes how current and voltage relate. This direct current (DC) biasing ensures the transistor operates reliably in one of three regions: cut-off, saturation, or active, each determining its role in the circuit shown in Figure (1). In the cut-off region, the transistor behaves like an open circuit with almost no current flow and very high resistance. In saturation, it acts like a closed switch, allowing current to flow freely with very low resistance. Between these two, the active region enables the transistor to amplify signals by converting small input voltage changes into proportional output current changes, a property defined by its, transconductance. To achieve proper biasing and avoid distortion or unintended switching, it is important to consider the specific parameters provided in the transistor's datasheet, such as maximum voltages like gate to source (V_{GS}) , drain to source (V_{DS}) and drain current (I_D) , as these influence the correct operating point.

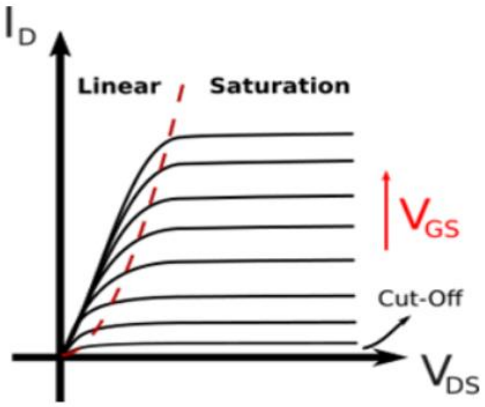

Figure 1: MOSFET characteristic output curve [3].

3.1 Reactance (X)

Reactance is a measure of opposition to the flow of alternating current (AC) caused by a capacitor or an inductor and is measured in ohms (Ω). Unlike resistance, reactance depends on the frequency of the signal, it is purely imaginary in phasor (complex) notation and does not dissipate power like resistance does.

3.2 RF Choke

RF coil or RF choke is a passive element designed to reject radio frequencies above certain limits while allowing lower frequencies f, including DC to pass through. Its inductance L can be calculated by the equation (1) considering the inductive reactance X_L ten times greater than the characteristic impedance Z_0 of the transmission line.

$$X_L = 2 \cdot \pi \cdot f \cdot L \,, \tag{1}$$

when $$X_L \geq Z_0 \cdot 10.$$

3.3 AC Coupling Capacitor

The AC coupling capacitor is a passive element designed to reject radio frequencies below certain limits including DC, while allowing higher frequencies f to pass though. Its capacitance C can be calculated by the equation (2) considering the capacitive reactance X_C ten times smaller than the characteristic impedance Z_0 of the transmission line.

$$X_C = \frac{1}{2\pi f l C}\,, \tag{2}$$

when $X_C \geq \frac{Z_O}{10}$.

4 Transmission Line

Not all high-frequency interconnects qualify as transmission lines. The concept of a transmission line is more about how the signal interacts electrically with the cable rather than being defined by the signal's frequency or the cable's physical attributes. In general, the impact of transmission line effects becomes important when the signal's wavelength is on the same order of magnitude as the interconnect's length. A common rule of thumb is that these effects start to matter when the line's length exceeds roughly one-quarter of the signal's wavelength.

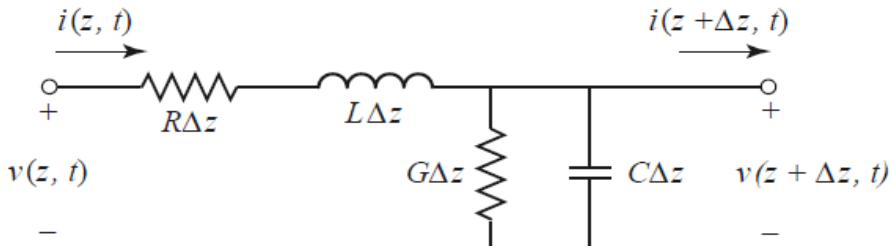

Figure 2: Circuit model on a transmission line per unit length. [1,49.]

The wavelength λ of a wave depends on the medium and the frequency. It is given by the equation (3).

$$\lambda = \frac{v}{f}, \tag{3}$$

where:

λ = wavelength (in meters)

v = velocity of the wave in the medium (in meters per second, m/s)

f = frequency of the wave (in hertz, Hz)

For electromagnetic waves traveling in a vacuum or in air, the velocity is approximately equal to the speed of light c,

$$v = c = 3 \times 10^8 \ \frac{m}{s}.$$

So the wavelength for electromagnetic waves in air or a vacuum would be described by the equation (4)

$$\lambda = \frac{c}{f}. \tag{4}$$

For waves in other materials, like a transmission line, the velocity v is reduced by the material's relative permittivity (dielectric constant) ε_r, and the speed of light in medium is.

$$v = \frac{c}{\sqrt{\varepsilon_r}}. \tag{5}$$

Thus, the wavelength λ in such a medium is given by,

$$\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_r}}. \tag{6}$$

4.1 Characteristic Impedance

The concept of characteristic impedance becomes relevant when a non-purely resistive load is connected to a network. This is where we begin to distinguish between a simple conductor and a transmission line. The former is intended to carry DC or low-frequency AC signals (up to a few kHz), where the signal's wavelength is much larger than the conductor length, and transmission line effects can be ignored. In contrast, a transmission line is designed to carry high-frequency AC signals, where signal reflections, impedance matching, and wave propagation effects become significant.

Modern microwave devices expect a characteristic impedance of 50 Ω described in the equation (7) as the ratio between inductance and capacitance.

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{7}$$

Ideally, the characteristic impedance of a transmission line (e.g. 50 Ω) remains constant along its length, as long as the geometry and materials (such as conductor dimensions, spacing, and dielectric constant) are uniform.

The losses in a transmission line are frequency dependent. At higher frequencies, conductor losses increase due to the skin effect, where the current is confined to a thinner layer near the conductor surface, effectively increasing resistance and, hence, the attenuation.

4.2 Voltage Standing Wave Ratio

Voltage Standing Wave Ratio (VSWR) is a measure used to determine the insertion and return losses of a transmission line. It is expressed by equation (8), where Gamma (Γ) is the reflection coefficient and is defined by the ratio in equation (9) between the forward travelling voltage amplitude (V^+) and the reflected backward travelling voltage amplitude (V^-). VSWR indicates how efficiently RF power is delivered from the source, along the transmission line,

and into the load. The value of VSWR is proportional to the return loss. A ratio of 1 represents the best transmission line efficiency (no reflections), while higher values than 1 indicate poor efficiency, and greater reflected power.

$$\mathrm{VSWR} = \frac{1+|\Gamma|}{1-|\Gamma|}. \tag{8}$$

$$\Gamma = \frac{V-}{V+}. \tag{9}$$

4.3 Planar Transmission Lines

A planar transmission line is a structure used to carry high-frequency signals across flat surfaces. It is made by placing conductive paths on or within layers of insulating materials. These lines guide electromagnetic waves (EM), often in transversal electromagnetic mode (TEM) or quasi-TEM mode. They are frequently used in systems involving microwaves, RF, or fast digital signals. Such lines are manufactured using printed circuit board or microfabrication techniques. The planar transmission line performance depends on its geometry and the properties of the materials used. [5,2.] where:

- L: Length of the center conductor
- W: Width of the center conductor
- T: Thickness of the metallization
- H: Thickness of the dielectric material
- a: Distance from the center conductor to the ground plane
- S: Gap between center conductor and ground planes.

4.3.1 Stripline

A stripline Figure (3), is a planar transmission line commonly used to carry high-frequency signals in RF and microwave circuits where maintaining signal

integrity is essential. It consists of a flat conductive trace placed between two parallel ground planes, all separated by a dielectric material. This symmetrical structure allows signal propagation in a transverse electromagnetic (TEM) mode and provides excellent shielding from external electromagnetic interference. Striplines are typically fabricated using multilayer printed circuit boards and are well-suited for densely packed designs that require controlled impedance. The characteristic impedance of a stripline is influenced by factors such as the width of the conductor and the dielectric constant of the insulating material. Thanks to their design, striplines offer low radiation losses and high isolation between nearby paths, making them ideal for precision, high-frequency applications.

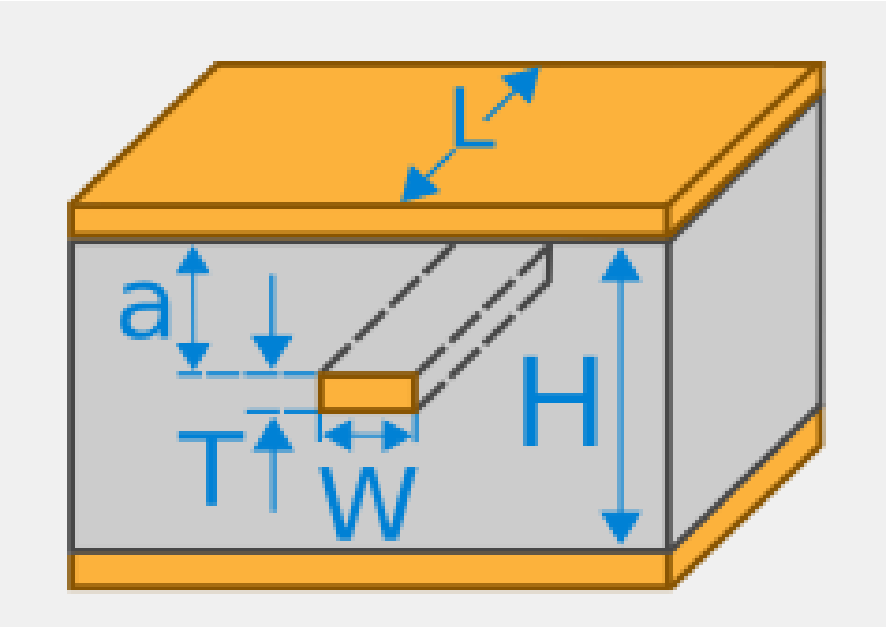

Figure 3: An illustration of a stripline [4].

4.3.2 Microstrip Line

A microstrip line Figure (4) is a type of planar transmission line commonly used in high-frequency circuits; It consists of a conducting strip placed on top of a dielectric substrate with a ground plane underneath. This structure is often visible on the outer layers of high-speed printed circuit boards. It supports quasi-TEM mode propagation suitable for RF microwave and even millimeter-wave applications.

Microstrip lines are widely used due to their ease of fabrication and compact

design. They allow for surface mounting of components and straightforward signal routing. The performance depends on the width of the strip, the substrate thickness and the dielectric constant. They are ideal for filters antennas, couplers, and impedance-controlled traces in modern communication systems, Microstrip lines are not fully shielded so they can be sensitive to external interference. Despite this they remain one of the most popular transmission line choices in PCB design. [1,147.]

4.3.3 Coplanar Waveguide

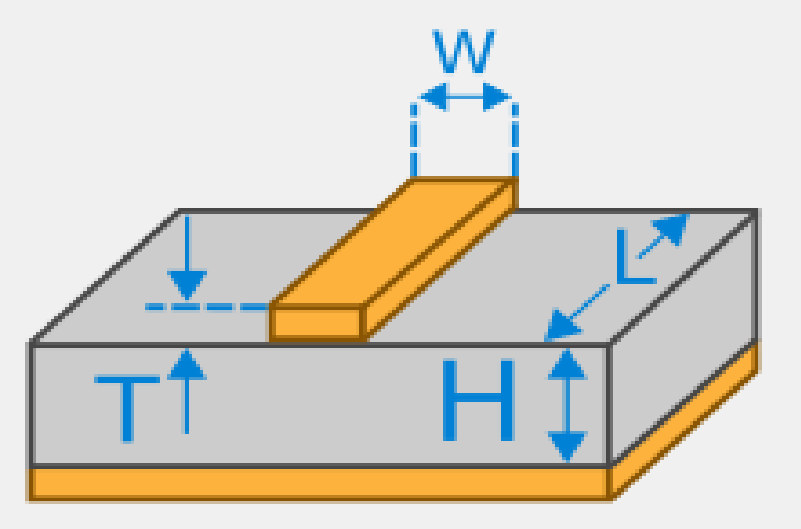

Figure 4: An illustration of a microstrip line [3].

A coplanar waveguide (CPW) Figure (5), is a type of planar transmission line used for high-frequency signal transmission, commonly found in RF and microwave circuit designs. It features a central conducting strip flanked by two ground conductors on the same layer, all positioned on top of a dielectric substrate, with no ground plane underneath. This structure supports quasi-TEM mode propagation and offers strong confinement of electromagnetic fields. One of the key advantages of CPWs is that they do not require vias to connect to ground, which simplifies layout and allows for continuous ground planes on the same layer. They are well-suited for surface-mount component integration and make transitions to other transmission line types straightforward. The impedance of a CPW depends on the capacitance, the inductance, the conductance, and the resistance per unit length which are defined by the geometry of the conductors and the dielectric medium around.

Coplanar waveguides are known for low radiation loss and efficient shunt component placement, additionally are widely used in filters, couplers, antenna feeds, and phase shifters. [5,1-4]

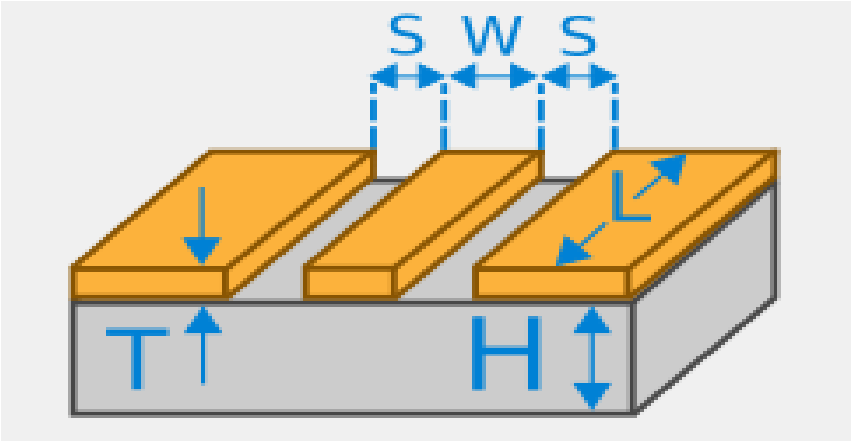

Figure 5: An illustration of a CPW [3].

4.4 De-Embedding

De-embedding is a technique applied after measurements are taken, aimed at reducing inaccuracies and revealing the true characteristics of the device being tested. When measurements include both the device under test (DUT) and associated fixtures, de-embedding can be used to isolate and remove the influence of the fixture, allowing the actual performance of the DUT to be observed. This method involves mathematically subtracting the fixture's impact from the overall measurement results, leaving only the response of the DUT. De-embedding is especially useful in setups where the connection from a vector network analyzer (VNA) to the DUT is not coaxial. It is commonly implemented in evaluating PCB traces, connectors, semiconductor packaging, backplane channels, and other discrete components [6].

5 RF Measurements

RF measurement is the process of analyzing high frequency signals to check their strength, frequency, and quality. RF signals are electromagnetic waves typically in the frequency range from about 3 kHz to 300 GHz.

5.1 Scattering parameters

Scattering parameters, or S-parameters, are a set of complex values used to characterize the behavior of RF and microwave networks. These parameters describe how signals are reflected and transmitted through a device with one or more ports, where each port can absorb, transmit, or reflect energy Figure(6). In essence, S-parameters express the relationship between incident and reflected waves at each port. For example, in a typical two-port network, the behavior is represented using a 2×2 matrix where each element corresponds to the ratio of reflected or transmitted power relative to an incident signal. These parameters provide information about both the magnitude and phase of signals. The representation of a Sxy parameter can take the form of cartesian graph power versus the frequency or in a smith chart.

The matrix (S_{11}) represents the scattering S-parameters for a 1-port device.

The matrix $\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$ represents the scattering S-parameters for a 2-port device:

- S11 = b1/a1 Reflected power seen from port 1.
- S12 = b1/a2 Transferred power from port 2 to 1.
- S22 = b2/a2 Reflected power seen from port 2.
- S21 = b2/a1 Transferred power from port 1 to 2.

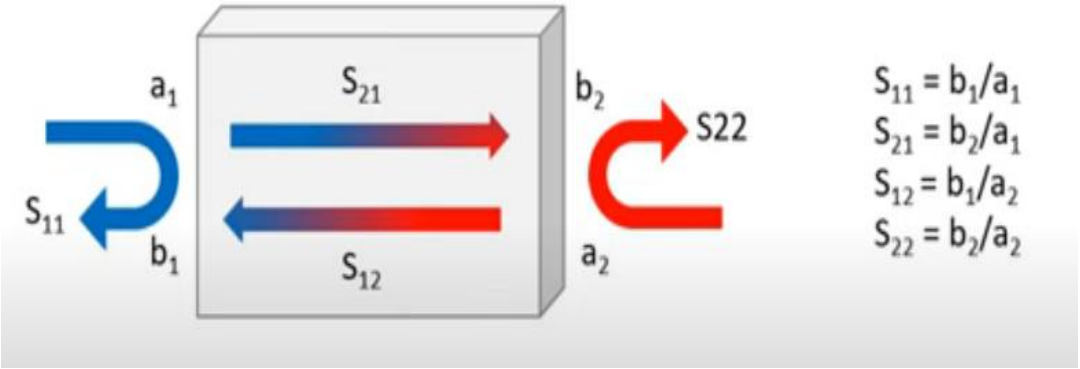

Figure 6: VNA and calibration kit Hewlett Packard 85033D 3.5mm.

5.2 Termination of Transmission Lines

Termination of a transmission line refers to how the end of the line is configured to manage signal behavior and minimize or control reflections. In most cases, proper termination involves matching the load impedance to the line's characteristic impedance to ensure that signals are absorbed rather than reflected, which helps maintain signal integrity. Mismatched terminations can cause reflections that interfere with the original signal, leading to distortion or loss of data, especially in high-frequency or high-speed digital circuits. However, in certain RF or testing applications, deliberately using an open or short termination can be beneficial for example, in measuring reflection coefficients, tuning circuits, or creating specific impedance conditions. Termination methods include resistive matching (series or parallel), as well as controlled open or short circuits depending on the design objective. Choosing the right termination strategy is essential for achieving reliable performance in communication systems, transmission lines, and high-speed electronic designs.

The reflection coefficient Γ is calculated by the equation (10)

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}. \quad (10)$$

where Z_L is the load impedance and Z_0 is the characteristic impedance of the line. When the load is a short circuit (Z_L = 0), the reflection coefficient is Γ = −1, indicating total reflection with phase inversion. For an open circuit (Z_L = ∞), Γ = +1, showing total reflection without phase inversion. If the load matches the line impedance (Z_L = Z_0), Γ = 0, meaning no reflections occur.

5.2.1 Short Termination

A short termination in a transmission line happens when the end of the line is directly connected to ground or a conductor, creating a zero-impedance point. This means the voltage at the termination is forced to be zero while the current can be very high. When a signal traveling down the line reaches this shorted end, it is fully reflected back toward the source, but with the voltage wave inverted in phase while the current wave remains in phase. The complete reflection leads to the formation of standing waves along the line, which can cause signal distortion or power loss if not managed properly. Short terminations are often used deliberately in test setups or specific circuit designs, but in general, designers try to avoid them in signal lines to maintain proper impedance matching. Proper termination helps reduce reflections and ensures efficient power transfer.

5.2.2 Open Termination

An open termination in a transmission line occurs when the end of the line is left disconnected, meaning no load is attached and no current can flow. This creates a condition of effectively infinite impedance at the termination point. As a result, when a signal reaches the open end, it cannot be absorbed and is entirely reflected back toward the source. The reflected voltage wave maintains the same voltage amplitude and phase as the incident wave, while the current component is inverted. This reflection can cause standing waves along the line, which may lead to signal distortion, inefficiency, or power loss in high-frequency

systems. Open terminations are generally avoided unless intentionally used for specific purposes such as tuning or signal sensing.

5.2.3 Matched Termination

A matched termination in a transmission line occurs when the load impedance at the end of the line exactly equals the characteristic impedance of the line. This perfect match ensures that the signal traveling along the line is completely absorbed by the load with no reflections returning toward the source. As a result, the voltage and current waves continue smoothly into the load, preventing the formation of standing waves. Matched networks are essential for maximizing power transfer at high-frequency and high-speed circuits [8, 3-5].

5.3 Measurement Setup Calibration

VNA calibration Figure (7), is typically performed on a setup to de-embed the contributions from the measurement cables into the measurement of the device under test (DUT). The calibration is done by terminating the measurement cables

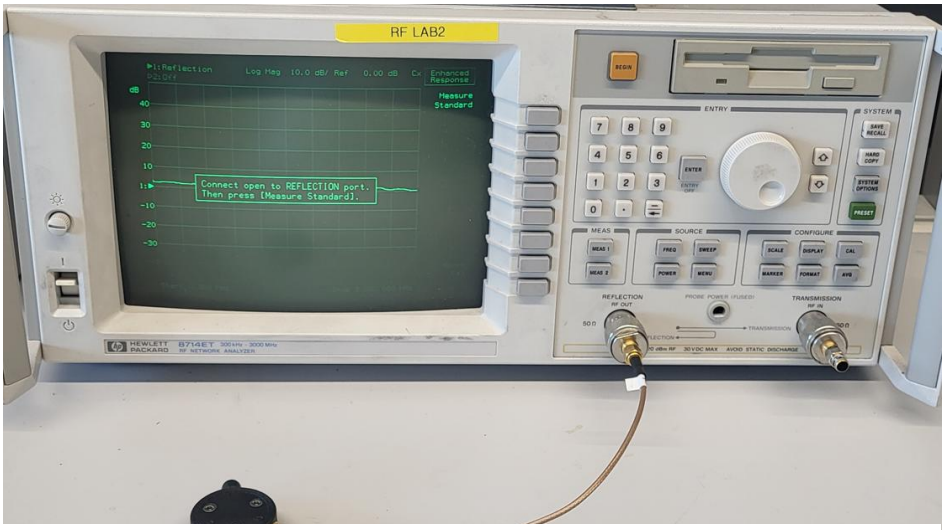

Figure 7: VNA and calibration kit Hewlett Packard 85033D 3.5mm.

with Short open load terminations and measuring a through transmission on the cables.

6 Switch Design and Simulations

This chapter covers the design, simulation, and fabrication of a coplanar waveguide (CPW), followed by the assembly semiconductor device. It also details the testing procedures conducted over a frequency range from 300 kHz to 3 GHz, emphasizing the evaluation of the device's performance within this spectrum. The CPW dimensions were calculated using the KiCad calculator, with the parameters provided in Appendix 1.

The Figure (8) shows the Applied Wave Research / Microwave office (AWR/MWO) simulation results of a 50 ohms coplanar transmission line (CPW) on a flame retardant 4 substrate (FR4), which has a relative permittivity ($\mathcal{E}$) of 4.2 and a loss tangent of 0,01. The reflection coefficients are displayed on a Smith chart, while both transmission and reflection magnitudes are plotted on a rectangular graph over the frequency range from 300 kHz to 6 GHz. The results of this simulation demonstrate excellent performance, with transmission remaining nearly flat around 0 dB and reflections consistently below -20 dB.

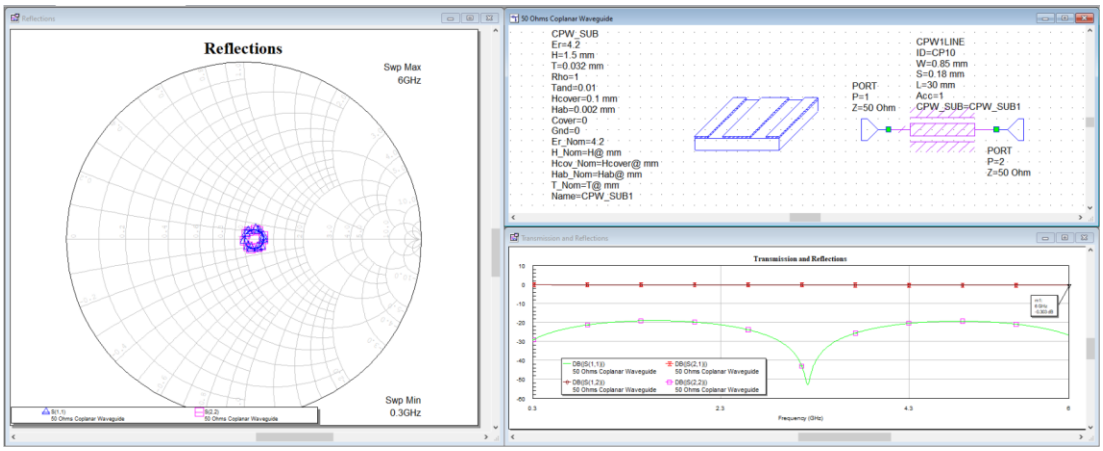

Figure 8:AWR simulation results of CPW.

Before manufacturing and assembling the CPW, a geometric simulation was performed using the finite element solver HFSS Figure (9), assigning finite dimensions to the ground planes to better represent real conditions. This simulation was used to validate the results obtained from AWR, and the

outcomes confirmed that the performance remained consistent across the frequency range.

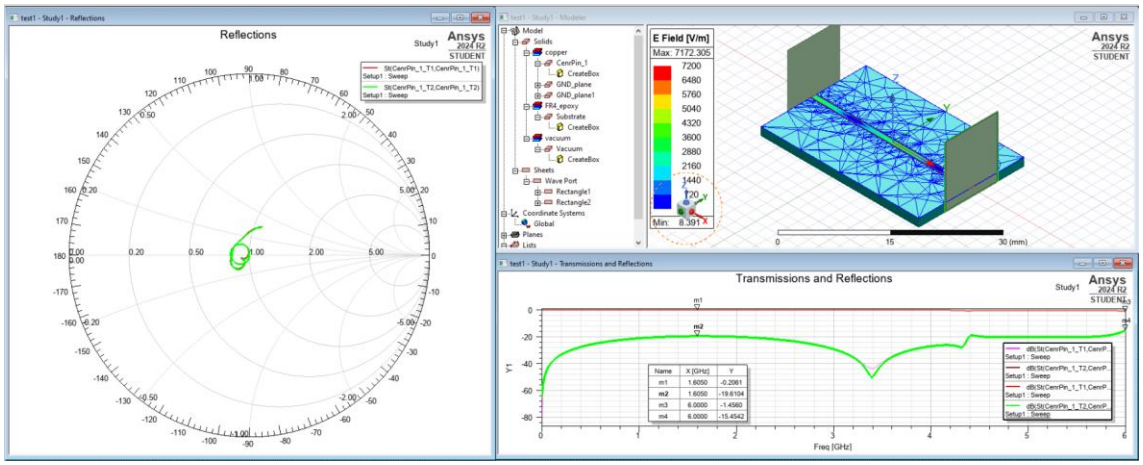

Figure 9:ASYS HFSS simulation results of the CPW.

The CPW Figure (10), with the dimensions identified in the EM simulations, was manufactured on an FR4 substrate. Additionally, the semiconductor circuit was machined on the same piece of substrate, ensuring that both structures share the same permittivity. This allows the CPW to serve as a reliable baseline for future measurements or for de-embedding purposes.

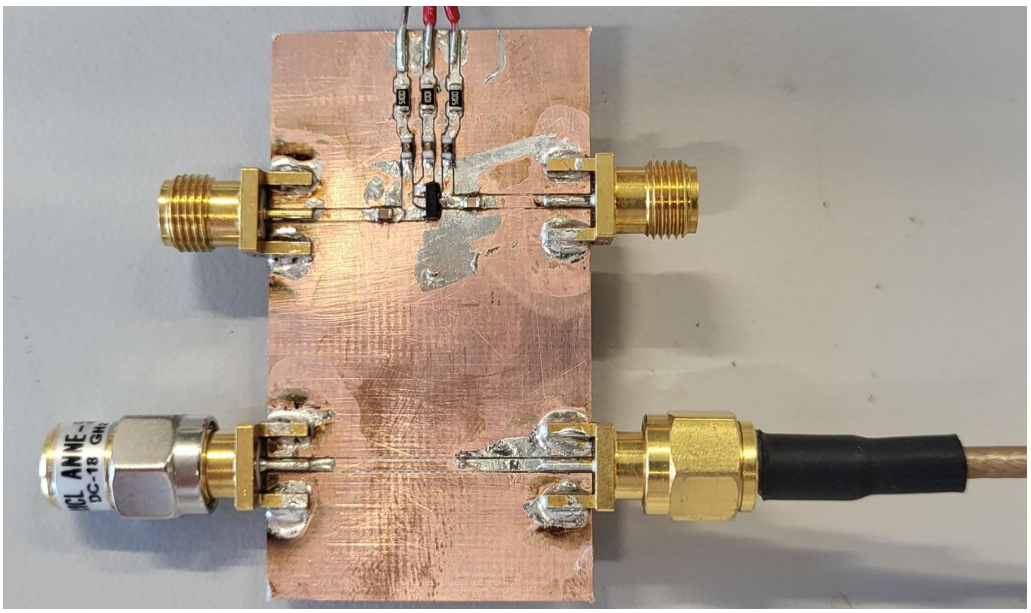

Figure 10: CPW manufactured in FR4 subtrate.

The measurements confirmed the simulated results, validating the accuracy of the design and simulation process shown in the Smith chart, Figure (11).

Figure 11: S11 parameters plot of the CPW frequency response.

6.1 CPW Coupling

To determine the transmission background of the two coupled transmission lines, a new simulation shown in Figure (12), was performed using AWR/MWO, in this simulation the S-parameters of both 68pF AC coupling capacitors were imported. These capacitors acting as high pass filters were calculated using the equation (2) for a cut-off frequency of 468.1 MHz. The frequency response of the coupled CPWs was simulated, incorporating the S-parameters of the AC coupling capacitors (package 0603, part number 251R14S680JV4T) from Johanson Technology. The results show a degradation in transmission performance, with signal reflections exceeding 1% at several points within the frequency range, corresponding to reflection levels between -20 dB and -10 dB.

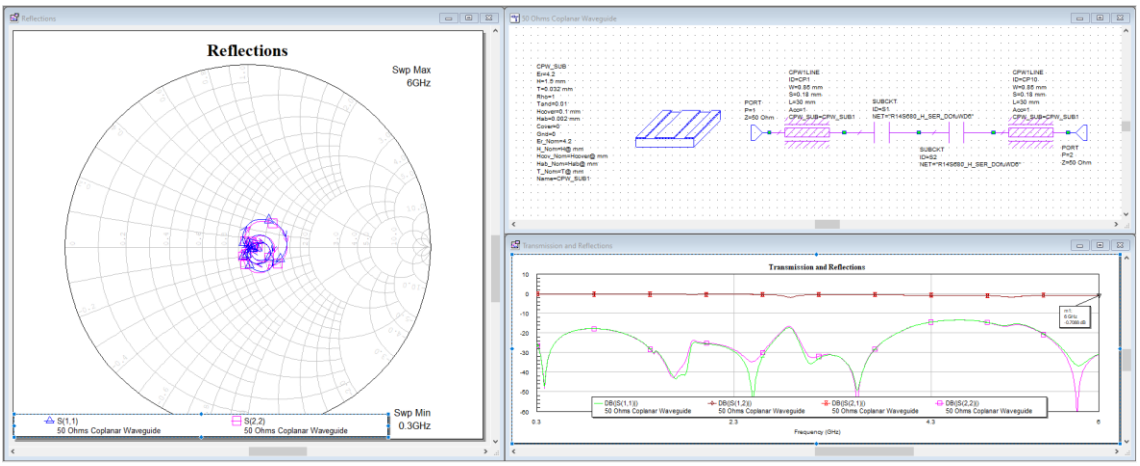

Figure 12: Transmission background simulation of two coupled CPW.

6.2 Semiconductor Parasitic Capacitance Simulation

Once the transmission background was determined, a parasitic capacitance model for the MOSFET transistor PJA3432-AU (package TO-23) was derived from its datasheet and incorporated into the simulation in between both AC coupling capacitors. The lumped transistor model shown in Figure (13) includes a 13 pF corresponding to the drain-to-source capacitance, 2 nH inductance, and 0.2 ohms resistance. The simulation results reveal that the frequency response and show that this capacitance value is relatively high for an RF switch application within the simulated range, and due to the low capacitive reactance at high frequencies, the transistor would be unable to effectively block the signal between the drain and source terminals. Additionally, a characteristic impedance mismatch is already visible in the Smith chart, further impacting the transmission performance. The simulation results were validated through experimental measurements, which showed high transmission near to 0dB across the frequency range from 300 kHz to 3 GHz shown in Figure (14), clearly demonstrating the parasitic behavior of this semiconductor device at high frequencies. The biasing circuit and PCB design can be seen in Appendix 2. Acting a low pass filter the RF chokes of 180nH were calculated for a cut-off frequency of 442.1MHz using the equation (1).

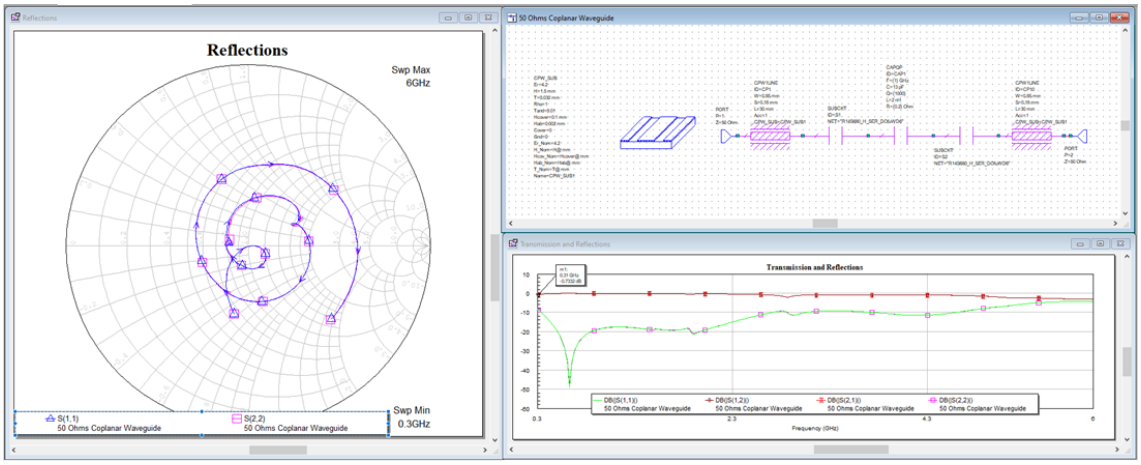

Figure 13: Simulation of the coupled CPW by the transistor model.

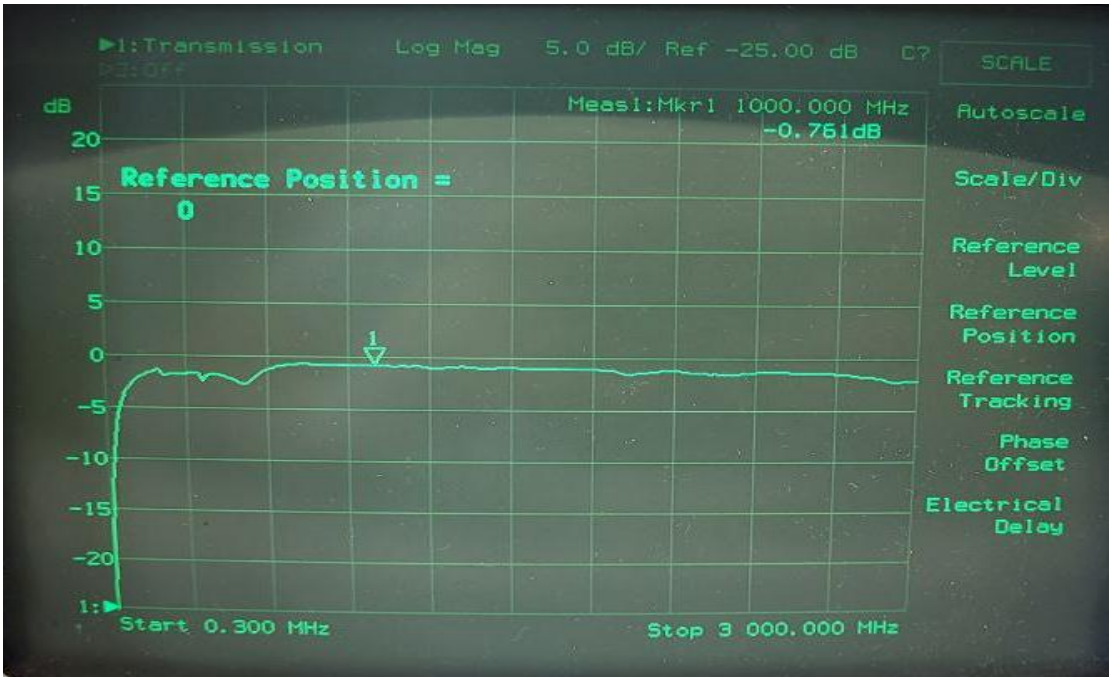

Figure 14: Rectangular plot of S21 parameter of the transistor PJA3432-AU; 10dB/div power 0dBm.

The observed parasitic behavior of the MOSFET is consistent with its small-signal model shown in Figure (15), where the cut-off frequency (f_t) can be estimated using the equation (11) [3,348], in which C'_{par} represents the total input parasitic capacitance [9, 347]

$$F_T = \frac{gm}{2 \cdot \pi \cdot (Z \cdot L \cdot C_{OX} + C'_{par})} \quad (11)$$

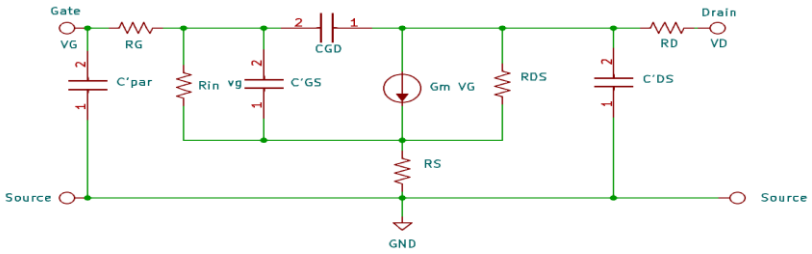

Figure 15: Small-signal model of the MOSFET transistor.

6.3 P-HEMT Based Switch

Based on the findings discussed in Section 6.2, a transistor with low parasitic capacitance was selected to reduce the unwanted coupling between the drain and source caused by parasitic effects. The CE3520K3 pHEMT was chosen for its favorable high-frequency performance. The biasing circuit, detailed in Appendix 3, was designed using the set of equations provided in Appendix 4. Although this configuration marked a clear improvement over the results in Section 6.2, it was not fully optimized, and no impedance matching network was incorporated in this initial design. The transmission coefficient (S21) in the ON state, illustrated in Figure (16), remained close to 0 dB across the 300 kHz to 3 GHz range, indicating effective signal conduction. In contrast, the OFF-state behavior, shown in Figure (17), revealed frequency-dependent signal leakage. A marker on the plot highlights a transmission level of −10 dB at 1.494 GHz, suggesting that while performance has improved, further design refinement is needed to enhance isolation and overall switching behavior at higher frequencies.

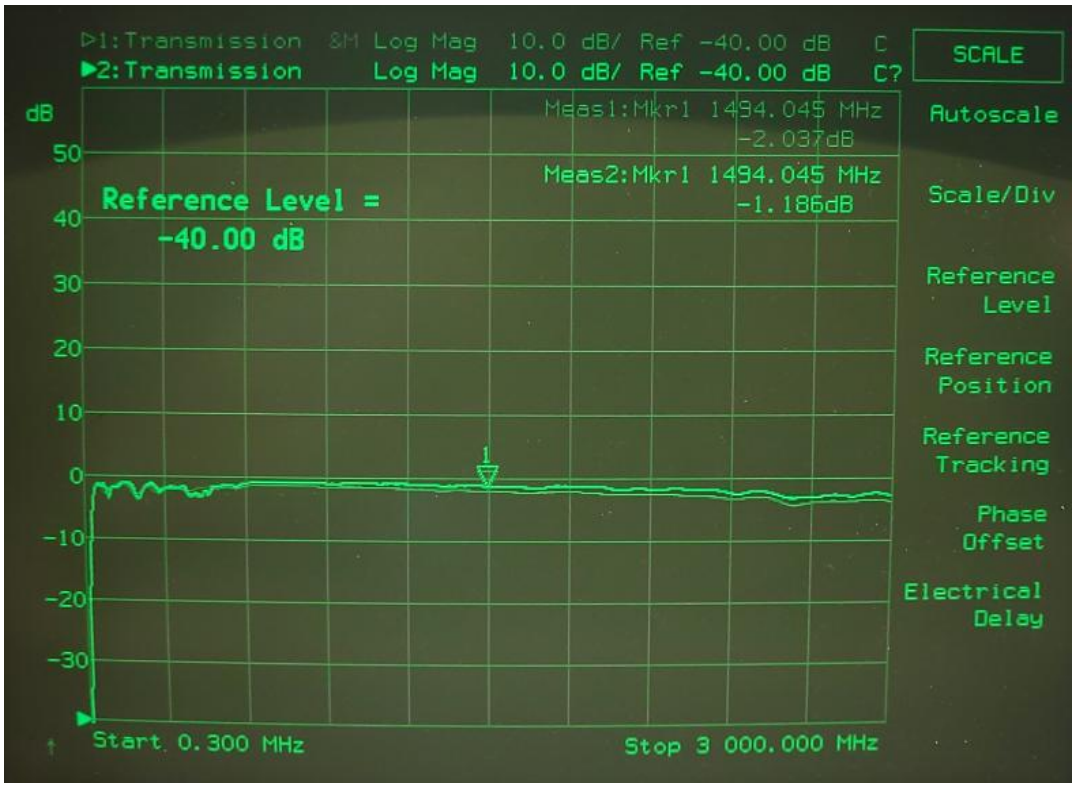

Figure 16: S21 plot of the transmission of the transistor CE3520K3 in mode ON.

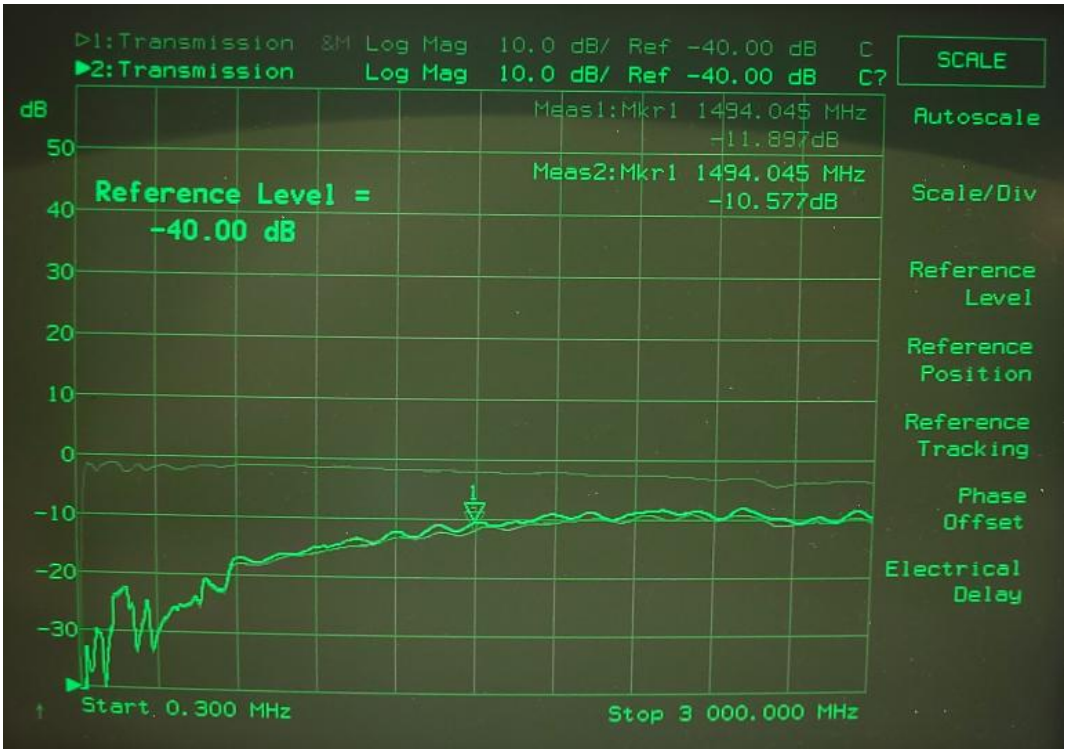

Figure 17: S21 plot of the transmission of the transistor CE3520K3 in mode OFF.

6.4 GaAs SP2T Switch

Following the initial evaluations of various passive and active components particularly the impact of parasitic capacitance on transmission performance, a series of simulations and measurements were conducted to assess transistor behavior under RF conditions. These studies revealed the limitations of certain semiconductor devices, especially in terms of unwanted drain-source coupling and insufficient isolation in the OFF state. To address these issues and evaluate a more suitable RF switching solution, the SKY13298-360LF GaAs SP2T switch was selected for testing. Biasing circuit and PCB design shown in Appendix 4.

This device, designed for ultra-wideband (UWB) applications from 3 GHz to 8 GHz, was examined in a narrower frequency range from 1 GHz to 3 GHz. The measured S-parameters demonstrated a stable insertion loss of approximately −5.8 dB across this band in the ON state shown in Figure (18), indicating consistent transmission behavior.

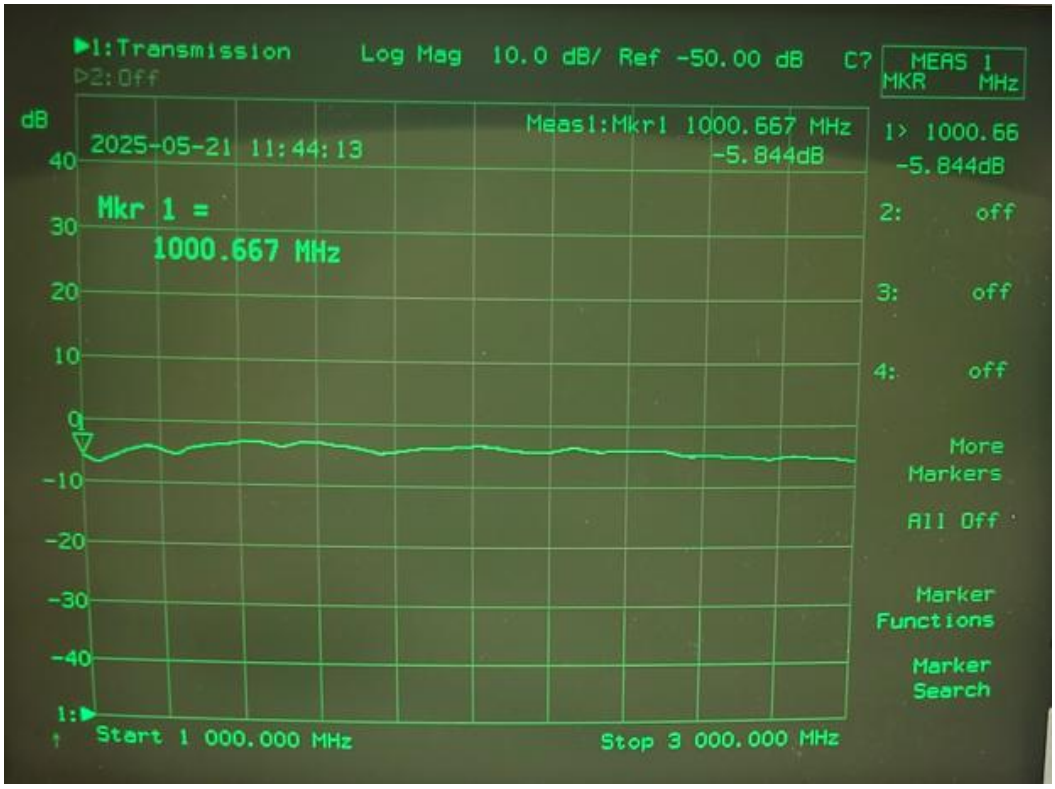

Figure 18: S21 parameter of the switch in mode ON.

In the OFF state, the switch exhibited effective isolation between the RF common port and output port J1, with reflection values remaining below −20 dB shown in the Figure (19), confirming its capability to suppress signal leakage in this configuration. These results highlight the improved performance of GaAs-based RF switches for broadband applications compared to earlier discrete transistor configurations.

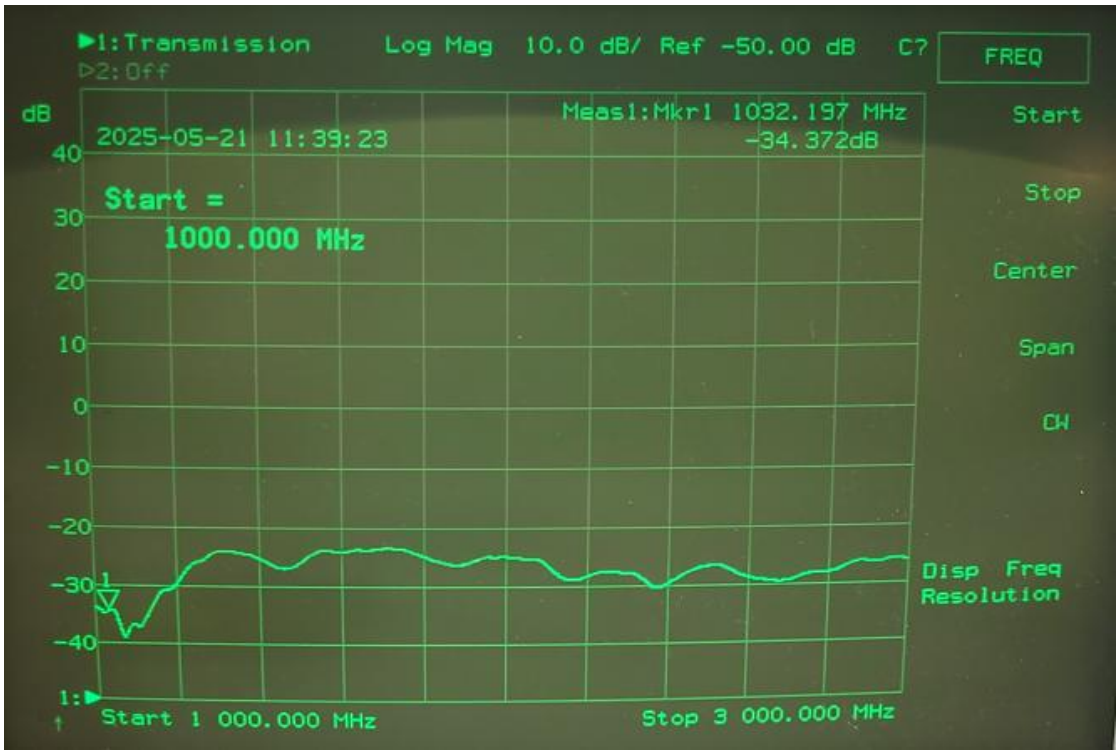

Figure 19: S21 parameter on the GaAs switch in mode OFF.

7 Conclusions

The experimental results confirm that the design and fabrication of a 50 ohm semiconductor switch operating at microwave frequencies is feasible within a defined frequency range, particularly when using P-HEMT GaAs FET technology. These types of transistors offer favorable high-frequency characteristics that make them suitable for RF switching applications. However, achieving optimal performance also requires careful attention to impedance

matching. Without proper matching networks, signal reflections can significantly degrade the transmission line’s efficiency and overall system behavior.

Observed discrepancies between simulated and measured data are likely attributed to several practical limitations. One notable factor is the uncertainty in the dielectric constant (ε) of the FR4 substrate, which may deviate from nominal values across frequency, impacting impedance and phase behavior. Mechanical tolerances from the PCB milling process and variability introduced during manual soldering further contribute to performance variation. Such issues can lead to impedance mismatches, increased insertion loss, and unexpected coupling effects.

Future improvements in performance could be achieved by adopting more precise fabrication and assembly methods. Using a high-frequency substrate such as Rogers RT/duroid 6002 would reduce material-related variability and enhance signal integrity. Moreover, implementing reflow soldering instead of manual soldering would help ensure consistent solder joints, minimize parasitic artifacts, and improve component alignment. These refinements would collectively support higher repeatability and better RF performance in future iterations of the switch design.

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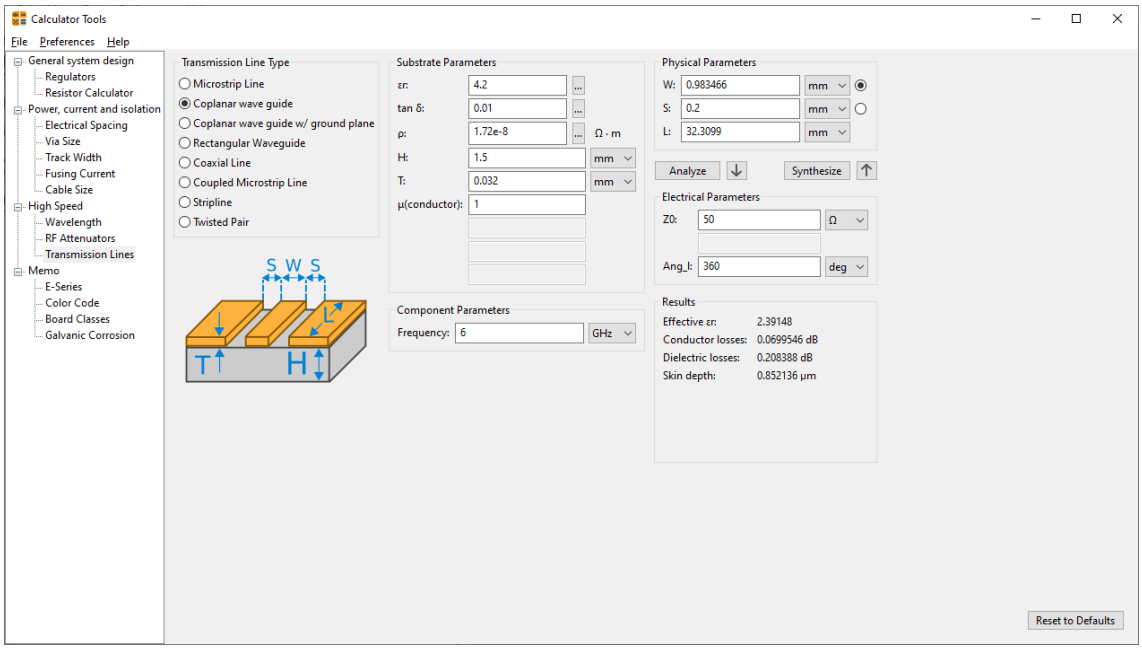

Figure 16: KiCad Calculator for CPW.

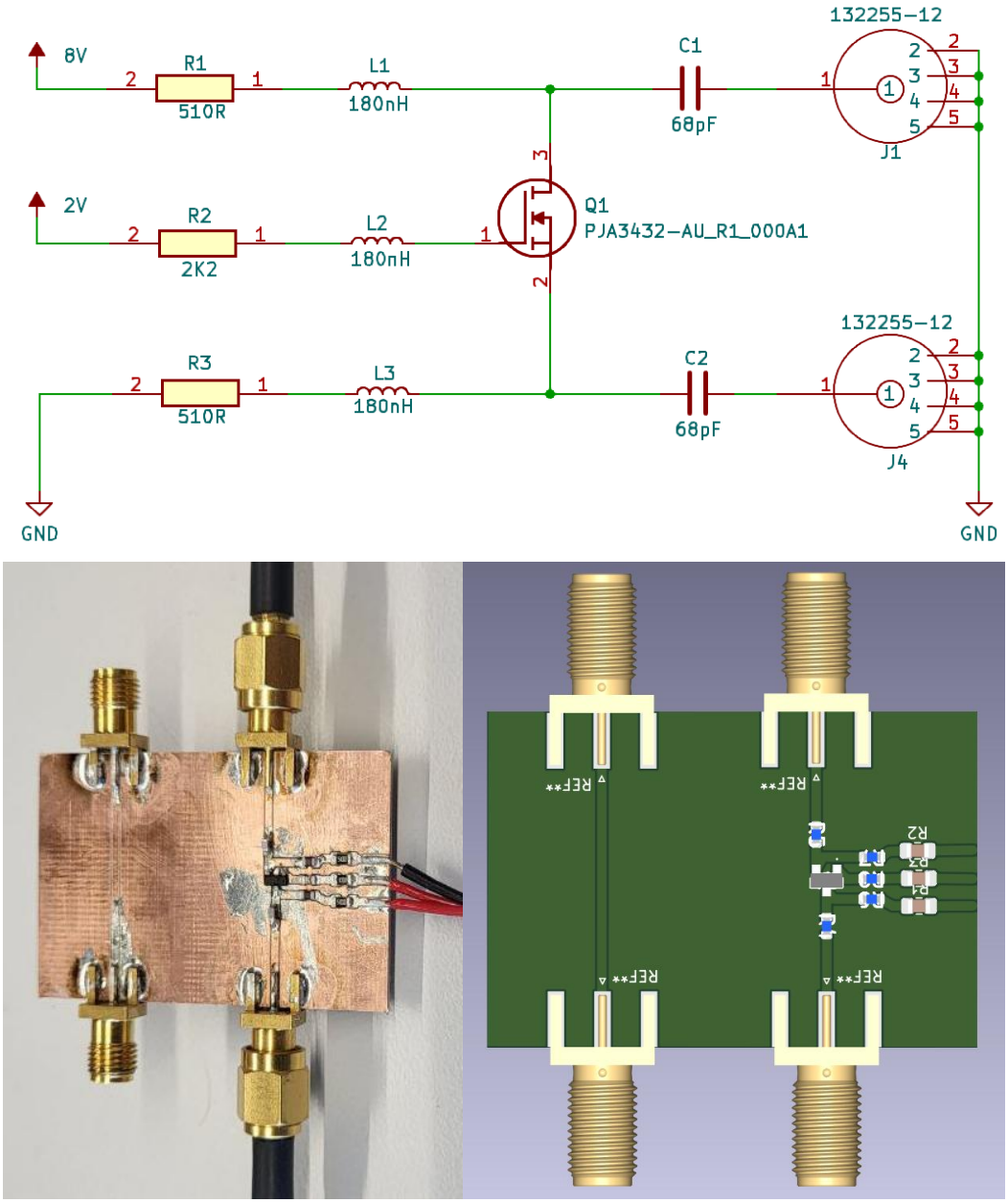

Figure 17: Biasing circuit and PCB design for the MOSFET transistor PJA3432-AU package TO-23.

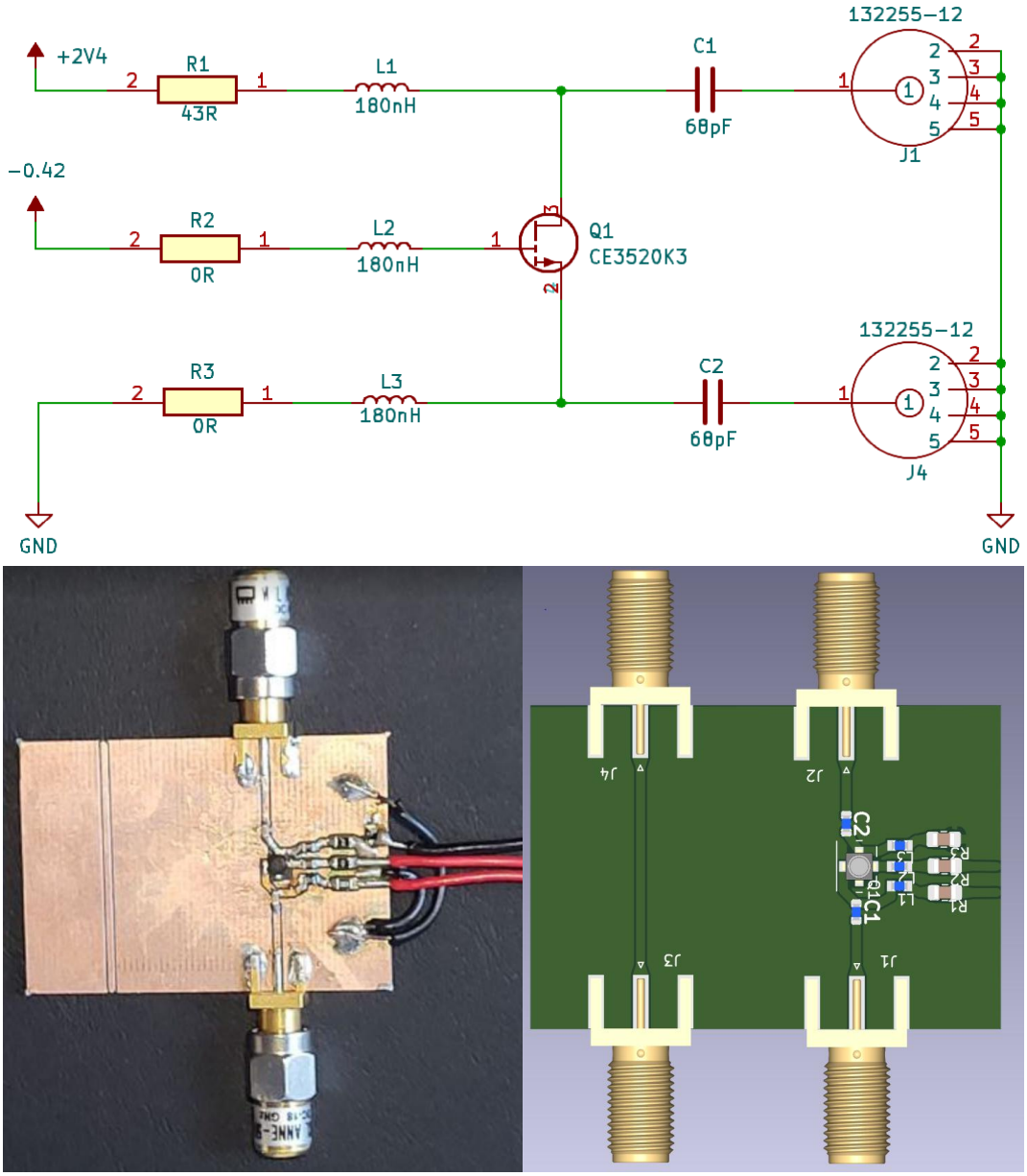

Figure 18: Super Low Noise FET biasing circuit and PCB design.

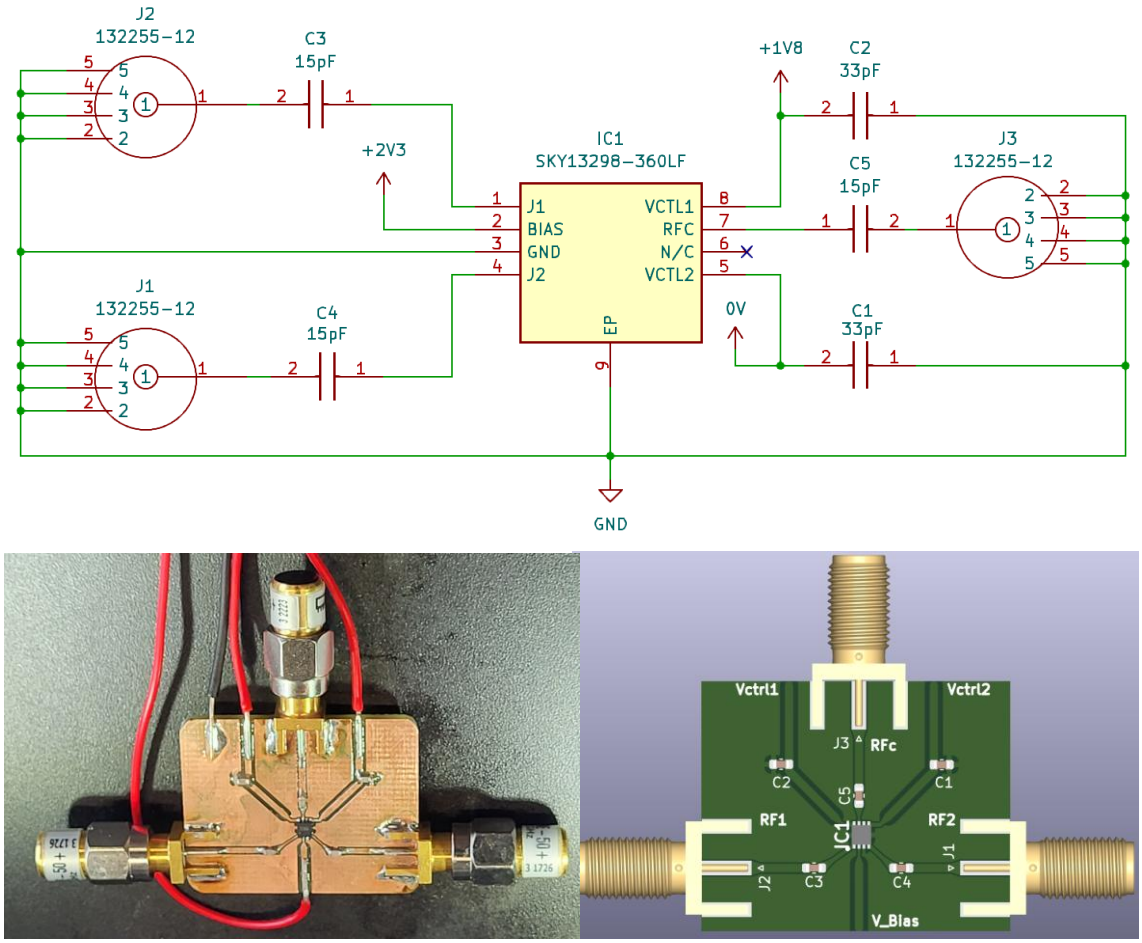

Figure 19: Circuit biasing and PCB design for GaAs SP2T Switch.

FET transistor biasing

$$V_i = V_{GS} \quad (12)$$

$$V_{DD} = I_D \cdot R_d + V_{DS} \quad (13)$$

$$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 \quad (14)$$

$$V_{GS} = V_{GS}\left(\text{off} \cdot \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)\right) \quad (15)$$

When VGS = -1V and IDSS = 30mA

$$V_{GS} = -1 \cdot \left(1 - \sqrt{\frac{10}{30}}\right) = \text{-}0{,}423\text{V} \quad (16)$$

If VG = 0V VDD = 2V and ID 10mA

$$VS = +0{,}423\text{V} \quad (17)$$

$$R_S = \frac{V_S}{I_D} = 42[\Omega] \quad (18)$$

$$V_{DD} = V_{DS} + V_S = 2{,}42\text{V} \quad (19)$$

Cutoff

$$VGS < VGS(\text{off}) \quad (20)$$

$$VG = VS + (\text{-}1) = \text{-}0{,}58\text{V} \quad (21)$$