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# Designing an Analogue Output for a Frequency Converter Control Board

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Insinöörityö tehtiin Asea Brown Boverille Helsingin Pitäjänmäen elektroniikkatehtaalla. Työssä parannettiin erään pienitehoisen taajuusmuuttajan ohjauskortin analogialähtö-ratkaisun linearisuutta ja tarkkuutta. Tarkkuustavoite asetettiin +/-1 %:iin edelliselle ratkaisulle määritellystä +/-3 %:sta. Uusien ratkaisujen suunnittelurajoiksi asetettiin hinta, fyysinen piirilevykoko sekä komponenttien saatavuus. Lisäksi ratkaisuun piti sisällyttää galvaaninen erotuspiiri.

Uusia ratkaisuja varten vanhaa piiriä tutkittiin soveltaen teoriaa, käyttäen simulaatio-ohjelmaa ja laboratoriokokeita. Kerätyn tiedon perusteella optoeristinaste, komparaattori-aste ja pääteaste todettiin vanhan ratkaisun vikalähteiksi. Tunnistettujen vikojen perusteella suunniteltiin kolme ratkaisua, joista valmistettiin prototyyppilevy.

Ratkaisuista mitattiin viiden levyn otannalla ulostulovirtavirhe sekä arvioitiin lineaarisuus. Lisäksi kaksi ratkaisua testattiin äärilämpötiloissa käyttäen olosuhdekaappia. Kahden ratkaisun tilastollista tarkkuutta tutkittiin kahden ulkopuolisen mittaajan avustuksella. He mittasivat ulostulovirtavirheen kolmen levyn otannalla.

Kaikki ratkaisut saavuttivat niille asetetun tarkkuustavoitteen +/-1 %, mutta yhden piirin tarkkuus jäi 1,1 %:iin. Lämpötilamittauksessa yksi ratkaisuista todettiin lievästi epä-vakaaksi korkeissa lämpötilaolosuhteissa.

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| Avainsanat | analogialähtö, lineaarisuus, ohjauskortti, tarkkuus |

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This bachelor's thesis was carried out at ABB electronics factory in Pitäjänmäki, Helsinki. The main objectives were to find cost efficient solutions which would improve the linearity and accuracy of the previous analogue output circuitry design in the old generation frequency converter control board. The target was set to increase the accuracy from +/-3% to +/-1%. The design parameters set for the solutions were cost efficiency, circuit board footprint, ease of sourcing and also a critical galvanic isolation stage.

The original design was studied by using theory, simulation and laboratory experiments. The isolation, comparator and output stages were identified as the main causes of error. Therefore three corrective solutions were designed and implemented on a printed circuit board. Five boards were tested for linearity and output current error. In addition, the performance of two solutions was tested in a climate device. Additional statistical data was collected from two solutions by two unaligned measuring operators which tested three boards.

Each solution achieved the target accuracy of 1% with an exception of one circuit which reached 1,1% in the designer performed initial measurement. In the additional unaligned operator measurement the statistical accuracy slightly decreased. One of the solutions was found moderately unstable at high temperatures in the thermal experiment.



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| Keywords | Analogue output, linearity, control board, accuracy |

## Preface

I wish to thank my thesis instructor Mr. Thierry Baills from Metropolia University of Applied Sciences for his guidance and support throughout this final academic endeavour. I would also like to give thanks to my supervisors at ABB Drives Helsinki, Mr Jari Mäkilä and Mr Vesa Mäkelä, for their support and insight.

I wish to express my gratitude to my family, friends and all those people who have been there for me when I most needed them.

I would also like to give a special thanks to fellow engineering students at ABB, Mr Ville Kärjä and Mr Hannes Aalto, for providing me assistance in obtaining the data used for the statistical performance analysis of the prototype on their own spare time.

Not long ago my good friend said to me: *"I would have never believed you would become a bachelor of engineering!"* a funny thing is that, neither did I. In the beginning there was only music, an electric guitar and a need for a tube amplifier. Then the curiosity came.

Espoo, May 31st, 2011

Mika Kontto

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List of Abbreviations and Meanings

AC-voltage

An alternating current voltage: a voltage of which value changes in time. Most commonly referred to sinusoidal waveform voltage of which a good example is the power grid voltage 230V/50Hz (Finland).

Analogue

An analogue signal is a time continuous typically voltage or current signal.

Amplitude

Amplitude is the maximum value of a periodical signal or a pulse.

Comparator

Comparator is a device which compares voltages in its input pins to each other and gives an output voltage of high or low state depending on the comparison result.

DC-Voltage

Direct current voltage: a voltage of which caused current flow in a conductor does not change direction.

Digital

Digital technology is a way to represent data via discrete values in electronics. The individual truth values also known as bits are 1 and 0. The bits can be formed into several bit long words to represent larger data.

Digital I/O

Digital input or output, depending on in or out state either sends or reads digital information in the form of individual bits.

Drive

An electrical drive is a device which is able to control the behaviour of an AC-motor.

Inverter

An inverter is a device which changes DC-voltage to AC-voltage.

HVAC-system

An abbreviation of Heating Ventilation Air Conditioning

Mod-Bus

The Modbus protocol, an embedded field bus communications protocol introduced by Modicon incorporated.

MOSFET

Metal Oxide Semiconductor Field Effect Transistor. MOSFET is channel transistor device of which operation is voltage controlled.

Operational Amplifier

Operational Amplifier is a high gain amplification device which is built from many transistors.

Optocoupler

An optocoupler is an isolation device, which transforms electric signal to light during the isolation between its input and output.

PWD

Pulse width distortion, an alteration inflicted to pulse width of a signal after a non-linear transfer.

PWM

Pulse width modulation, a technique to control the pulse duration of a square wave signal.

Rail-to-Rail (operational amplifier)

A device which can amplify signal voltage value up to its power supply rails.

# 1 Introduction

## 1.1 Company Introduction

### 1.1.1 ABB Business and Fields of Operation

Asea Brown Boveri, also known as ABB, is the globally leading company in the field of power electronics and automation. ABB provides power electronics solutions, products and services for a broad spectrum of customers ranging from individual consumer via military and industry to infrastructure. ABB has operations in around 100 countries. [1]

The company business is divided to five main divisions: Power Products, Power Systems, Discrete Automation and Motion, Low Voltage Products and Process Automation. [1]

The Power Products division provides components for power electronics applications in both medium and high electric power application area. The Power Products division manufactures power infrastructure related products such as transformers, cables and circuit breakers. [1]

The Power Systems division is specialized in providing full solutions instead of individual products for instance power generation solutions or power transmission and distribution. [1]

The Discrete Automation and Motion division provides products, solutions and services for automation and industry. The range of products consists of for instance programmable logic controllers, drives, motors and generators and robotics. Solutions for instance are wind and solar generators and various operations platforms. [1]

The Low Voltage Products division offers low voltage components for wide application field. The product range consists of switches, wiring accessories, enclosures and cable

systems to protect the individual consumer, property and electronic systems from potential hazards of electricity. [1]

The Process Automation division provides solutions and products for safeguarding the industrial process functions. Products offered are instrumentation, control systems, force measurement and turbo charging. [1]

### 1.1.2 Drives and Low Power AC (LAC)

The thesis was carried out at the ABB factory located in Pitäjänmäki, Helsinki.
The factory is divided to an electronics section and to an electric machines & motors section. The site also includes two additional facilities for the ABB service sector and for additional office space.

The electronics unit in the factory designated as Drives produces and develops electric drives of a broad range of output power for various market sectors and applications. The thesis was carried out at the Low Power AC profit centre whose main focus is on low voltage ac drives, and more particularly, their manufacture, design and product support.

## 1.2 Use Case

There are many situations around the world in various surroundings in which an electric motor is the fundamental part of an application. Typical applications for low voltage drives are control of a pump, a fan, a conveyor or various HVAC applications. Let us consider as an example from our daily lives a conveyor system in a shopping mall in which a motor controls a conveyor which moves people up or down between floors.

Like any other motor whether diesel, petrol or hydrogen powered motor, the electric motor needs power to operate. Depending on the type of the motor whether an AC motor or a DC motor, a corresponding electric drive is used to supply the motor with the power it needs. In many applications there are several separate motors operating as one unit, this requires also more drives and for the motors to operate as one also

the drives must work as one. Let us consider a two-motor-driven conveyor illustrated in figure 1 as an example.

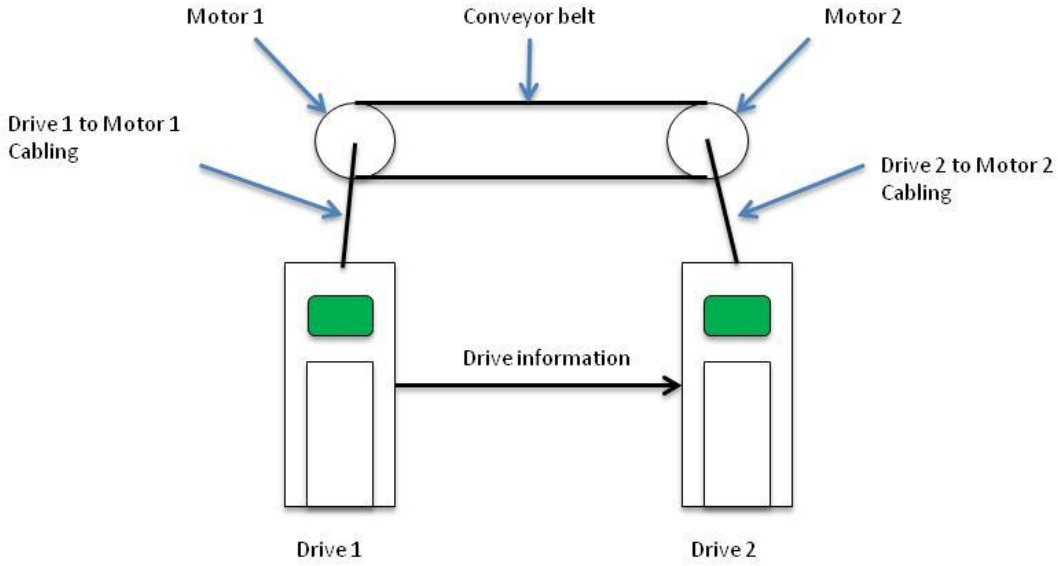



Figure 1 Motor drive application example

In figure 1 two independent motors are moving a conveyor belt. The drive 1 acts as the master and sends for instance speed or torque information for the slave drive 2 to synchronize it to the master's operation pace. Ideally, the information is accurate and they work together smoothly, however if the information is inaccurate the inefficient information transfer may incapacitate the whole system.

## 1.3 Business Case

The project was initiated because ABB was keen on improving the accuracy of the analogue output system in its standard class drives. The current design was old and had not been thoroughly revised for many years. According to the ABB design engineer who initiated the study project highlighted that rivalling companies have more accurate analogue output systems as a standard feature in their standard class low voltage drives and ABB customers have requested better performance analogue outputs from ABB, as well. Therefore ABB wanted to react and answer the competition [2].

## 1.4 Project Definition

### 1.4.1 Objectives

The project objective was to find a viable cost efficient solution to replace or to improve the previous analogue output circuitry design in the old generation frequency converter control board. If successful, the solution would be implemented in the new generation of standard low voltage wall mounted and HVAC frequency converter product line. Furthermore the solution could be implemented in other similar frequency converter control boards that need cost efficient improvement for their analogue output circuitry. Along with the upgrade ABB would improve its competitive edge in the low power frequency converter market as well as the end customer product satisfaction.

### 1.4.2 Scope and Focus

The project scope was set around the analogue output circuits AO-1 and AO-2 of the control board, excluding the technical improvement requirements of external sub circuitry such as reference voltage or the power supply used by the analogue outputs. However, due to the sensitive nature and importance of the reference voltage the immediate effect of its fluctuations was evaluated with simulation.

The focus was set on finding the critical bottlenecks of error sources caused by technological solutions and critical component selections in the circuit and providing a corrective technology solution. The semiconductor device offset voltages and drifts are considered but are secondary in the order of priority. Non-critical passive component drifts are left out of the scope of the study, while critical position resistors and their tolerance effects are evaluated. The classification whether a resistor is in critical or non-critical position will be assessed as the possible circuit technology based errors are analyzed in the forthcoming section 3.1.

The effect of ambient temperature was included in the study scope and a brief study was to be carried out on the overall increase in output current error and identifying the

components that are the most vulnerable to temperature variations in the current solution and designed prototypes. This was, however, done within the limits of the time available.

### 1.4.3 Targets

The targets set for the project were to improve the linearity and the accuracy of the analogue output system. The corrective solution improvement target in the full-scale error performance was set to decrease the gap from the old specified value of +/-3% to +/-1%.

According to the ABB design engineer and definition found from Analog Devices internet site under the list of terms and definitions the full-scale error, also known as the total system error; definition is the maximum error relation to the full-range output as defined in equation (1). [2, 3]

$$Full-scale\,error-\% = \frac{Error_{MAX}\,(mA)}{20mA} \times 100\% \quad (1)$$

Design boundaries set for the project which would limit the ways to reach the targets were that the solutions were to remain cost efficient. Therefore component costs should not increase significantly over the old AO-1 and AO-2 circuit expenses; however any added costs would be eventually weighed against the improved accuracy. The components used must be approved by the sourcing department of ABB for ample availability thus eliminating the use of any special or otherwise exotic components. In addition, the solutions were not allowed to occupy much more physical circuit board space than the previous solutions.

## 1.5 Low Voltage Frequency Converter System

### 1.5.1 The Frequency Converter

Fundamentally a frequency converter is a device which creates AC voltage whose frequency and amplitude can be controlled. The need for frequency converters originates from the need to control an AC motor and particularly its rotational speed and direction.

AC motors are cheaper, more robust and easier to maintain than the equivalent DC voltage counterpart. In addition, today's AC motors can emulate the characteristics of a DC motor making them a very attractive choice among the buyers in today's market over the DC motor. The AC motor speed is directly proportional to the input supply voltage frequency fed in to it and therefore a variable frequency drive is needed to gain full control over the motor. [4]

The typical input voltage range for the low power standard frequency converters is 208-240V; 380-480V; 600V regionally and the output power ranges from 0,75kW to 350kW. [5]

### 1.5.2 Introduction to the Control Board

The functions of a frequency converter system are directed by a control board. Its main tasks are the control of the motor, the frequency converter system control, communication and I/O monitoring. [6]

The control board has several programmable control connections. It has 6 digital I/O's of which digital input number 6 can also be used to measure frequency. The digital I/O's can control and forward for instance control motor rotational direction and on/off command information. The digital I/O's functionalities are very flexible as they are all programmable to meet the customer's needs. [6]

The three relay outputs which can be used to route high voltage control signals such as 230VAC signals that must remain isolated from the control board and the frequency converter such as external control systems. [6]

For analogue type signals the control board has 2 analogue inputs, 2 outputs and a reference voltage output of +10VDC. [6] The analogue inputs can be configured to read either 0-20mA current or a 0-10VDC voltage signal via a dip switch and the corresponding outputs produce a 0-20mA current signal. [6]

The control board houses also a connector for serial communications via Modbus embedded field bus protocol using RS485 interface. The serial communications can also be done using a field bus adapter on one of the two option module slots the control board houses. Other more uncommon field bus communication methods are implemented by using option modules. [6]

The most important communication interface of the control board is the display equipped control panel which enables the system to be configured and controlled locally. [6]

As already briefly mentioned the control board houses two option module connections which allow for instance, the use of extension relay outputs or an encoder for motor speed feedback for additional motor control. [6]

## 1.6 Study Structure

The study was conducted by using both theoretical and practical approach. In the initial part of the study the current system and later on the probable causes of error were first analyzed by applying and evaluating the theories involved in the various components in the circuitry. Additional supplementary information was also acquired by discussing with ABB electronics engineers throughout the project process.

The theoretical approach was further expanded to the use of simulation software and finally the circuit was studied with hands-on-approach in a laboratory.

The laboratory experiments were conducted in various temperature conditions and the system was examined for both the entire circuit and isolated parts of it.

The block diagram of the study structure is given in figure 2 observing the project timeline progressing vertically downwards.

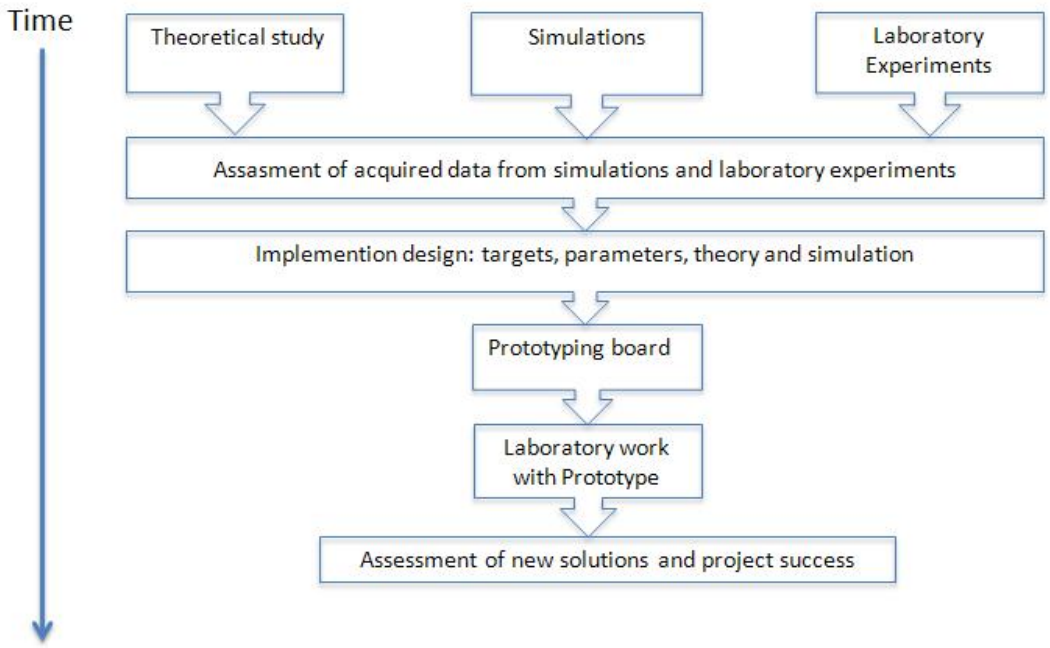



Figure 2 the study structure

In the final part the corrective solutions were designed within the given design parameters and using the error cause data found thus far in the project. The solutions were gathered to a single prototyping circuit board and their performance was measured in the laboratory and finally evaluated against the old solution.

# 2 Project Study

## 2.1 Current Status of the Analogue Output Circuit

### 2.1.1 Initial Analogue Output Simulations by ABB

The ABB electronics design engineer who initiated the project carried out a simulation on the error behaviour of the control board analogue output and the results are given in appendix 1. The simulated current was compared to the output current defined by equation (2 which was found from the original result Excel sheet.

$$I_{out} = \frac{10}{47^2}\left(10 - \left(5 - \frac{5t_{on}}{T}\right)\right) = kD \qquad (2)$$

In which k=constant, D=input signal duty cycle

Equation (2 describes the ideal behaviour of the output stage AO-1 and it plots a linear slope from 0mA to around 22mA as illustrated below.

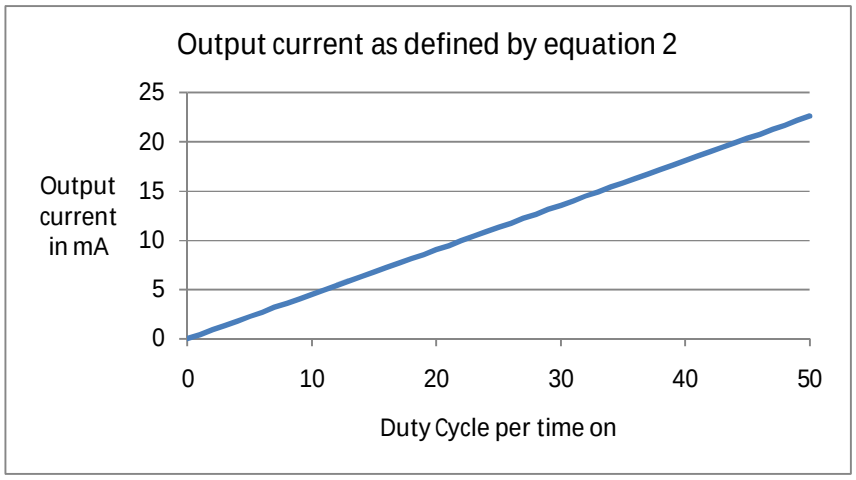



Figure 3 the ideal output current

According to ABB electronics research and development, the slope is purposely over ranged to ensure that the output is guaranteed to achieve 20mA regardless of component tolerances and increased load. Furthermore, in many applications the system is

set in such a manner that the output never falls to 0mA, instead a 4mA current is considered as the zero-level [2]. This is due to the reason that if there is always some current flowing in the loop, the integrity of the system can be easily monitored: once the current ceases to flow it immediately indicates a fault in the loop [2]. The properties of a current loop will be further discussed in section 2.2.3.

Equation 2 is derived from the output stage circuit of the AO-1 illustrated in the following page in figure 4, which transforms voltage to current. The input voltage is fed to the circuit from the left side node of R712 and the output current $I_{out}$ is taken from the connector pin X1-7.

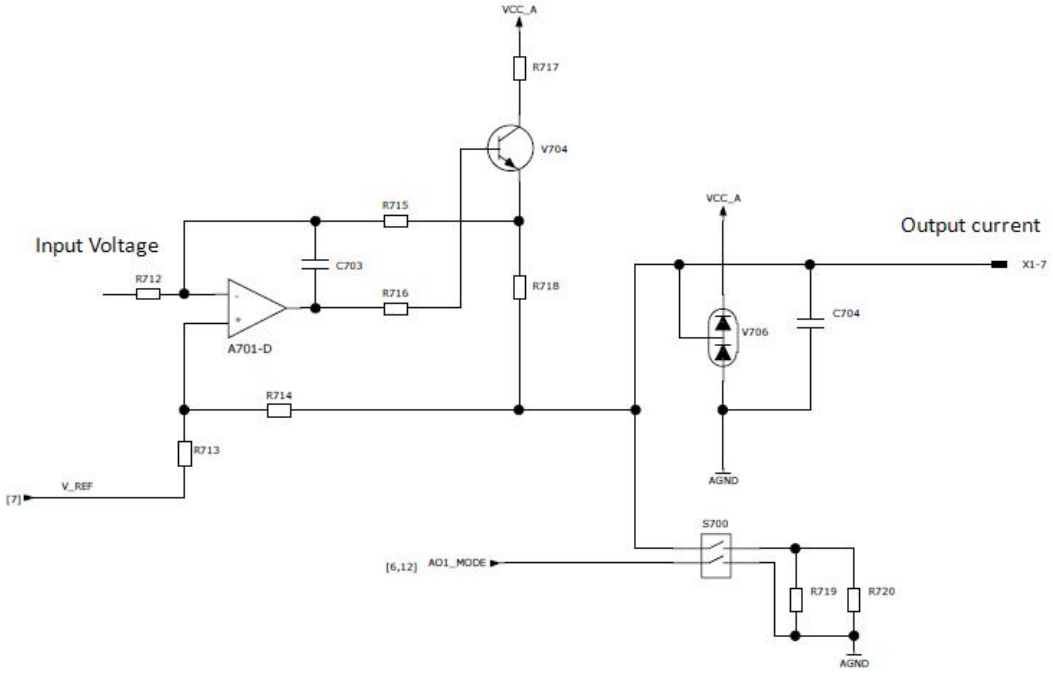



Figure 4 the output stage of the control board analogue output

If the pulse width modulation signal sent by the microcontroller is transferred to the output stage circuit linearly and the output stage would work ideally, equation (2 would also describe the transfer of the entire system. This seems not to be the case as there is an error produced to the output current as illustrated in figure 5.

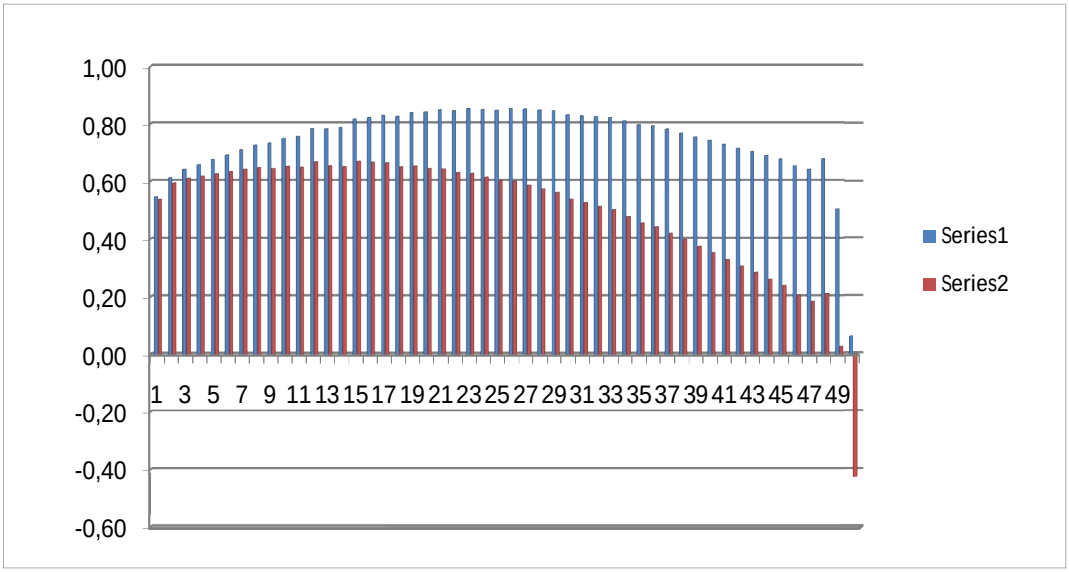



Figure 5 initial analogue output simulation results

Figure 5 provided by ABB represents the error in milliampere calculated by subtracting the ideal current defined by equation (2 from the simulated output current results in respect to the input signal pulse width in micro seconds. The blue columns designated as series 1 are the simulation results for the old generation control board but they will be discarded as they are out of the scope of the study and present control board simulation results can be seen in the red columns referred to as series 2.

The general behaviour of the series 2 curve resembles a downward open parabola justified strongly to the left. The maximum error of 0,670mA was found at 16us of time which translates as 32% duty cycle input signal. The simulation results are provided in appendix 1. By using equation 1 the full-scale error for the simulated system can be calculated as

$$Error - \%_{Full-Scale} = \frac{0{,}670mA}{20mA} \times 100\% = 3{,}35\%$$

According to the simulation the output clearly exceeds its specification of +/-3%.

## 2.2 Analysis of the Current Solution

### 2.2.1 Functionalities of the System

The fundamental transfer concept of the system is based on the extraction of the average value of a pulse width modulated signal to form a control voltage which can be used to drive a voltage-to-current transformer circuitry that produces the final output current for the loop. The properties of the system PWM signal will be discussed in section 2.2.3.

The AO1 and AO2 can be divided in to four fundamental functional blocks, which translate the initial PWM voltage signal in to the direct current form. These sections in the signal flow are the galvanic isolation stage, the waveform shaping stage, the filtering stage and the voltage-to-current transformer stage. The control board analogue output schematic is provided in appendix 2 and the system block diagram is shown in figure 6.

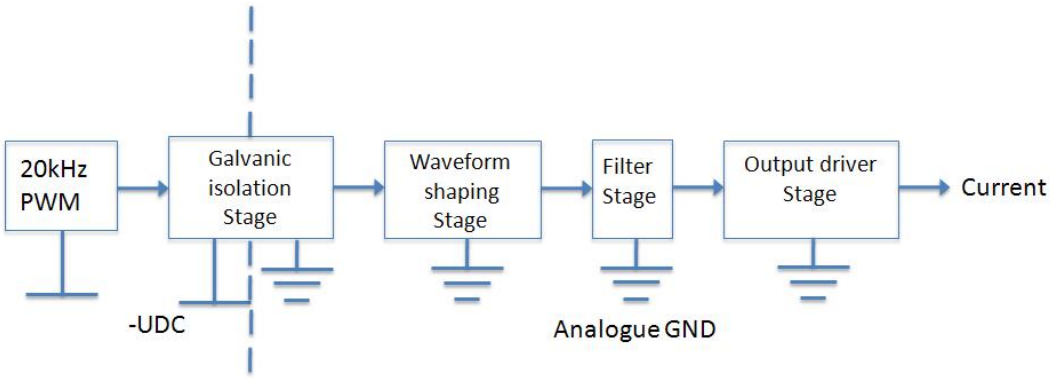



Figure 6 the block diagram of analogue output system

The functionality of the galvanic isolation stage is a critical part of the system as there are very high voltages present in the control board. Due to the current frequency converter design topology many of its circuits are in the mains potential. The figure 6 shows how the AO1 and AO2 ground potentials are connected to the –UDC which is the negative high potential DC voltage rail.

Input supply AC voltage for current generation low voltage frequency converters ranges regionally from 208V to a maximum of 600V and the DC voltages in the DC

supply rails can be as high as the input supply AC voltage maximum or minimum value times the square root of 2 which gives such a high value that it can be potentially lethal. Therefore due to safety reasons regulated by the IEC standard 61800-5-1 it is critical to isolate the hazardous voltages out of the reach of the user. [6, 7] The galvanic isolation functions as an electrical separation between the high voltage potential of the main circuit in the frequency converter and user potential, thus providing a necessary safety measure to meet the IEC 61800-5-1 standard. [8]

Galvanic isolation is also used to minimize the measuring error due to noise caused by ground currents. Especially in power electronics applications which use high currents, a small milliampere scale signal can be completely lost in the midst of noise caused by ground currents. If there is no galvanic contact between the smaller signal and high power grounds the influence of ground current from the high power circuitry is effectively eliminated from interfering the small signal.

The waveform shaping stage functions as a square wave shape enhancer or as a squarer if you will. Due to the nature of the technology used in the isolation stage the signal waveform is altered during the isolation and the linearity of the transfer is compromised, therefore a signal shaping circuit is introduced to the signal path to restore the signal with its original square wave shape.

While the shaping circuitry safeguards the linearity of the transfer, it also serves as a voltage level shifter and logic inverter. The circuit is required to pull up the microprocessor PWM output signal level to higher potential for the DC voltage controlled voltage-to-current transformer stage to produce a desired dynamic range for the current output, in addition the circuit inverts the signal meaning that when the microprocessor output signal is high the waveform shaping circuitry output signal is low.

After the DC-level shift the signal is fed in to a Sallen-Key low-pass filter which is an important part of the analogue output circuitry, because it is responsible for separating the PMW signal average value that is used to control the output stage voltage-to-current transformer, from the rest of the harmonically complex signal. Furthermore,

the filter is responsible for keeping the noise level caused by the harmonics as low as possible.

The final functionality is the voltage to current converter, which translates the average voltage value of the PWM signal to corresponding 0-22mA output current as briefly already discussed in section 2.1.1.

### 2.2.2 Technology Solutions

The schematics analysis was done using the same block diagram and functionality approach as presented earlier in section 2.2.1. In the following section, however, the solutions are studied in deeper detail. The circuit topology was examined in both component and circuit configuration level. Due to the fact that the outputs are almost identical the analysis is conducted using only the AO1-channel part references in the control board schematics and in the case of any discrepancy between signal paths further information will be provided for the reader.

The isolation circuit shown in figure 7 is based on an open collector optocoupler designated as V702, which is driven by the V700 N-channel enhancement-type MOSFET. The MOSFET is configured to operate as a high-speed electronic switch which will operate according to the logic state of the PWM. The switch opens and closes a path for current through the optocoupler transmitting LED which will illuminate and darken accordingly.

The PWM signal is fed to the MOSFET's gate through the R700 gate-stopper resistor which protects the MOSFET from high frequency oscillations that may occur during logic transitions, it is also the first part of a two-resistor-voltage divider formed by R700 and R701 that determines the amount of voltage that is used to drive the MOSFET's gate [9].

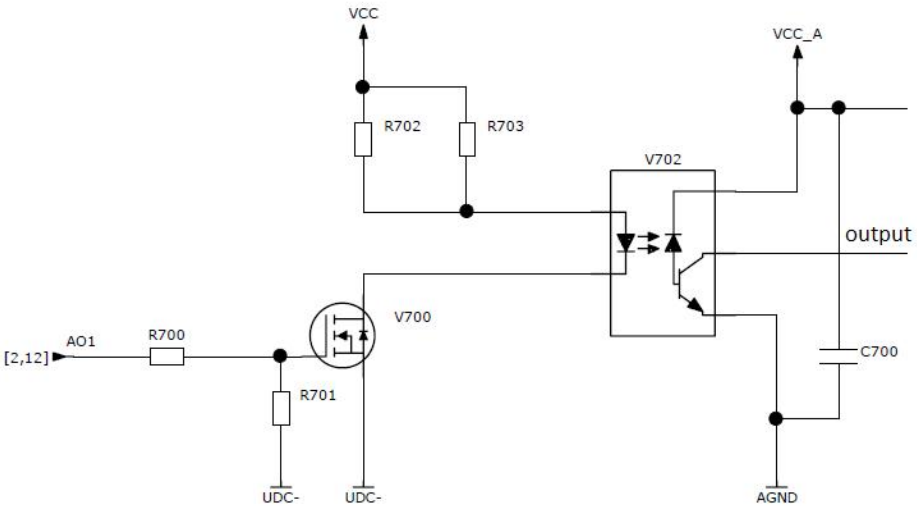



Figure 7 the isolation stage

The voltage divider gives as output voltage a fraction of the input PWM signal determined by its impedance ratio as illustrated in figure 8 and the voltage distribution can be calculated using the equation (3).

$$V_{out} = \frac{Z_{out}}{Z_{in} + Z_{out}} \times V_{in} \tag{3}$$

The second series resistor R701 in the voltage divider also serves as a pull-down resistor and ensures that the MOSFET gate voltage is able to discharge to 0V when the PWM state is driven low by the microprocessor and the gate voltage is always resolved in respect to the ground.

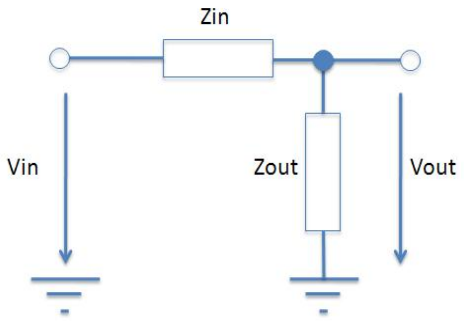



Figure 8 the voltage divider

The voltage divider values are generic but chosen so that the MOSFET's gate will see enough voltage to cover threshold voltage, $V_{Th}$, which is needed for the channel to form and the overdrive voltage, $V_{od}$, which will broaden the channel to deeper saturation. Once overdriven the switch is open and according to the datasheet of the MOSFET provided in appendix 3, the on-state resistance, $R_{DSon}$, is small enough to be considered negligible and the cathode of the optocoupler LED will effectively see –UDC.

The transmitter in the optocoupler designated as V702 is a light emitting diode which emits infrared light. A LED is a current controlled device and therefore the LED current is correctly limited by using the two parallel connected resistors R702-703 to prevent device destruction and proper LED operating current.

The photo detector in the optocoupler is a photo diode which is connected to the user potential analogue power supply from its cathode therefore being reverse-biased, it is also shunted to the user potential analogue ground via bypass capacitor [10:3.2]. The bypass capacitor is a common enhancement component, which ensures correct switching operation. [10:3.19]

The optocoupler operates as an electronic switch in similar manner as the MOSFET and serves as a logic driver for the comparator in the waveform shaping stage illustrated in figure 9.The incoming photo current from the transmitting LED will be received by the photo detector which will in turn drive the transistor in the optocoupler to conductive state and optocoupler output will fall to logic low [10:3.2]. Once the photocurrent diminishes the transistor will turn off and the optocoupler output will be pulled to logic high level determined by the voltage divider formed by resistors R704 and R706.

In addition to the optocoupler secondary and the aforementioned voltage divider the waveform shaping circuit utilizes two more functionalities: a resistive voltage divider formed by R705 and R707, and the A700-A comparator.

According to the A700-A datasheet found in appendix 4, the device is an open collector type comparator. The type definition comes from the topology of the comparator out-

put stage, in A700-A the output transistor's collector is open in default, hence the name open collector comparator.

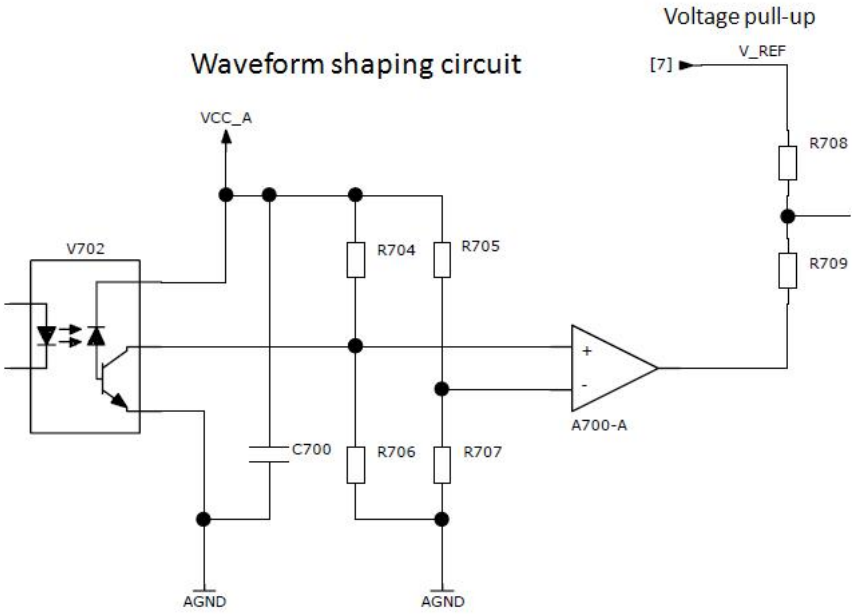



Figure 9 the waveform shaping stage

The second voltage divider formed by the R705 and R707 sets the static threshold voltage level $V_{Th}$ for the comparator.

The device selections for the isolation and waveform shaping circuits forces the PWM logic operation to inverse as displayed in the truth table below.

Table 1 the truth table of the waveform shaping stage

| | Logic state | |
|---|---|---|
| Micro processor PWM | High | Low |
| Optocoupler output | Low | High |
| Comparator Output | Low | High |

This immediately affects the configuration of the output stage as we will see later on in this section.

The comparator output is connected to a reference voltage with two equal value resistors R708 and R709 in series. This circuit forms the voltage pull-up stage of which the output to the following stage is coupled in the net between the resistors. The comparator's output logic states will be effectively pulled up to low level of half $V_{ref}$ and high level of $V_{ref}$ for the subsequent filter circuit illustrated below.

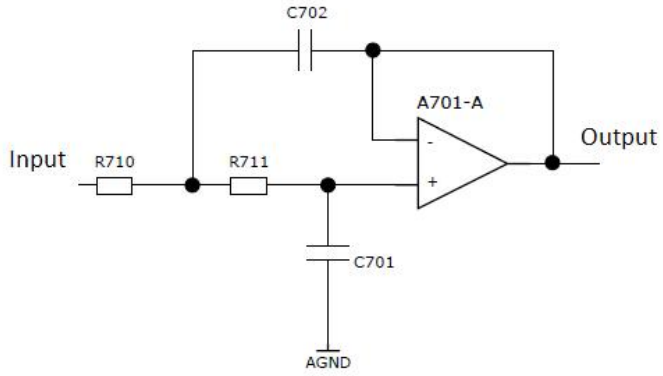



Figure 10 the filter stage

The Sallen-Key topology low-pass filter circuit is based on a conventional operational amplifier A701-A. The operational amplifier itself is a voltage follower and the input section has two frequency selective filtering networks formed by R710-711 and C701-702.

The transfer function of the Sallen-Key filter describes the signal transfer through the system [11:32]. It can be shown that the transfer function of the filter is as derived in equation (4) [11:1009-1010, 12].

$$H(s) = \frac{\omega_0^2}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_0^2} = \frac{1}{R^2C^2s^2 + 2RCs + 1} \tag{4}$$

In which the corresponding components found in the circuit are R=R710=R711, C=C701=C702.

Requiring the component values are selected as R=R710=R711 and C=C701=C702 the filter cut-off frequency can be determined as in equation (5) [13:745-746].

$$f_{-3dB} = \frac{1}{2\pi RC} \tag{5}$$

Taking note that the transfer function denominator, also known as the characteristic equation, is a second order polynomial which means that that the filter is second order. This quality gives the Sallen-Key topology filter its excellent filtering properties since a second order filter has 40dB per decade attenuation above its cut-off frequency which in this case is determined by equation (5).

The voltage-to-current converter stage shown in figure 11 is a modified class-B type power amplifier with only the pushing output transistor.

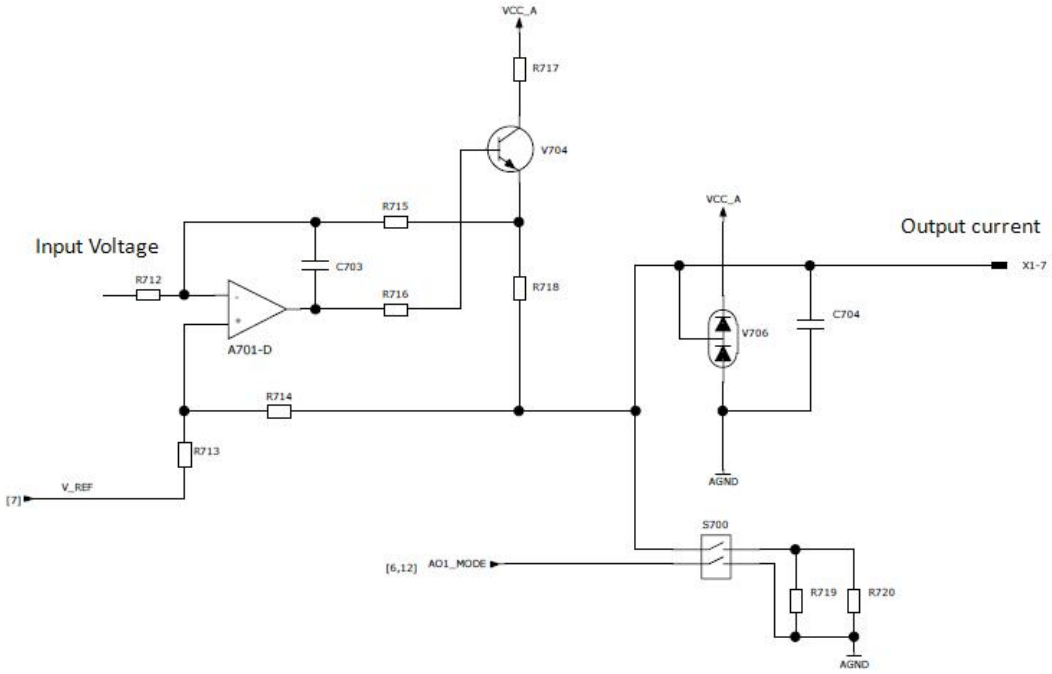



Figure 11 the output stage

The output of the conventional A701-B operational amplifier is used to drive the base of the V704 bipolar transistor. The control and reference voltages are inserted to the

operational amplifier through the resistors R712 and R713 to create a differential control voltage to the operational amplifier inputs. The system stability is increased by using additional resistive and capacitive feedback.

The resistive current sensing feedback from the transistor V704 emitter is formed by the resistors R715 and R714. These feedback resistors smooth the operation of the output stage and stabilize the operation in harsh conditions. The C703 creates stabilizing capacitive feedback against high frequency oscillations and noise that might be encountered in the output of the operational amplifier.

The output current is sourced from the VCC_A power supply network through the resistors R717 and R718. The resistor R716 limits the drive current which is fed to the base of the drive transistor V704 to limit the accumulating transistor base charge thus aiding its recovery from saturation which in turn improves the response time of the output circuit.

The final components of the output circuits are the output current smoothing and filtering capacitor C704 and the transient protection diode V706. The V706 protects the output stage from fast overvoltage spikes that can potentially damage the output circuit components and other systems that are connected to the AO1.

The only functional difference between AO1 and AO2 is at the output stage, namely the optional voltage output selection via S3. In the AO1 the switch S3 can be switched to drive the output current to resistive load formed by the two parallel-connected resistors R719 and R720 thus changing the output current to voltage form.

### 2.2.3 Signals of the System

A signal is an information carrier and in the control board analogue output system the primary information carrier signal is the pulse width modulated square wave voltage signal. The PWM signal used in AO1 and AO2 is only modulated in duty cycle, however may it be noted that there are additional further modulated PWM methods but such signals are beyond the scope of the thesis [14].

A DC voltage is a constant voltage which does not vary in time. It can be modulated to produce a square wave signal by for instance repeatedly turning the DC voltage output on and off using a switching mechanism as given in figure 12.

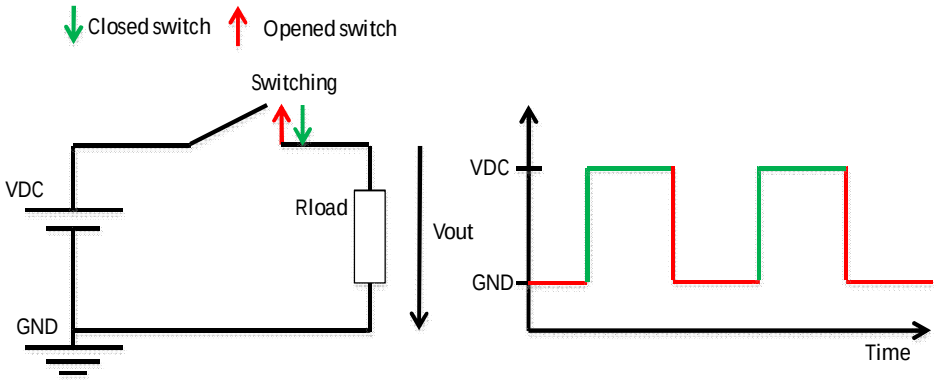



Figure 12 DC-voltage to square wave using a switch

When the switch is closed the voltage over the load will be the VDC and when the switch is opened the voltage will fall to GND. The square wave in figure 12 is symmetrical in waveform, in other words the voltage is equally long time in both VDC and GND potentials but there is no obstruction to alter the times to be unequal which takes us to the essence of PWM which is an abbreviation for pulse width modulation.

The essential time definitions are illustrated in figure 13. The time the output is high is referred to as $t_{high}$ and the time low $t_{low}$ respectively, and the sum of these factors is the pulse period T.

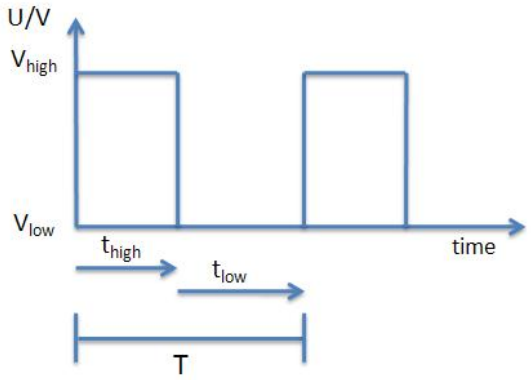



Figure 13 a PWM signal

The PWM is basically control over the $t_{high}$ to extend it to last the whole period, part of it, or remain low for the whole period, hence the name pulse width modulation. The $t_{high}$ relation to the overall period is called duty cycle which is defined in the equation (6).

$$Duty\ cycle = \frac{t_{high}}{Period} = \frac{t_{high}}{T} \tag{6}$$

The duty cycle is also sometimes given as a percentage value which only means that the duty cycle ratio in the equation above is multiplied with 100%.

In the system at hand, the information is carried in the average value of PWM signal. The general function defining the average voltage value of the periodical PWM signal is defined by an integral over the pulse period as given in equation (7).

$$V_{average} = \frac{1}{T}\int_0^T f(t)dt \tag{7}$$

If the function $f_{high}(t)$ describes the voltage when the pulse is high and $f_{low}(t)$ the voltage when the PWM voltage is low, the equation (7) can be written as

$$V_{average} = \frac{1}{T}\left(\int_0^{t\,high} f_{high}(t)dt + \int_{t\,high}^{T} f_{low}(t)d\right) \tag{8}$$

For a PWM signal with a $V_{low}$ value of 0, which is a typical case for microcontroller generated PWM signals such as in the AO-1 system, the latter integral over $f_{low}$ (t) in equation (8) yields 0, thus the equation (8) can also be written for 0 to $V_{high}$ voltage range PWM as below

$$V_{average} = \frac{V_{high} \times t_{high}}{T} = V_{high} \times Duty\ cycle \tag{9}$$

From equation (9) we can see that the average value output will be a portion of the maximum voltage defined by the duty cycle.

A periodic function such as a PWM square wave signal can be represented as an infinite sum of sinusoidal and cosine harmonic components in both time and frequency domain. The fundamental theorem behind these representations is the Fourier series. The full derivation of the mathematical dependencies regarding the Fourier series and Fourier transformation is beyond the scope of this thesis, however a small introduction to the Fourier series is important so that the properties of the PWM signal and the importance of the filter circuit in the current solution are more profoundly understood.

The most common ways to represent the Fourier series for periodic functions are the real development as defined in equation (10) and the complex coefficient defined in equation (11). [15, 16]

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos\left(\frac{2\pi nt}{T}\right) + \sum_{n=1}^{\infty} b_n \sin\left(\frac{2\pi nt}{T}\right), n = 1,2,3... \tag{10}$$

$$a_0 = \frac{1}{T}\int_h^{h+T} f(t)dt,\ a_n = \frac{2}{T}\int_h^{h+T} f(t)\cos\left(\frac{2\pi nt}{T}\right)dt,\ b_n = \frac{2}{T}\int_h^{h+T} f(t)\sin\left(\frac{2\pi nt}{T}\right)dt$$

$$f(t) = \sum_{n\in Z} C_n e^{i\frac{2\pi nt}{T}} \tag{11}$$

$$C_0 = a_0, \quad C_n = \frac{1}{T}\int_h^{h+T} f(t) e^{-i\frac{2\pi nt}{T}} dt$$

Recalling the equation (7) we can see that the first term $a_0$ describes the average value of the signal f(t) while the latter terms in both developments describe the harmonic content of the signal which will define its waveform.

It can be shown that the average value and the harmonic content coefficients of the PWM signal in the analogue output yield as defined below [17].

$$a_0 = \frac{1}{L}\int_{-L}^{L} f(t) = \frac{2V_+ t_{on}}{L} = 2V_+ D$$

$$a_n = \frac{1}{L}\int_{-L}^{L} f(t)\cos\left(\frac{n\pi t}{L}\right)dt = \frac{2V_+}{n\pi}\sin(n\pi D) = 2V_+ D\frac{\sin(n\pi D)}{n\pi D}$$

$$b_n = \frac{1}{L}\int_{-L}^{L} f(t)\sin(n\pi t)dt = 0$$

In which the duty cycle is bound to 0≤D≤1. Differentiating the acquired $a_n$ equation in respect to duty cycle and solving the roots will show that the maximum value of $a_n$, and therefore the greatest amplitude of a harmonic is present when the duty cycle is 50%. It can be also shown that the fundamental harmonic is the strongest. The maximum amplitude of the harmonic can be evaluated by using the function for $a_n$ in the function of the duty cycle and substituting D=0,5 and n=1 yields

$$a_n = \frac{2V_+}{\pi n}\sin(n\pi D) = \frac{2V_+}{\pi}\sin(0{,}5\pi) = 3{,}18[V]$$

As we can see the magnitude of the first harmonic can be very large and therefore the importance of effective filtering which prevents these components from causing noise to the system is emphasized.

As mentioned earlier, the harmonics give the pulse its distinctive waveform. The more the harmonics are calculated using the Fourier series the closer the representation of the signal will be as shown in the example 50% duty cycle +/-1V peak-voltage square wave signal in figure 14.

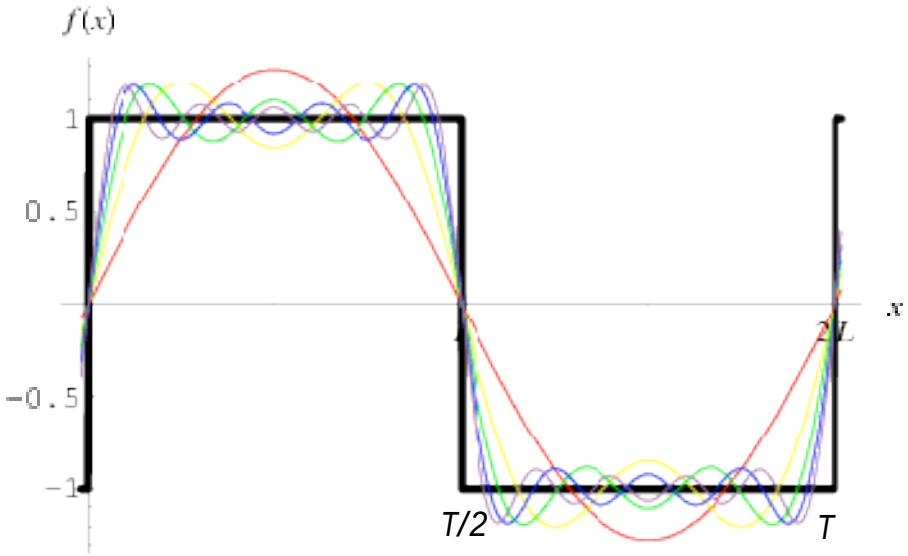



Figure 14 A square wave pulse harmonic composition in time domain [15]

The figure 14 illustrates how the added harmonics gradually shape the overall signal, the red curve is the first harmonic, also known as the fundamental frequency, the black curve is the ideal signal and the purple curve has five summed harmonics.

The harmonic content of a signal can also be represented in the frequency domain by using the Fourier transformation. The theory behind the Fourier transformation is beyond the scope of this thesis but in short, the Fourier transformation shifts the time domain Fourier series harmonics to the corresponding frequencies in the frequency domain. The Fast Fourier Transformation is a method of Fourier transformation which requires less calculation developed for fast analysis of signals.

The DC current output signal is generated by a controlled constant current source which pushes current to the receiving circuit as described in sections 2.2.1 and 2.2.2. In ideal case the current is constant regardless of the load resistance but in reality the maximum load is limited by the qualities of the current driver stage.

The main advantage of the current signal over voltage signal is the nature of information transfer. A current signal system is a series loop and it obeys the Kirchoff's current law [18]. Using figure 15 as an example, the Kirchoff's current law states that the transmitted current signal is exactly the same along the signal path from the transmitter to receiver's load and back to the current transmitter regardless of the resistance caused by for instance the leads connecting them. [18, 19]

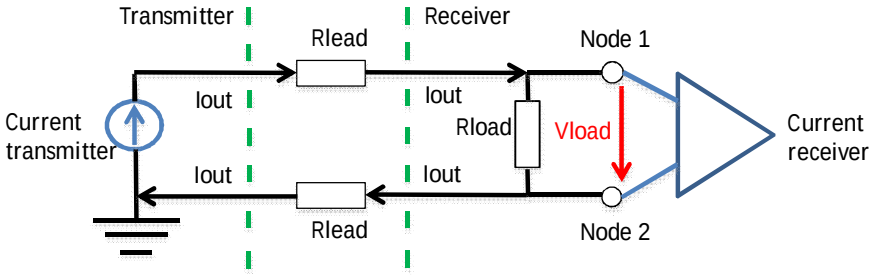



Figure 15 a current signal loop

Figure 15 displays the operation of a DC current loop. The current transmitter sends out a DC current signal $I_{out}$ which flows through the $R_{load}$. The same initial current re-

turns to the transmitter circuit just as the Kirchoff's current law states, therefore in theory the current signal provides very accurate information transfer. The current signal is read typically as a voltage $V_{load}$ at the receiver end from the nodes 1 and 2 over the $R_{load}$ by an analogue to digital converter for example. The most common current range is the 4-20mA range driven in to a 250Ω load as this transcribes conveniently to a voltage range of 1-5V used by common analogue to digital converters. [18]

The AO-1 provides also a voltage output option which will divert the output current to a resistive load $R_{out}$ which translates the current to a voltage value and the functional diagram is shown in figure 16. The voltage output obeys the Kirchoff's voltage law which states that the net sum of the voltages in a closed-loop is 0V [20].

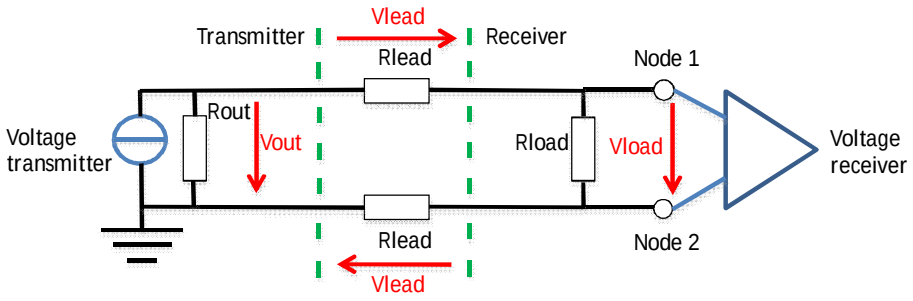



Figure 16 a voltage signal transfer

If the voltage losses over the leads are considered negligible, applying the Kirchoff's voltage law to the figure 16 will show that the $V_{out}$ will be completely dissipated over the $R_{load}$ as $V_{load}$ as the net voltage must be 0V. In reality the voltage mode does not transfer the true $V_{out}$ to the load but instead there are some voltage losses in the transfer due to the connecting cabling. However, the voltage system supports the connection of multiple receivers better than a current loop, because the voltage transfer can support common ground potential sharing unlike the current loop [2,21].

# 3 Root Cause Analysis

## 3.1 Identifying the Sources of Error

To identify the most probable and significant sources of error, the focus is to be set on finding functionalities and components which before the averaging stage alter the PWM duty cycle and its DC voltage level and after that the control signal DC level.

The first component of interest in the circuit is the V702 MOSFET. The MOSFET's behaviour in switching mode is symmetrical and it should not introduce a significant duty cycle error to the PWM in this perspective [11:535]. However the MOSFET's channel must be sufficiently overdriven to ensure proper current flow through its channel and the LED in the optocoupler throughout the control board's life cycle [11:360-363]. Calculating the MOSFET gate voltage and subtracting the $V_{Th}$ found from the datasheet from it, the overdrive voltage was found to be 2,26V which should be sufficient enough. The MOSFET seems robust against temperature fluctuations as well. Once again referring to the datasheet the MOSFET's $R_{DSon}$ and the $V_{Th}$ are sufficiently unaffected by temperature effects.

The first probable cause of error is the required isolation optocoupler. Its key characteristics are the propagation delay, current transfer ratio (CTR) and the optocoupler transistor base time constant.

The propagation delay describes the time delay introduced to the signal during the isolation [10:3.11]. The propagation delay is separated to optocoupler output rising and falling edge related delays which are designated as $t_{pLH}$ and $t_{pHL}$ respectively. The propagation delay definition can vary between device manufacturers, however a common definition and the definition used in this thesis is given in the timing figure 17.

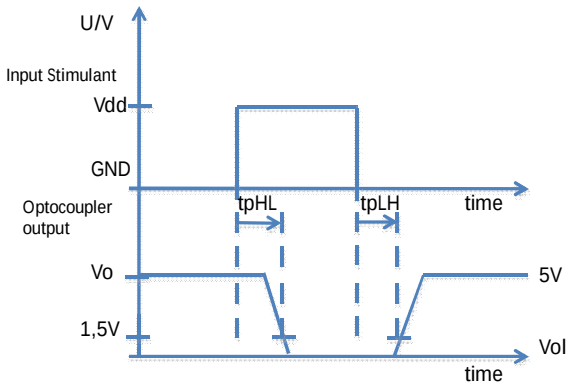



Figure 17 $t_{pHL}$ and $t_{pLH}$ definition

We can see from figure 17 that the optocoupler output falls and rises to a certain threshold level which defines the level of transition between the states. In addition, it is clear that propagation delays must remain symmetrical for the system PWM signal pulse width to preserve its original value.

The LED forward current determines the amount of photons sent to the photo detector, therefore the larger the $I_f$ the faster the $t_{pHL}$ but on the other hand, the $t_{pLH}$ will be slower due to the transistor's increased recovery time from saturation [10:3.11]. In addition the current transfer ratio, CTR, which describes the quality of the transfer between the input current $I_F$ and output current $I_{out}$ in percentage affects the propagation delays because it has a similar effect as a variable $I_F$.

$I_f$ in AO-1 is found to be

$$I_F = \frac{V_{Supply} - V_{Forward}}{R_{Anode}} = \frac{VCC - 1{,}65V}{(R702 // R703)\Omega} = 11{,}97mA \approx 12mA$$

The specifications in the optocoupler datasheet, provided in appendix 5, for unity propagation delays are gained with 16mA forward current and 5V supply voltage into around 3,3kΩ load. In the analogue output the supply voltage is higher but the load is scaled accordingly; nevertheless a 12mA forward current does not reach the requirements for symmetrical operation.

While the load is dimensioned properly to accommodate the higher supply voltage, the transistor's base time constant is altered. The base time constant determines the response speed of the transistor and is defined by equation (12)

$$\tau_B = R_B\left(C_{PD} + C_{BC}\right) + \beta R_L C_{BC} \tag{12}$$

In which $C_{BC}$ and $C_{PD}$ are the transistor base and stray capacitances, $R_L$ is the load resistance, β is transistor gain and $R_B$ is the transistor dynamic resistance [10:3.10-11]. We can see that although the time constant is greatly determined by the manufacturing process an increased load resistance effectively slows the response of the transistor as well. The dynamic resistance depends on the current transfer ratio, forward current and the transistor gain as in equation (13). [10:3.10-11]

$$R_B = \beta \frac{25mV}{\frac{CTR}{100\%} I_{Fdc}} \tag{13}$$

Due to component sourcing reasons the parameters in equation (12) cannot be controlled and thus the behavior of the optocoupler may vary greatly [2].

The optocoupler digital speed of operation is 1Mbit/s with maximum propagation delays of 0,8µs. Which means the optocoupler should be able to transmit one million falling or rising edges in a second that can be referred to as a threshold and interpreted. From the system point of view the optocoupler performance supports the transfer of maximum frequency of 1µs pulses which translates as the system PWM 2% duty cycle length which eventually means transfer problems at high and low duty cycles.

From the temperature variation's point of view $t_{pHL}$ and $t_{pLH}$ follow a different temperature relation curve. According to the datasheet the $t_{pLH}$ is noticeably more sensitive to temperature variations, which effectively means that the ambient temperature will cause it to increase or decrease more than the $t_{pHL}$ thus creating pulse width distortion. The waveform shaping stage key point is the comparator device and the voltage pull-up load it drives. The surrounding voltage dividers do determine the threshold voltage for the comparator but are less important.

The comparator device schematic is given in figure 18. When the output is to change from high to low, the output transistor is driven into saturation by shutting down the driver transistor and the output will be actively turned to low. However the weakness of the open collector type comparator is observed in the changeover from low to high as the high state is achieved by simply passively pulling up the voltage through a load.

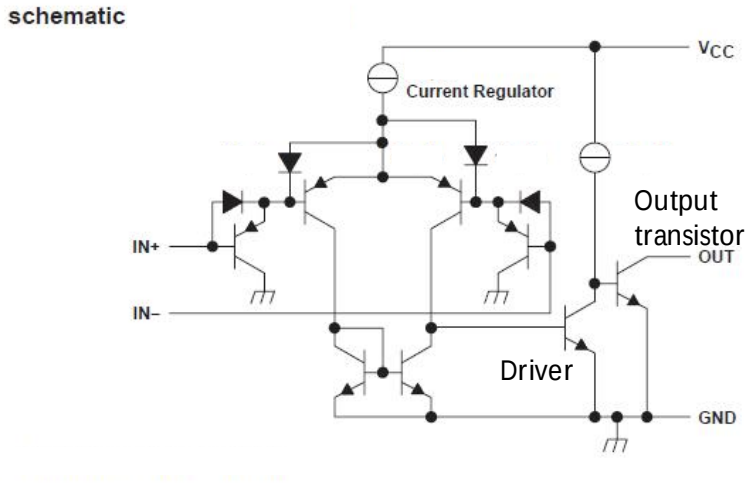



Figure 18 internal schematics of the comparator

As the device output operates both passively and actively, of which the active mode is substantially faster than the passive, the signal duty cycle accuracy will be compromised. In addition to the probable pulse width distortion (PWD) the logic levels and the low level in particular of the comparator are not as the design requires. According to the device datasheet the output low-level ranges from 150mV to 400mV at around 4mA output current instead of the intended 0V. The immediate effect to circuit will be that the filter will put out higher average value and the output current will be altered.

The comparator input side voltage divider resistors have 1% tolerance and it can be shown that the corresponding input voltage and threshold voltage variations in percent are as calculated using equation (14)

$$V_{Variation} - \% = \frac{V_{ideal} - V_{WCS}}{V_{WCS}} \times 100\% \qquad (14)$$

Which yields for the input voltage a variation of +/-1% and for the threshold voltage a +/-1,8% variation.

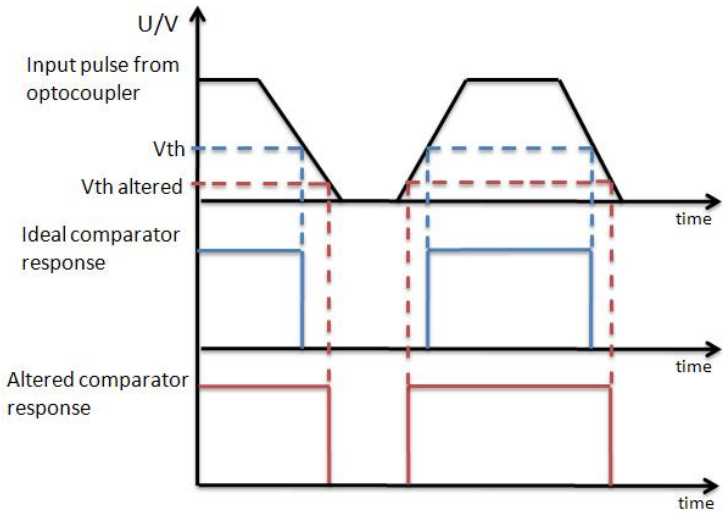



Figure 19 effect of altered comparator threshold voltage

From figure 19 we can see that the threshold voltage has an impact on the PWM duty cycle and the voltage divider has a key task in defining the pulse width of the signal. However since the comparator operates in conjunction with the optocoupler the accuracy of this voltage setting will be for naught if the optocoupler output signal varies greatly between the units due to device properties or locally due to temperature variations. In comparison to $V_{th}$ .the input voltage variations are less important.

The voltage pull-up is identical to the input voltage divider and therefore the 1% tolerance resistor caused error is the same as calculated earlier +/-1%. The average voltage variations seen by the filter can be written as

$$V_{average} = (V_{low} \pm 5mV) + D((V_{high} - V_{low}) \mp 5mV) \quad (15)$$

Which yields in the worst case scenario +/-25mV offset discrepancy with respect to the ideal voltage.

The Filter stage resistors and capacitors have 1% and 5% tolerances respectively. Despite the capacitor high tolerance the filter is relatively sturdy to component tolerance variations due to the fact that it is second order and its bandwidth is set very low as we can see from calculations in the following page done by using the equation (5)

$$f_{-3dB} = \frac{1}{2\pi(R710)\Omega \times (C701)F} = 159{,}15Hz \approx 160Hz$$

Furthermore, expanding the equation (4) to calculate the absolute value of the gain at a certain harmonic frequency and substituting s=jω, and recalling $\omega = 2\pi f$ yields

$$|H(j\omega)| = \frac{1}{\sqrt{\left(R^2C^2\omega^2+1\right)^2 + \left(2RCj\omega\right)^2}} = \frac{1}{\sqrt{\left(R^4C^4\omega^4 + 2R^2C^2\omega^2 + 1\right) + \left(4R^2C^2\omega^2\right)}}$$

$$|H(f)| = \frac{1}{\sqrt{R^4C^4(2\pi f)^4 + 6R^2C^2(2\pi f)^2 + 1}}$$

$$|H(20kHz)| = \frac{1}{15794}, \quad A_V dB(20kHz) = 20\log_{10}\left(\frac{1}{15794}\right) \approx -84dB$$

It is easy to see that the attenuation at first harmonic frequency of 20kHz is so strong that slight fluctuations in cut-off frequency do not significantly affect the performance of the circuit.

The operational amplifiers are prone to DC imperfections such as input offset voltage and offset current. The offset voltage means that there is some voltage between the input pins due to internal structure of the amplifier even though in theory this voltage should be 0V. The input offset voltage can be either negative or positive voltage which means that it can reduce or increase the output voltage slightly [11:121-122]. The operational amplifier has according to the datasheet a 9mV input offset voltage which will be summed or deducted from the input DC voltage which will eventually be the voltage follower output signal. The operational amplifier datasheet is given in appendix 6.

May it be noted that in the operational amplifier there are also input bias currents present. However according to the operational amplifier's datasheet the input offset current poses so small error in the whole scale that it can be considered negligible. How the bias currents possibly load the output is unclear, in any case they are also considered insignificant and therefore are left without further examination.

It is also rather common knowledge that although some operational amplifiers are specified to handle the single side power supply configurations, they usually do not perform as well near ground nor supply rail voltages. Therefore there is a possibility that this feature affects the averaging process as well, however the how much is uncertain.

In the output stage the operational amplifier suffers from the same DC-imperfections as the device in the filter and because the output stage is DC voltage driven they may cause noticeable error. Also the device is similarly powered with single sided supply which in this stage may cause noticeable error in the form of inaccuracy or it is unable to shut down the output transistor.

However the utmost critical components in the output stage are the feedback and output resistors that will eventually define for most part the accuracy of output current. Although the tolerances are kept in 1% limit the feedback system itself is asymmetrical. The inputs are fed with differing information as the inverting input will see a feedback voltage smaller by the voltage over the R718. Due to the complexity of circuit configuration the effect of the resistor tolerances and the feedback topology will be further examined using simulation.

## 3.2 Simulation

### 3.2.1 Simulation Using the Orcad Capture 16.2

The circuit functionalities were simulated using Orcad Capture version 16.2 and Orcad Capture Demo version. The software uses PSpice models to mathematically describe the behaviour of components. In addition to basic circuit simulation the Orcad Capture

is able to calculate worst-case scenarios of the circuitry due to component tolerances and attributes.

### 3.2.2 Simulation Limitations

The simulation result is as good as the available PSpice models. The PSpice model parameters are measured and defined by the device manufacturer from the actual device. If the parameters are unavailable the software user can approximate a device by creating own models, however by doing so the overall simulation profile will not fully reflect the actual circuit. The AO1 circuitry uses an optocoupler, which had no PSpice model and for the simulation purposes it was replaced with another device hence the simulation results can only be regarded as approximation for the optocoupler functionalities.

### 3.2.3 Simulation Process

The AO1 circuitry was constructed with Orcad Capture to as close to the actual circuit as possible by using the corresponding components, values, tolerances and device manufacturers. AN2504A was selected as the substitute for the true optocoupler and its performance in the circuit was optimized.

The circuit was divided to same functional sections as discussed in section 3.1. The dividing approach supports the study method used thus far and gives detailed information about the error introduced by an individual key location and decreases the amount of software calculation. However the transfer between stages does not show and therefore some additional simulations were conducted to study the effects of coupling between stages.

Most important studies were a transient and DC voltage sweeps. Additionally the simulated effects of component tolerance variations were conducted using the worst-case scenario and sensitivity properties of the Orcad Capture while keeping the input stimulant as constant. Furthermore the DC-imperfections such as offset voltage of the operational amplifiers were estimated using simulation.

A square wave signal with 20kHz frequency, 5V to GND logic states and 50% duty cycle was used to simulate the microprocessor PMW signal in transient studies. The rise and fall times of the pulse were varied according to simulation success with a minimum of 10p seconds to maximum of 100n seconds depending on the successful simulation yield. In DC voltage controlled functionalities the input stimulant sweep was taken with 10-100mV interval. The method was also used in the special study of reference voltage fluctuations.

The effect of temperature fluctuation was simulated using the temperature sweep with maximum ambient temperature of 55°C due to the limitations of some models. Some of the critical models did not allow higher temperature to be used.

### 3.2.4 Simulation Results

In case the result graphs are of poor quality they are also provided as an appendix.

The voltage pull-up response to the input PWM signal suggests the first severe error source in the circuit. We can see from figure 20 that the low level of the comparator is slightly above the logic low and on the other hand the high level reaches logic high.

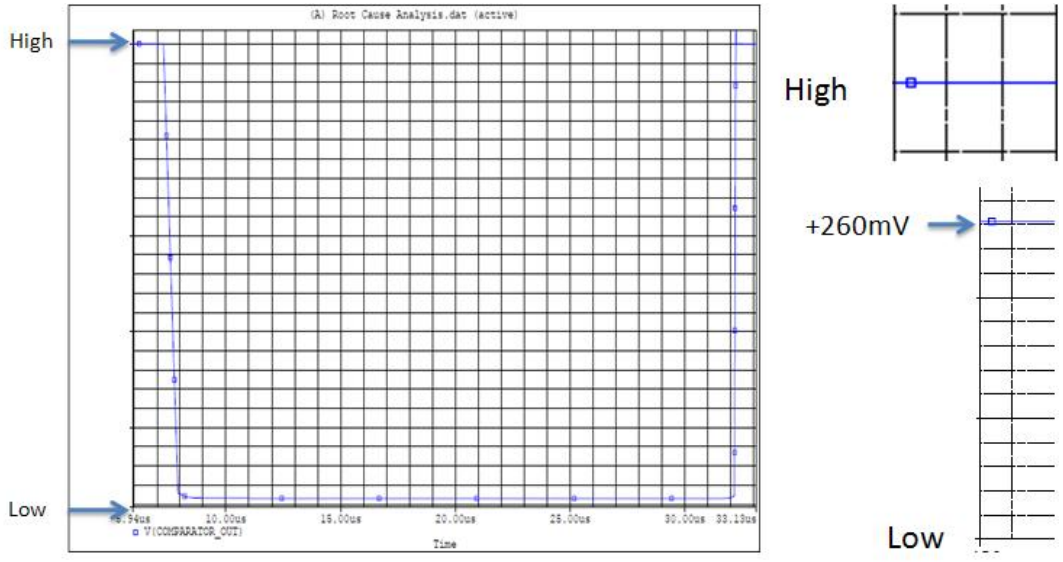



Figure 20 simulated voltage pull-up output

A closer examination indicated that the low level is approximately 260mV above the ideal low-state voltage, which shifts the DC voltage level of the PWM. The figure 20 also indicates asymmetric rise and fall times as the falling edge takes slightly more time to reach its steady state than the rising edge. The additional worst case scenario simulation form the stage in figure below suggests also slightly differing rise and fall times due to component tolerances.

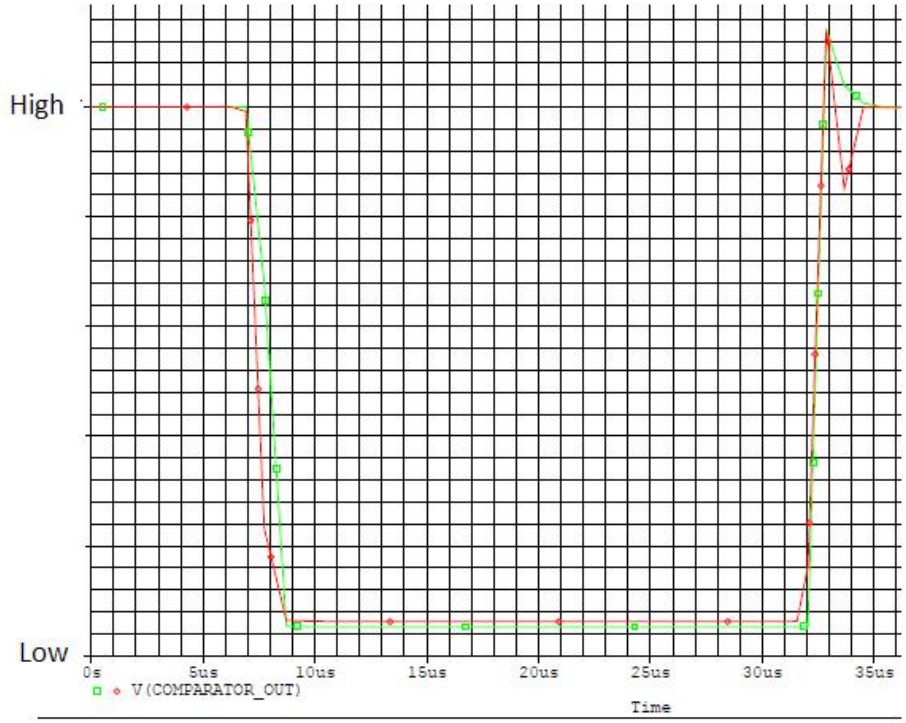



Figure 21 comparator worst case scenario simulation result

The difference was evaluated to between 250ns to 500ns, which will result increase the pulse width with an equivalent of 0,5% to 1% duty cycle pulse, also observe once again the fluctuation in low level steady state.

The comparator stage is also very susceptible to temperature effects. figure 22, which is also provided as appendix 7, indicates that the response of the comparator becomes slower as the temperature increases. The propagation delay from high to low is prolonged more than the delay from low to high as the function of temperature. The comparator stage reference voltage simulation results are given in appendix 8. However, its affects are discussed later in this section.

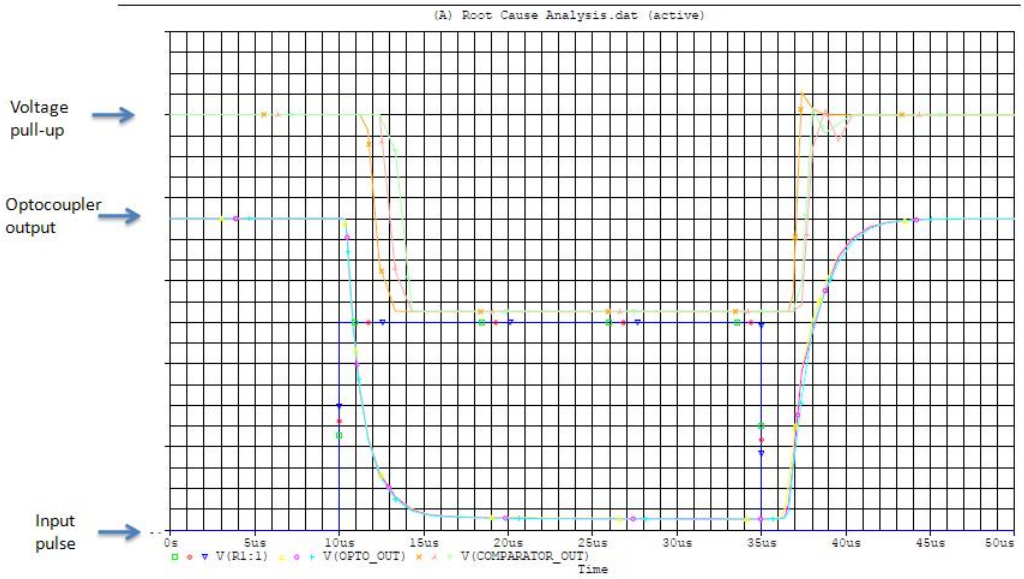



Figure 22 the voltage pull-up stage under temperature variations

The left hand side image in figure 23 shows the steady state voltage of the filter output for simulated voltage pull-up 50% duty cycle PWM and the right side graph illustrates the filter output when its inputs are grounded the blue curve being the differential voltage between input pins and the red curve being the filter output voltage.

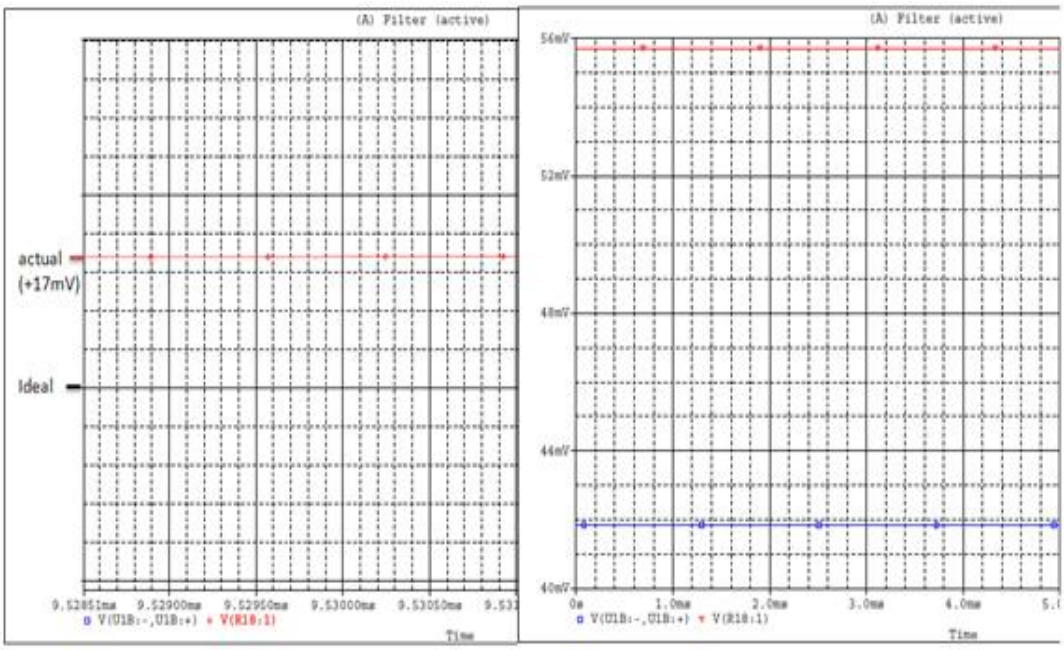



Figure 23 Filter transient offset (left), Filter input differential and output offset voltage(right)

The left side graph shows that after the settling to steady state the filter output voltage is slightly higher than the ideal. When the input of the filter was grounded the differential voltage in the inputs is set to 55mV instead of 0V and additionally the input offset voltage respect to ground was found to be 42mV as illustrated in the right side graph in figure 23.

The output stage characteristic voltage-to-current-transfer curve at pure DC voltage input signal seems initially very linear but when run against equivalent but balanced feedback output stage the current solution exhibits shift further in x-axis as shown in the figure below.

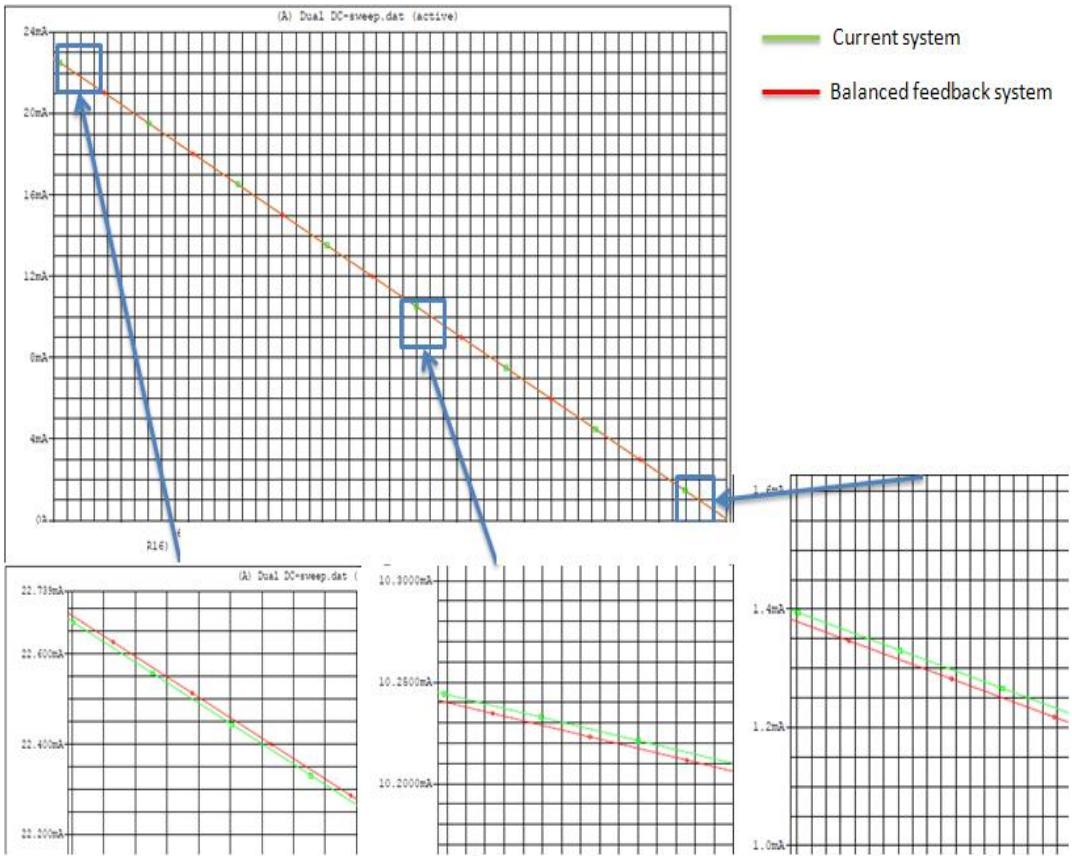



Figure 24 the current output stage versus balanced feedback output stage

Maximum deviation between the curves was estimated as 40µA and besides this an additional output current slope of the current system shown in figure 25 evinces that the output stage is unable to shut down to 0A. The collage is provided as appendix 9.

As we can see from figure below the output stage is unable to shut down to 0mA and a residual current of around 35µA remains in shut down state.

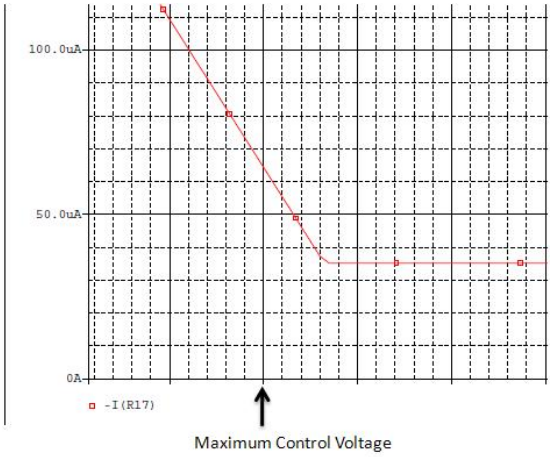



Figure 25 the residual output current

The Monte Carlo unity form runs for the output stage are illustrated in the figure below.

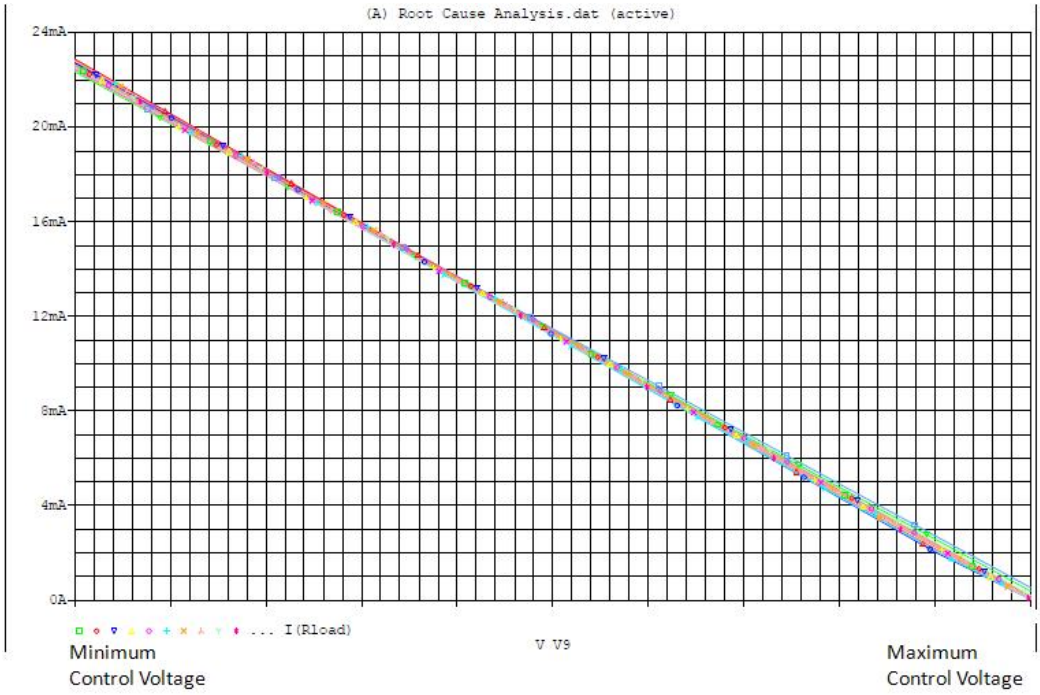



Figure 26 unity form Monte Carlo runs of the output stage

Noticeable deviations in the output stage performance can be seen at opposite ends of the curve while the range between 40-50% of the sweep remains practically unaffected. The maximum deviation is found at input voltage range from 90% to 100%. The figure 26 is also provided in larger scale in appendix 10.

A temperature sweep from 25°C to 100°C for the output stage with 5V input voltage gave a linear slope with a deviation of 4µA between minimum and maximum.

The reference voltage simulation results are provided only as appendices due to the reason that reference voltage study is secondary side study. Nevertheless they strongly demonstrate the importance of a stable accurate voltage reference. The left upper corner image of the appendix 8 from the voltage pull-up falling edges suggests that at 9,4V and beyond the response is delayed more than on the other values which seem to have identical fall-times also we can see that for each rising edge the slopes manifest different rise-times. The lower left hand corner shows that the overall DC level of the pulse is immediately affected if the reference voltage is altered. The simulated evaluation of unstable reference voltage is given in appendix 11. The output current error voltage to current conversion ratio was calculated by using the software minimum and maximum finding properties which yielded

$$k = \frac{\Delta y}{\Delta x} = \frac{(\Delta I_{out})mA}{(\Delta V_{reference})V} \approx 4{,}53\frac{mA}{V} \tag{16}$$

The gradient k causes a full-scale error in current as described below

$$Full - scale\,error - \%(V_{reference}) = \frac{(\Delta I_{out})mA}{20mA} \times 100\% = \frac{k\Delta V_{reference}}{20mA} \times 100\% \tag{17}$$

In example, an error of 10mV in reference voltage causes full-scale error of

$$Full - scale\,error - \%(10mV) = \frac{4{,}53\frac{mA}{V} \times 10mV}{20mA} \times 100\% \approx 0{,}2\%$$

The equation assumes the input voltage ideal and the error is caused by inaccurate reference voltage alone, furthermore as the control voltage is differential the equation (17) can be used to evaluate input DC voltage error effects to full-scale error as well.

### 3.2.5 Comments and Conclusions about the Simulations

The simulation results seemed to prove throughout the simulation process that the most noticeable sources of error component wise are located around the comparator and output circuit. The operational amplifier DC imperfections seem to have moderate impacts to the DC level that are worthwhile to take in to consideration. Even though these errors seem insignificant at first glance the cumulative error can reach formidable proportions.

The input and output voltage dividers have moderate effect and the output voltage divider in particular. The error caused by the input voltage divider was calculated to be a +/-1% and the output voltage pull-up resistors cause +/-1,8% worst case scenario PWM pulse width discrepancy. The input resistor accuracy is for naught however if the optocoupler properties which for most part determine the rising and falling edge characteristics of the device such as CTR or $R_B$ are not under control.

From the simulation point of view the comparator device is the most noticeable source of error as it clearly alters the PWM DC voltage level and seems to slightly distort the duty cycle. This result was anticipated since the theory was already introduced in section 3.1 so the simulations further support the theory. The final verification of this error will be in the laboratory experiment but the evidence is already rather solid.

Even though the filter circuit seems docile and only calculates the average value of the signal that it is given, the filter operational amplifier possesses a possible small error source in the form of the offset error as seen in the figure 23. The offset voltage in the transient analysis was less severe than the static analysis of both inputs grounded. This suggests that the operational amplifier has some trouble reaching the ground when the input is also grounded. Nevertheless 18mV to 56mV error will be definitely

seen in the output current as the output system voltage to current gain ratio given in equation (16) is very sensitive.
The offset voltage error holds true in the output stage as well and in this application the voltage can be particularly hazardous because the output stage is DC voltage driven. Additionally the input offset voltage is a +/- differential voltage which means the output stage control voltage error may be additive or subtractive to the true control signal so that the output current is slightly low or high respectively.

The output stage Monte Carlo runs imply that the output stage component tolerances have indeed a strong effect to the output current accuracy. The current transfer curve in figure 26 manifests the strongest variation in output current at the high end of the control voltage which translates to low duty cycle PWM input signal, in addition the high duty cycle portion of the output current curve varies also moderately. The curve seems to have almost as a pivot point at around 35% of which around the current curve balances between so that the current will be below nominal on one end and above on another. In any case the error can be drastic in the low duty cycle end and a modest visual estimation is around 500µA while the output should be 0mA.

The behaviour of the component tolerances in conjunction with the residual current in the shut down state, shown in figure 25, support the output inability to shut itself off. The operational amplifier and the single sided power supply are most likely the main reasons and the component tolerances further increase the residual output current. The testing of the bipolar supply voltage was conducted in the prototype design simulations out of personal interest and the results are discussed in section 4.1.3.

An accurate and stable reference voltage is one of the evident keys to a precise output as it defines the most important voltage levels in the circuit as seen from appendices 8 and 11. The output stage reference voltage is more fragile in nature than the voltage pull-up because it is the other from two control voltages that immediately change the result of the conversion and as we can conclude from the obtained relationship to the full-scale error in equation (17) as a millivolt scale voltage already greatly affects the output accuracy.

## 3.3 Laboratory Measurements

### 3.3.1 Introduction to the Laboratory Environments

The Metropolia University of Applied Sciences electronics laboratory at Albertinkatu was a modest laboratory with basic equipment. The laboratory tables were ESD protected and had a built-in fuse protected power supplies, in addition each table had one transformer coupled power outlet for oscilloscope use. The laboratory had also several soldering stations if any board modifications are needed.

The ABB electronics laboratory at the Helsinki electronics factory that was used to conduct the most of the analogue output studies is one of the several laboratories at the site. This particular facility was dedicated for control electronics study and research. The laboratory tables had similar options as in Metropolia laboratory albeit the oscilloscope had to be isolated using an external coupling transformer. The ABB laboratory also provided an environment chamber, which could be used to simulate different operation conditions or to age the DUT in purpose. The laboratory also provided soldering and desoldering stations in case any modifications or component replacements were required.

### 3.3.2 Measuring equipment and setup

The measurements were conducted using the equipment indicated in the table below.

Table 2 the measuring equipment

| Experiment: | Power supply: | Signal generator: | Oscilloscope: | Multimeter: |
|---|---|---|---|---|
| Initial | Hameg HM7042 | Hewlett Packard 8116A | Hameg | Fluke 175 |
| | | | | |
| Main | Tti302RT | Hewlett Packard 8116A | Tektronix DPO4340 digital | Fluke 175 |
| | | Wavetek 100MHz model 395 | | |

The initial measurements labelled in table 2 were conducted at Metropolia University of Applied Sciences electronics laboratory as a comprehensive functionality study and the main measurements at ABB electronics laboratory as the conditions there were more suitable.

The basic measurement setup is illustrated in figure 27, however additional more stage specific measurements were also conducted to the analogue output circuit and the setup was altered accordingly. The modifications are discussed in more detail at corresponding experiment topic.

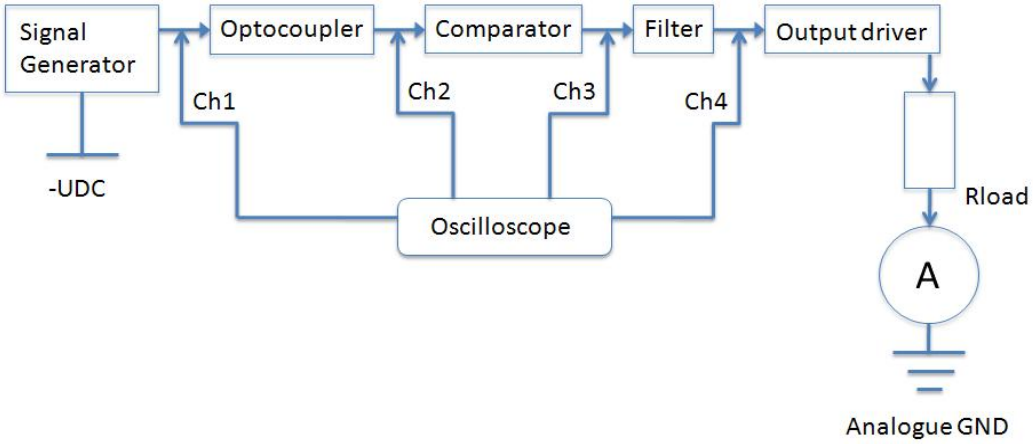



Figure 27 the Basic measuring setup

The oscilloscope probe Ch1 was grounded to –UDC and the Ch2 thru Ch4 to analogue ground and the oscilloscope itself was isolated from the main grid using an isolation transformer. The signal generator was generally set to provide a 0-5V square wave signal that emulated a microcontroller PWM-signal and the pulse width was kept constant or altered depending on the measurement.

The output load, which was formed from two 1kΩ wire wound resistors with 1% tolerance and 1/8W power rating connected in parallel, was kept constant throughout the laboratory experiments.

The numerical results were documented manually using Excel and the visual images were collected using the screenshot feature of the Tektronix oscilloscope, furthermore

the oscilloscope was used to perform mathematical calculation such as FFT and signal averaging.

### 3.3.3 Initial Output Current Error Measurement

The output current error measurement was part of the comprehensive measurements at Metropolia facilities. The current error data however is the only data considered comparable with the main measurements. The measurement was carried out using the basic measurement setup given in figure 27. The signal generator was used to create a microcontroller emulating PWM and a 10%-90% duty cycle sweep with steps of 10% was carried out. The output current values were collected to an excel file and error calculations were performed and the data placed in to a graph.

### 3.3.4 Linearity Measurement

The basic measurement setup was employed to measure the PWM duty cycle transfer in the isolation and voltage pull-up stage. The linearity measurement was performed twice using a microcontroller PWM emulating signal with controllable pulse width was used as the input signal for the AO1 circuit.

In the first phase the pulse was inserted to the MOSFET driver and the output pulse widths were measured at the output of the optocoupler using a 19,4% threshold voltage and at the output of the voltage pull-up with 50% threshold as reference points in the oscilloscope which performed the calculations. Threshold for referencing was determined by calculating the comparator threshold voltage and comparing it to the high level seen by the positive input of the comparator.

In the second phase only the optocoupler output pulse was evaluated using 18,2% and 19,7%. The 19,7% referencing measurement was done after the initial experiments due to personal interest as a comparison to the actual measurement results because the first impression implied that the low duty cycle error decreased as the threshold voltage increased. However the first impression proved wrong in as the measurement progressed and only few data points were therefore collected.

The measuring results were documented to a spreadsheet every step of 2% in both measurements, however visual material was taken using the oscilloscope screenshot feature only while examining both the optocoupler and the comparator.

### 3.3.5 Thermal Behaviour Measurement

The measuring equipment configuration was rearranged on to a movable cart and the control board was modified with long signal measuring and power cables. The board was placed in to the climate cabinet the cables were brought outside through a cable via and were finally connected according to the basic measuring setup illustrated in figure 27.

The cables were secured and the cable via was further sealed by additional duct tape blockage. The AO1 input was stimulated with microcontroller PWM emulating signal with controllable pulse width and the output current response was measured every 10% step, furthermore the optocoupler and comparator pulse behaviours and filter output voltage were observed and recorded. Similarly as previous measurements the possibility of screenshots was employed to capture visual material to aid the interpretation of the numeric results.

The measurements were conducted in three different temperatures of 25°C, 50°C and 75°C. After the desired temperature was reached the board was allowed to warm up for 15 minutes prior to the start of the measurement sweep. The moisture of the cabinet was set to minimum, which translates to the laboratory ambient moisture. However, the climate cabinet showed variable response to moisture settings in different temperatures and the effect of moisture remains slightly unclear but is considered as the ambient laboratory humidity.

### 3.3.6 DC voltage and PWM-Stimulant to Filter Measurement

The AO-1 circuit was modified by isolating the voltage pull-up from the rest of the remaining circuitry before the filter circuit by removing the voltage-pull up resistors R708

and R709. The final measurements were done using the configuration described in figure 28.

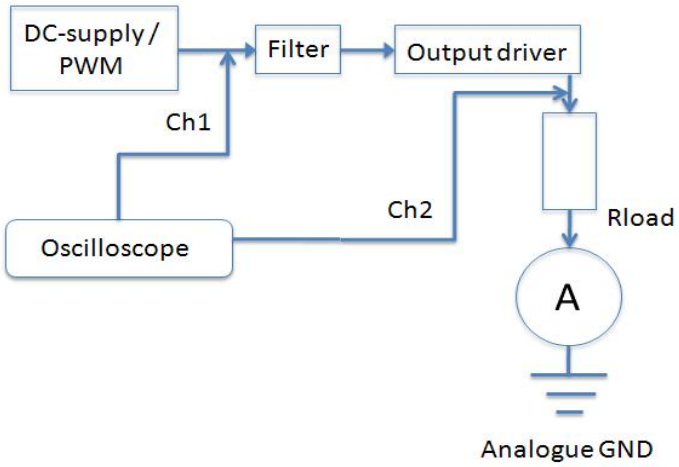



Figure 28 DC voltage input measurement configuration

The input DC voltage sweep and output voltage were carefully monitored using the oscilloscope and the output current and voltage were documented every step of 100mV input voltage. The circuit was also stimulated with a microprocessor emulating PWM by replacing the DC power supply with the signal generator. Due to the nature of the measurement no visual material was collected.

### 3.3.7 Effect of PWM-Frequency Measurement

The effects of the PWM frequency to the output current and to the linearity of the system performance were measured using the standard measuring configuration shown in figure 27. Full range 0-98% duty cycle sweeps were carried out using 10kHz and 5kHz frequencies. No visual data was recorded.

### 3.3.8 Laboratory Measurement Results

The initial laboratory work is in line with the reports from the production and the preliminary work done by the ABB design engineer. The output current error data was

obtained by subtracting the calculated ideal current defined by equation (2) from the measured output current values. Equation (2) is revised on the following page.

$$I_{out} = \frac{10}{47^2}\left(10 - \left(5 - \frac{5t_{on}}{T}\right)\right) = kD$$

In which k=constant, D=input signal duty cycle

The acquired output current error data is given in the figure below.

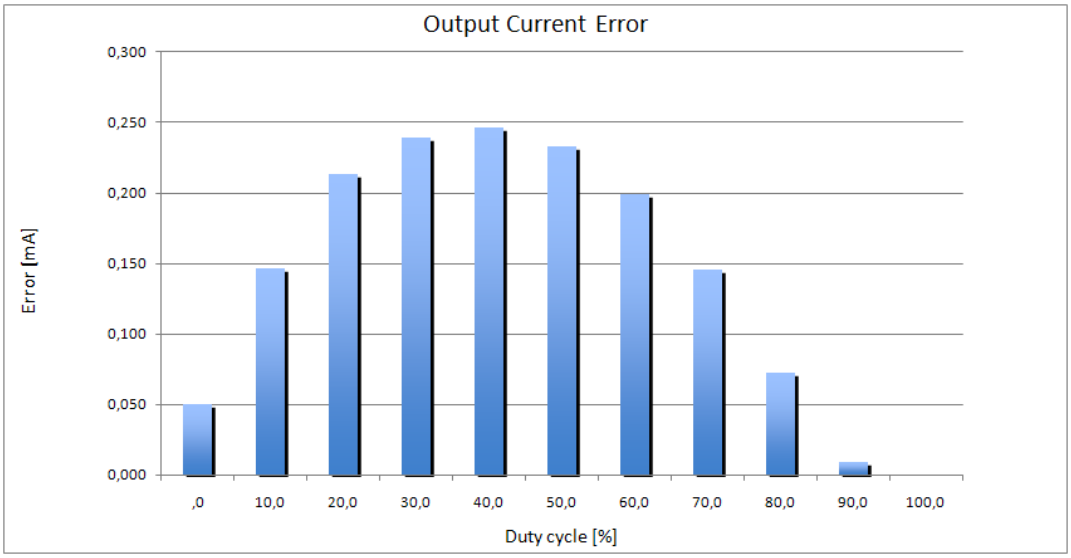



Figure 29 Initial measurement output current error

We can see from the graph that the AO-1 exhibits the worst current error when the duty cycle is around half way and the maximum error of 0,246mA occurs at 40% duty cycle and the minimum of 0,147mA at 10%, while 100% error is unavailable.

The first linearity measurement results shown in figure 30 indicated two opposite behaviours in error patterns. The optocoupler exhibits maximum difference of 0,352% at low pulse width and the minimum at around 80%, while on the other hand the voltage comparator does the opposite as the voltage pull-up error is at the maximum difference of 0,620% at 98% duty cycle. In addition the optocoupler PWD is relatively constant after around 10%, whereas the voltage pull-up discrepancy increases strongly after 50%.

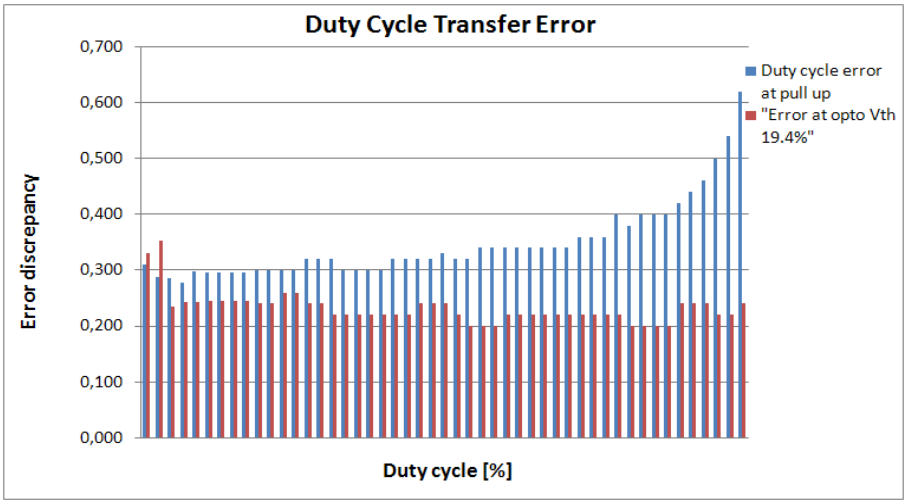



Figure 30 Duty cycle transfer error measurement 1

The second measurement results of the PWD exhibited by the optocoupler shown in figure 31 indicate that the pulse width seen by the comparator with 18,2% threshold voltage is less than the original PWM signal at low duty cycles until around 40% and more than the input PWM when the duty cycle is between 70 – 90%.

The pulse width distortion changes polarity once more at around 90% duty cycle. The maximum difference is consistently found at the beginning of the sweep.

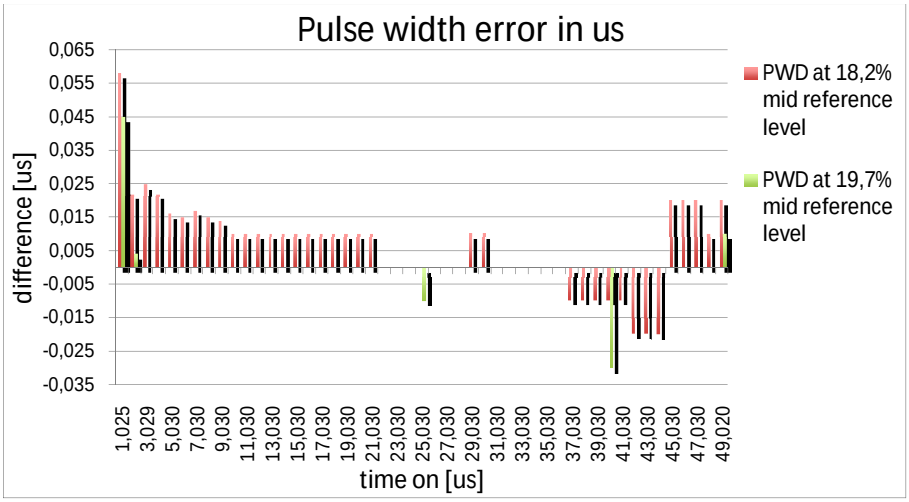



Figure 31 Optocoupler pulse width distortion at 18,2% and 19,7% thresholds

The 19,7% threshold measurement was done for comparison for the 18,2% measurement and the results are included in figure 31. We can witness once again similar turning in the duty cycle. However, as the reference is increased the turning points occur earlier.

The thermal measurement error current data was extracted from the collected values by subtracting the calculated current from the measured one as before and the error data was plotted in a column graph illustrated in figure 32.

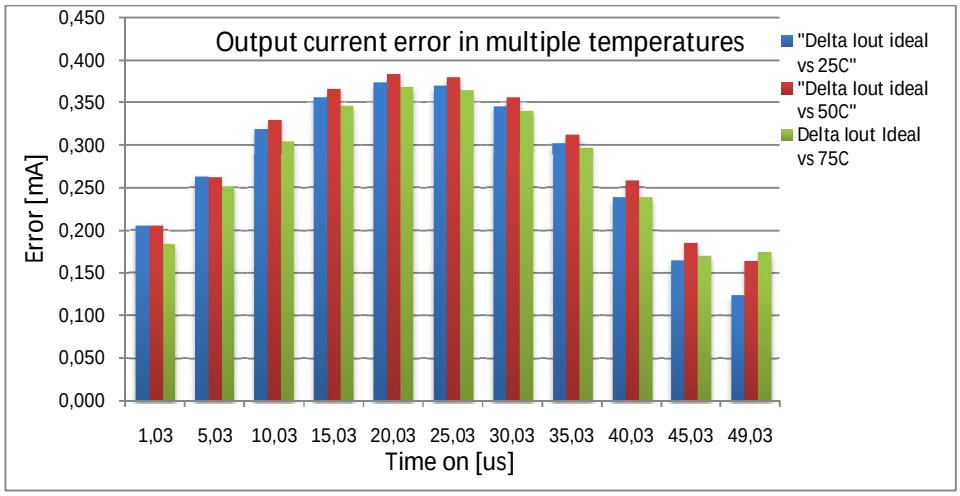



Figure 32 output current error in various test temperatures

The maximum error at 25°C of 0,373mA occurs at duty cycle of 40% and the minimum error of 0,124mA can be seen at 98%. Increase of 25°C from initial temperature of 25°C to 50°C increased the output current error slightly starting noticeably at 20% duty cycle. We can also see that the error is more emphasized at higher pulse widths around 80% onwards. At 50°C the maximum error of 0,383mA was found at 40% duty cycle and the minimum of 0,164mA at 98%. The biggest increase in error was found to be at high duty cycles past 70%.

The final measuring temperature of 75°C showed reversed behaviour in error. The measured error data plunged below the data measured at 25°C with an exception of duty cycles of 90% and beyond which remained higher or continued to increase.

The maximum error of 0,368mA occurs at once again at 40% duty cycle, however, the minimum error of 0,170mA was found at 90%.

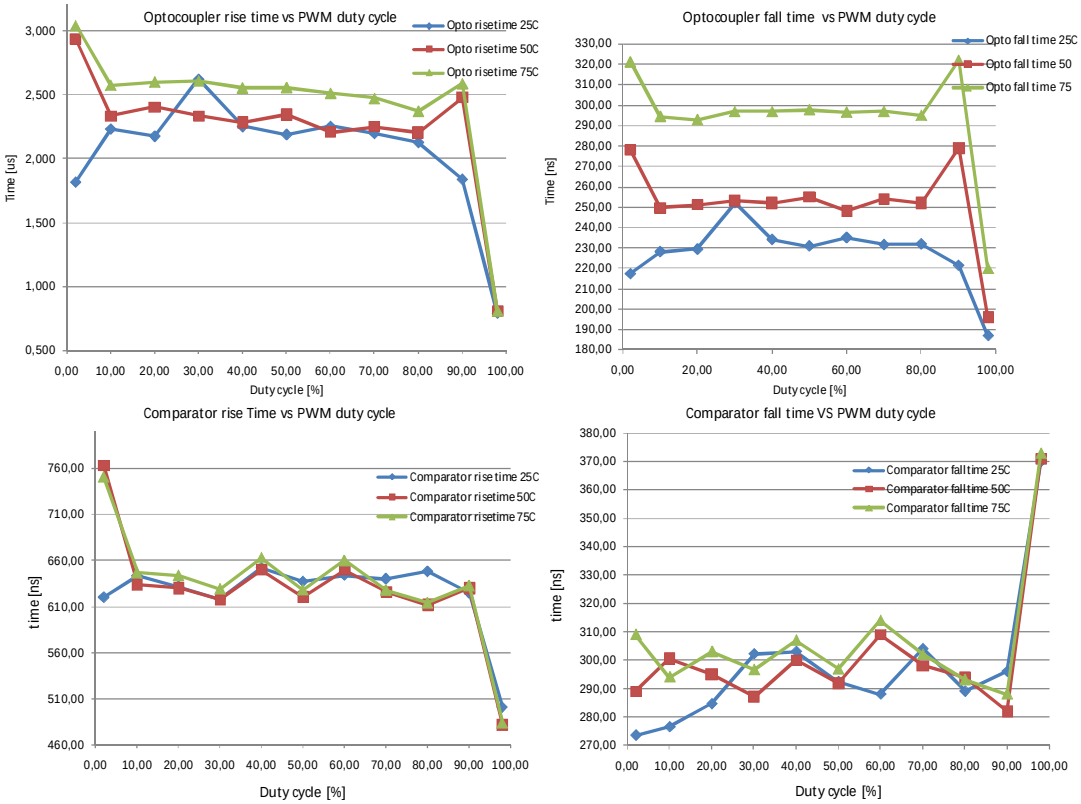



Figure 33 optocoupler and the comparator pulse width behaviour in test temperatures

The collected pulse width behaviour data from the thermal measurements is plotted in figure 33, which is also provided in appendix 12. The optocoupler exhibits nearly constant rise and fall times at duty cycles between 10-80%, however the low and high ends have an increase in both of the variables at temperatures of 50°C and 75°C, furthermore the fall time takes a plunge at maximum measured point of 98% in all measured temperatures.

The maximum values can be seen at the opposite ends of the duty cycle sweep besides at temperature of 25°C, which exhibits the maximum value at 40%. The optocoupler rise and fall times show a global trend of rise with the temperature. The comparator rise time behaves similarly as the optocoupler rise time, however the fall time

results are very different. The fall time varies a lot throughout the pulse width sweep and at the high end it soars to high maximum.

The output current error in the DC-input measurement was acquired same way as in the previous output current error measurements. The first error curve “Error1” data was extracted by subtracting the calculated current from the measured results. Measuring the output voltage across the output resistor and determining the output current using the Ohm’s law and finally subtracting the ideal current from it obtained the second error curve “Error2”.

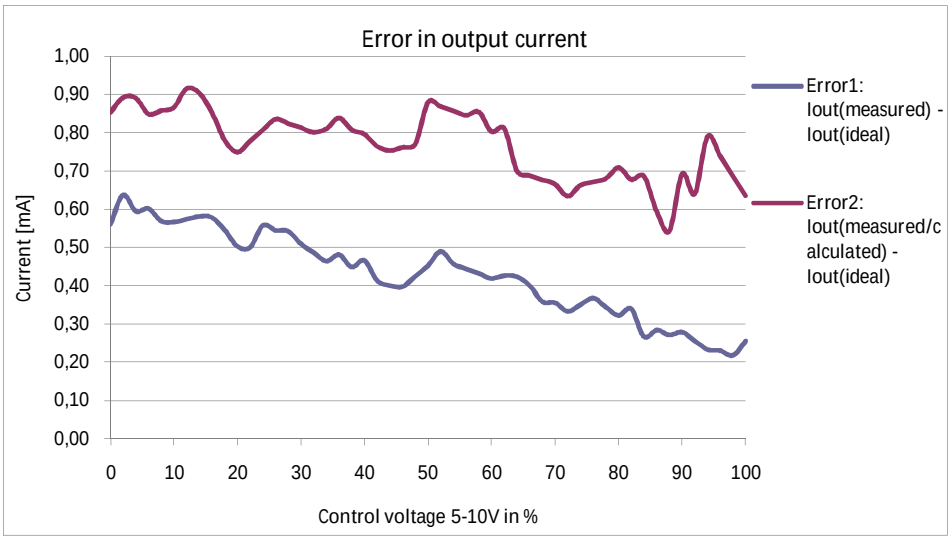



Figure 34 Error in output current with DC voltage stimulant

In figure 34 the error slope 1 trend shows that as the control voltage increases the error in the output current approximately linearly decreases. An increase in control voltage transcribes as decrease in PWM duty cycle, therefore we can say that the according to the measurement the output current error is somewhat inversely proportional to the PWM duty cycle. The error slope 2 shows similar behaviour as the error slope 1 but the magnitude of the error is significantly higher than that of the counterpart. Still, although the behaviour is similar the fluctuations show much more non-linear connection with the control voltage magnitude.

A direct PWM stimulant followed the DC voltage input measurement. The error data was obtained similarly as in the previous experiment and it is shown in figure 35 as a plot of function generator input signal PWM duty cycle.

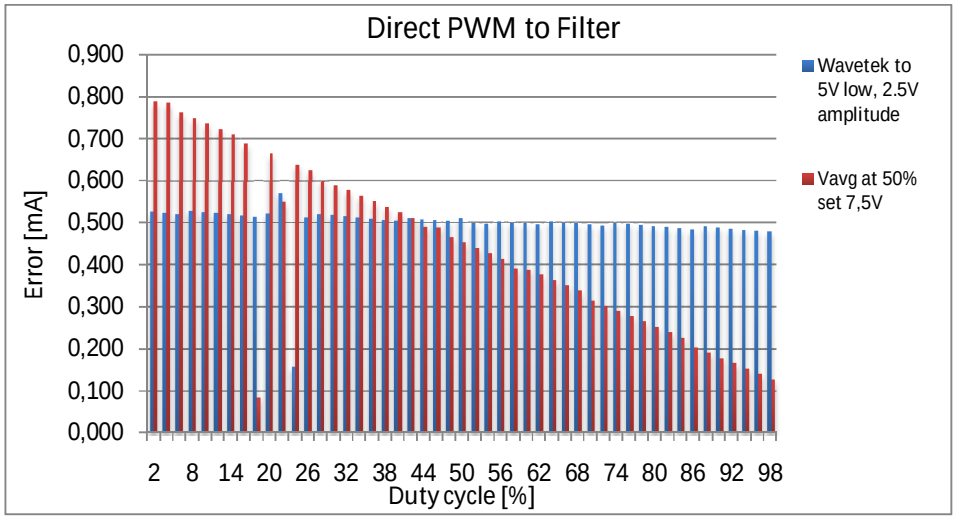



Figure 35 Output current error with direct PWM stimulant to the filter

The first measurement data marked with blue columns indicates an almost constant error but closer examination shows a slow decrease with input pulse duty cycle. To interpret the results correctly it must observed that the input duty cycle seen here is not corresponding to the PWM sent by the microcontroller but the inverse of it. In other words, from the AO1 input point of view as the error increases proportionally to the duty cycle.

The second measurement with the PWM average value set to 50% is marked with red columns in the figure 14 and it shows that the error increases approximately linearly with the AO1 input PWM duty cycle. The maximum error can be found at the high duty cycle and the minimum at the opposite low side.

The output current error in the frequency study was calculated as in preceding error in current laboratory experiments by using the output current values recorded in both 5kHz and 10kHz sweeps and subtracting the calculated current from it. The output current error was plotted in to a column graph illustrated in figure 36.

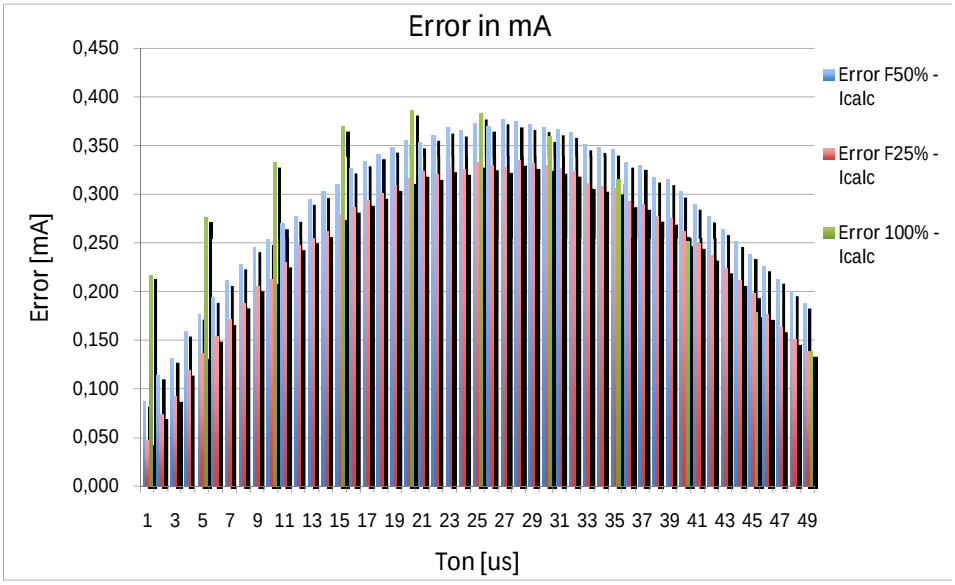



Figure 36 output current error with different PWM frequencies

It can be seen from the figure above that the error is decreased throughout the duty cycle sweep as the frequency is lowered. The maximum error of 0,383mA at 20kHz can be found at 40%, at 10kHz when duty cycle is 54% with 0,377mA magnitude and at final value of 5kHz the maximum error of 0,335mA has shifted position to 56%. The maximum drop in error between 10kHz and 5kHz of 50uA can be seen at the very high beginning at 88% and upwards and also at 50%.

### 3.3.9 Photographic Evidence

Visual data was collected from most of the measurements to aid and support the pin pointing of error locations by examining possible PWM distortion after certain stages.

The main interest was initially placed on the optocoupler as its performance was unknown from the simulations in addition the comparator output was placed under high priority as the simulations suggested that it is a potential root cause error.

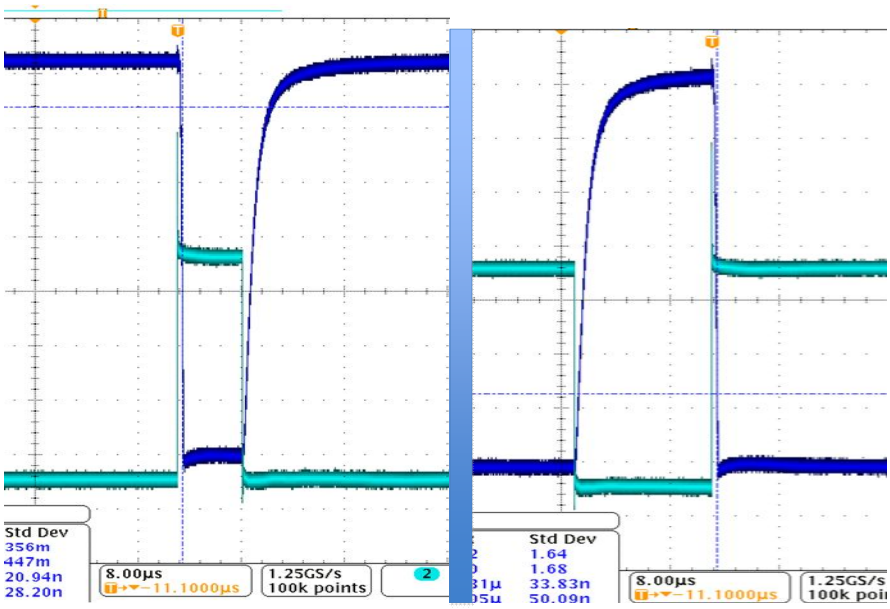



Figure 37 Optocoupler output versus input pulse at 10% and 80% duty cycles

figure 37 shows the optocoupler response to input PWM. The asymmetry yet small one with this scaling between propagation delays can be estimated from the image and careful study seems to indicate that the $t_{pHL}$ would be slightly slower than the $t_{pLH}$.

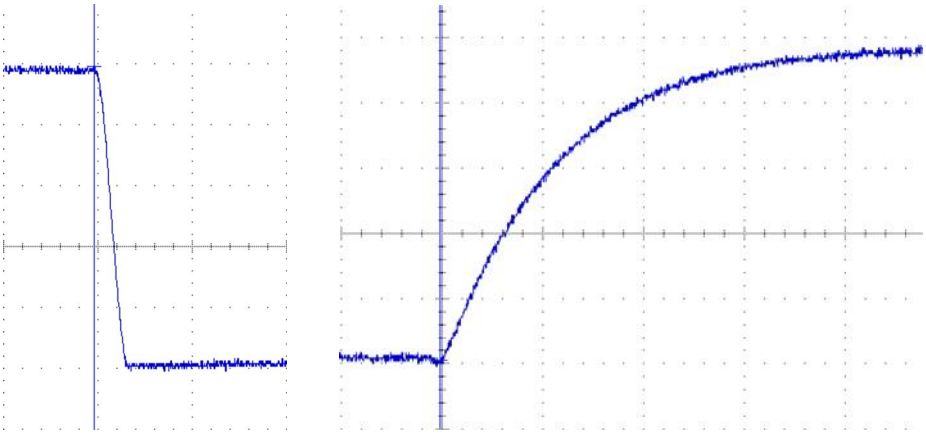


Figure 38 comparator output edges

A close-up taken from the comparator output pulse edges shown above indicates the asymmetric operation due to the comparator device topology. As the comparator is open collector the falling edge is actively pulled down while the rising edge is passively pulled up causing asymmetry to the response.

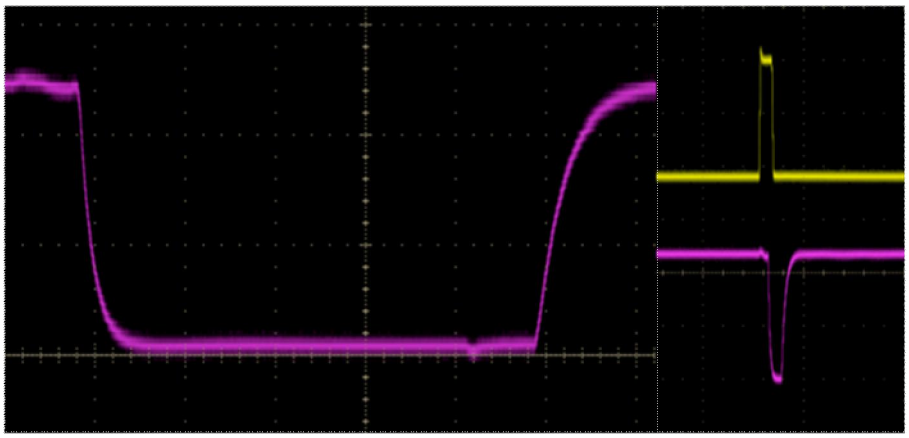


Figure 39 the PWM waveform at voltage pull-up

The voltage pull-up response is shown in figure 39. The purple curve of voltage pull-up waveform shows that the voltage pull-up seems to have even more trouble than the comparator in replicating the actual PWM curve in yellow sent by the function generator.

The Fast Fourier Transformation for pulses of 40% and 10% duty cycle in figure 40 indicates that the DC voltage values are higher than they should by the design parameters.

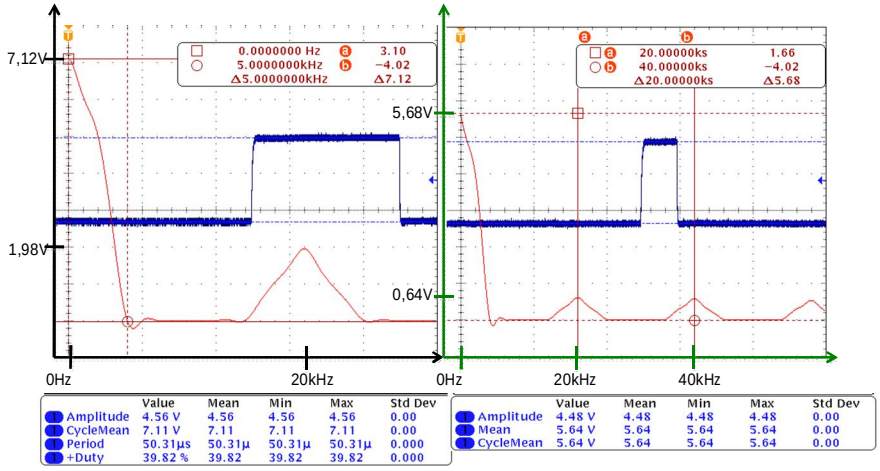



Figure 40 FFT of 40% and 10% duty cycle pulses

The oscilloscope software calculations indicate a 39,82% duty cycle to a corresponding input PWM duty cycle of 40% signal, furthermore the FFT DC-voltage value and the cycle mean calculated by the software show an additional discrepancy. The software calculations with FFT and with average calculation showed 7,12VDC and 7,11VDC respectively. The 10% duty cycle measurement indicated similar behaviour. The DC voltage values calculated by the software are 5,68V for FFT and 5,64V for averaging and later on when the software was made to measure the duty cycle it was found reduced from 10% to 9,739%.

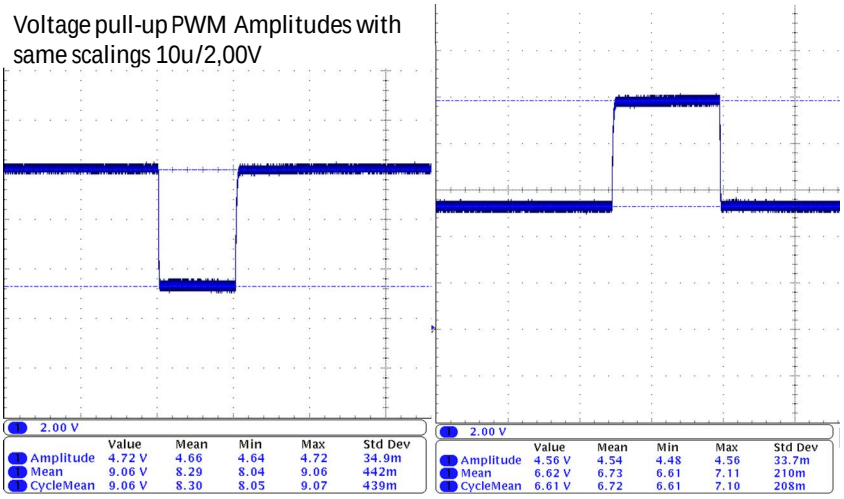



Figure 41 the DC voltage error at voltage pull-up

figure 41 shows how the amplitude of the PWM signal at the voltage pull-up was varying from 4,54V to 4,66V depending on the pulse width. The correct value for the before mentioned values is 5,0V.

### 3.3.10 Comments and Conclusions about the Laboratory Measurement Results and Graphical Evidences

The initial, thermal and DC voltage input measurements were conducted on different boards. This can be seen as quite well as the output current error varies somewhat between the measurements. There is always the possibility of error in measurement caused by the measurement method, time, place or the operator, but in this case the possibility of heavy tolerance fluctuation between units is a good question.

In any case the error pattern is clear. The maximum error magnitude appears around half way of the duty cycle sweep and the entire error forms a downward opening parabola like pattern.

Lowering the frequency of the PWM reduced the error somewhat and unfortunately the original output error data in which the lowering effect was compared against was measured from another board which proved to be poor choice to save time. However considering the target at hand the most important area in which the accuracy must be improved is located at the middle portion of the sweep. A careful estimate from the efficiency of this method to improve the accuracy can be made by comparing the maximum accuracy improvement gained in the middle portion between the 20kHz and 5kHz. The maximum full-scale error improvement can be found as

$$Full-scale\,error-\% = \frac{(0{,}383-0{,}335)mA}{20mA}\times 100\% \approx 0{,}2\%$$

We can see that lowering the PWM frequency does not alone provide sufficient improvement, however it could be used to compensate the temperature fluctuation caused error.

Nevertheless, the comparison shows that the error maximum and the overall plot may shift in the x-axis between boards quite a lot which must be a result of at least optocoupler and possibly also comparator tolerance variations.

The DC voltage and PWM inputs to the filter measurements were very susceptible to the success in setting the input signals correctly as the resulted slope steepness varied significantly between experiments. When the isolation circuit was removed from the system the shape of the plotted error formed a decreasing slope in respect to decreasing duty cycle as seen in figure 34. It is suspected that the error is due to filter and output stage DC voltage imperfections, furthermore the accuracy of the reference voltage and the imbalanced output stage feedback network is under suspicion. The conclusion is that the overall error trend seems moderately consistent error caused by aforementioned factors and the slope is slightly altered due to operator error.

The PWM error and thermal measurements further indicate that the optocoupler and the comparator have difficulties in replicating the original PWM signal at high and low duty cycle values which could be the result of the slightly low bandwidth of the optocoupler for the application, in addition it seems that the optocoupler asymmetric rise and fall time characteristics are further imbalanced in higher temperatures as seen in figure 33. If the optocoupler is to be used in future solutions, it is advisable that its temperature behaviour is taken into account.

The comparator reshaping of the input signal to a square wave pulses was found to be inefficient because this time the rise and fall times of the comparator are asymmetric as seen from the figure 33 and the shape of the output waveform is unacceptable replica of the original PWM signal as shown in figure 39. It seems that the comparator in conjunction with the optocoupler, as concluded earlier, both affect the parabola shape of the error pattern as their edge performance is asymmetric, which is emphasized at high and low duty cycles as there the time to recover from the transient is the shortest.

The graphical evidence proves what was already expected and initially discovered in section 3.1 that the low level of the comparator will not reach 0V as the design requires. It is obvious that if the true expected output for the filter is 5,49V and the oscilloscope readout calculation indicates 5,68V there is something terribly wrong.

Evaluating the average value for a 39,82% and 9,739% yields in ideal case

$$V_{Average}(39{,}82\%) = (0{,}3982 + 1)5V = 6{,}99V$$
$$V_{Average}(9{,}739\%) = (0{,}09739 + 1)5V = 5{,}49V$$

Comparing the figures to the ones obtained from the measurements using FFT of 7,12V and 5,68V gives a discrepancy of 130mV and 190mV. From additional collected data but not presented here for around 90% and 70% duty cycles the same figures were evaluated as 140mV and 120mV respectively. This proves that there is a DC-level shift in the PWM average value at this point of the circuit.

#### 3.3.11 Comparisons with the Simulations

The comparator and voltage pull-up stage simulations showed similar behaviour as the laboratory experiment revealed, however in smaller proportions. The true operation of the comparator and voltage pull-up stage were found to be in far more grave condition than the simulations initially suggested. Nevertheless the simulations gave a good direction from where to search for causes of error.

The filter simulations suggested a DC voltage offset error which could somewhat explain the increased output current. This in conjunction with the output stage operational amplifier offset error could be part of the reason why the output error indicated the steadily decreasing slope. Also the Monte Carlo runs imply that the output stage is vulnerable to component tolerances, furthermore if the reference voltage is not spot on 10V the output current will be affected immediately.

#### 3.3.12 Diagnosis

The overall diagnosis suggests that there is a constant DC voltage offset error in the circuitry after the voltage pull-up which is explained by the DC-input and the direct PWM insert measurements to the filter. This constant offset is compensated by the PWD introduced by the optocoupler and the comparator stage's inability to handle the PWM at low and high duty cycles and also the comparator stage's voltage pull-up DC-level shift.

# 4 Corrective Actions and Implementations

## 4.1 Prototype Design

### 4.1.1 Corrective Solutions

As a revision from section 1.4.3 the boundary design parameters for the corrective solutions were cost efficiency, circuit board space and availability of components.

The main selected error sources to correct were the DC offset error introduced by the operational amplifier and the imbalanced output stage, the comparator DC voltage level error and the PWD caused by the optocoupler and the comparator.

From a handful of possible solutions a group of three were selected to be implemented in a hardware prototype. The control signal topologies selected for the systems were the already familiar PWM duty cycle and a new approach using the PWM frequency. The topology of averaging a pulse train and transforming the obtained voltage to current was maintained for all solutions and the main focus was placed on improving the PWM integrity before averaging.

The first selected design approach was based on fine tuning and correcting the key error sources in the current output system with affordable simple components, which would guarantee easy sourcing and product development lead time. However the system was expected to pay a small price in accuracy for cutting corners on the optocoupler selection as the small bandwidth of the current device would somewhat introduce PWD to the system. The key locations to fine tune were the optocoupler forward current, the comparator load and the output stage feedback network.

As the input current was found to be earlier in section 2.2.2 around 12mA and the datasheet of the device suggests 16mA would reach good results in achieving symmetry for the propagation delays the forward current was increased to 16mA.

A second fine tuning area, the comparator load, was too large for fast operation. The load was decreased to 10% of the previous load to improve the rising edge performance. Finally the output stage feedback network was balanced for both inputs and redimensioned to suit the output current range.

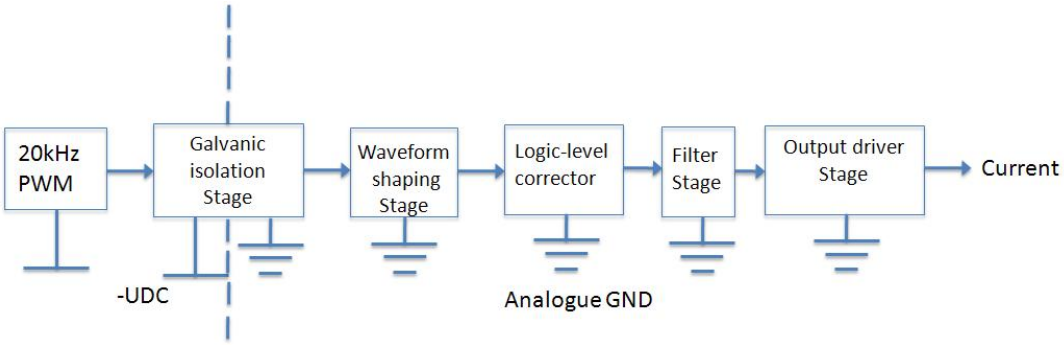



Figure 42 block diagram of solution 1

The new functionality introduced to the solution 1 shown in the system block diagram in figure 42 was a DC-level corrector of which purpose was to more accurately define the logic levels of the voltage pull-up in the waveform shaping stage. This stage would correct the DC voltage accuracy seen by the filter.

The second solution was built around a more advanced optocoupler with active output operation and its block diagram is given in figure below.

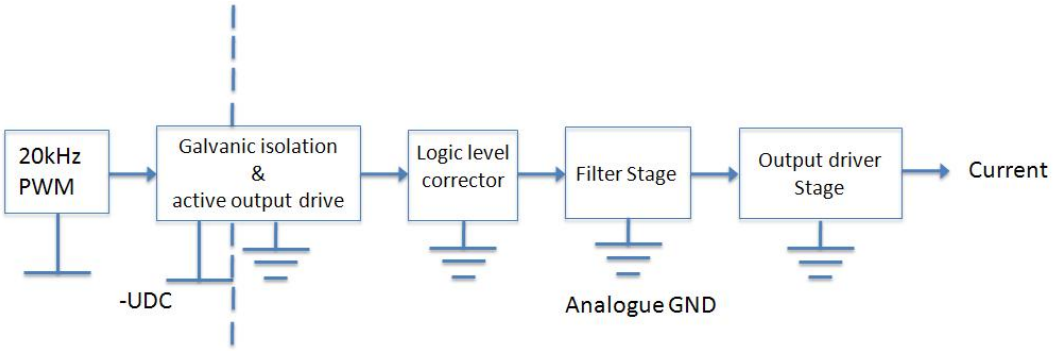



Figure 43 second solution block diagram

The new optocoupler would in conjunction with the aforementioned DC-level corrector, waveform shaping and the DC-level corrector stage to one compact hardware implementation thus reducing board space. The new device is more expensive than current device but its use is justified by superior performance in transferring the PWM duty cycle through the isolation and the saved board space. A second source availability for the optocoupler is yet to be confirmed.

The final solution is built upon the idea of transforming PWM signal edge frequency to pulses. From the solution block diagram given in figure 44 we can see that the system performance is more independent of the optocoupler operation as the pulse encoding from the frequency is carried out after the isolation. The frequency to pulse converter block incorporates the waveform shaping and voltage pull-up stage which makes the system highly integrated and small in size which we will conclude in section 4.1.2.

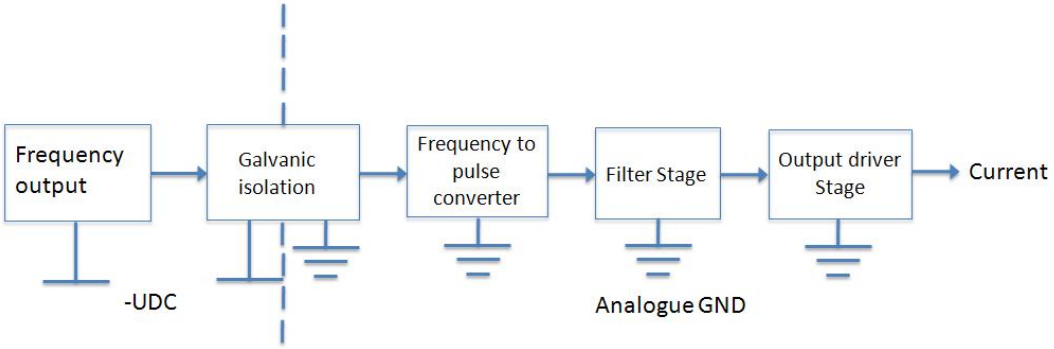



Figure 44 the frequency to current solution

The solution components are widely available and cheap but the expected performance is unknown. A limiting drawback is the fact that the control board microcontroller PWM output or other designated output must be flexible enough to provide sufficiently accurate control over the output signal frequency and it must be precise enough.

### 4.1.2 The Corrective Technology Solutions

The output stage schematic of solution 1 is given in figure 45. The feedback network was balanced by adding a feedback resistor R38 equal to R39 and the collector resistor was omitted as irrelevant for the system performance.

The feedback diode V7 and the re-dimensioned current limiting resistor R36 adjust the operating conditions of the output the transistor so that it is driven with more current while the diode prevents the base from saturation and aids it to recover quickly from base charge thus allowing faster system response. [22] The output stages in other solutions were adjusted according to individual solution needs for input resistors, ca-

pacitive feedback and reference voltage. The reader may refer to the prototype schematics provided in appendix 13.

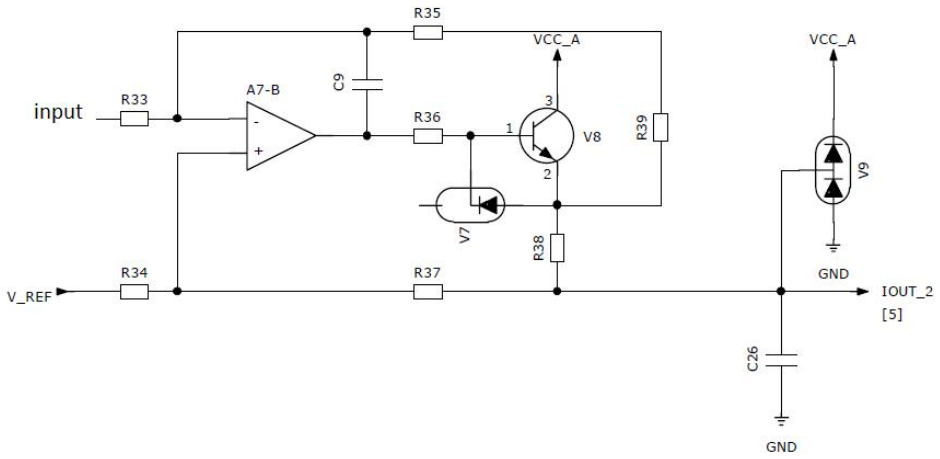



Figure 45 the improved output stage

In solution 1 the stage individual hardware modifications were also the added flywheel diode V4 to the optocoupler LED. The V4 helps the optocoupler LED to recover faster from saturation similarly as the Baker clamp in the output stage, which in turn improves the rise time of the optocoupler transistor.

The added DC corrector functionality for systems which use PWM pulse width as the information signal, namely solutions 1 and 2, was a switching system based on either a P-channel or N-channel MOSFET driven by the comparator as in solution 1 or directly by the optocoupler as in solution 2.

On the left side of figure 46 is the switching system in solution 1 in which a P-channel MOSFET bypasses the R29 and connects the output directly to $V_{Ref}$ when the output of the comparator A1-B is low and while the comparator output is high the switch is closed and the output of the system is defined by the voltage divider formed by R29, R30 and $V_{ref}$.

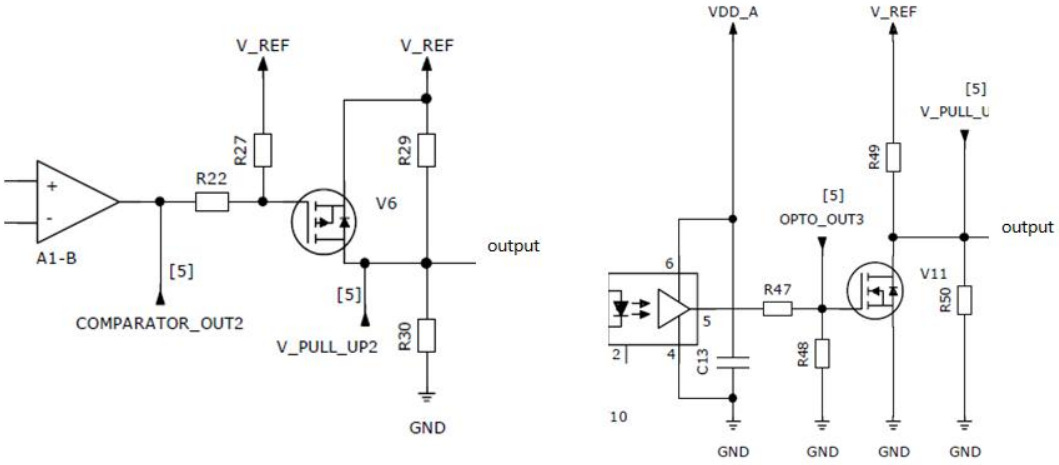



Figure 46 Logic level correction stage in solutions 1 and 2

The right hand side circuit in figure 46 is the switching system for solution 2 which utilizes a fully active output optocoupler thus allowing fast drive of a MOSFET. The system differs from the solution 1 circuit by its logic operation and switched voltage levels. When the optocoupler output is high the switch bypasses the R50 and the output of the system will be coupled directly to the ground and on the opposite logic level the switch will be closed and the output will be driven to voltage defined by the voltage divider formed by R49, R50 and the reference voltage.

The technology solution in the frequency to voltage converter was based on a timing device which will trigger a fixed period of high or low state determined by external timing network at every given input stimulant to it. The first device of choice was a precision universal timing device which was configured to suit the task and the second device was a timing operation designated dual device.

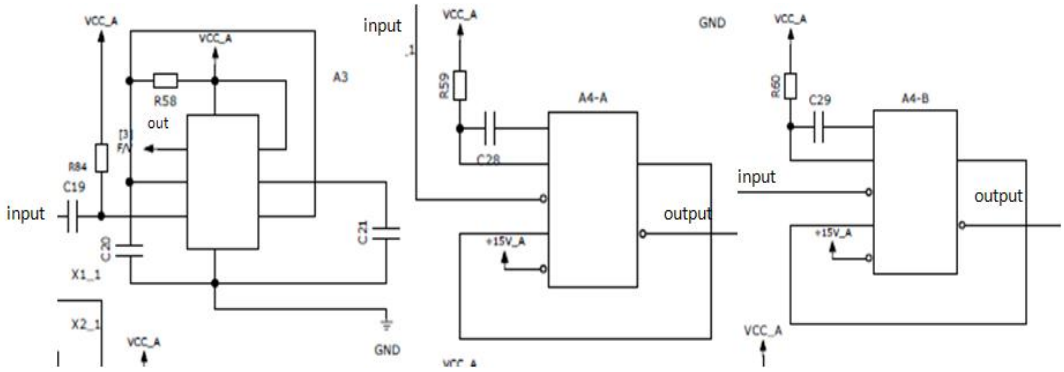



Figure 47 the frequency to voltage converters

The first timing device in the left hand side of figure 47 produces a fixed high state period on falling input stimulant edge from the optocoupler. Recalling the average voltage value equation (9) and the relation in equation (18) we can rewrite the approximate average voltage equation for the frequency to voltage conversion as

$$f = \frac{1}{T} \tag{18}$$

$$V_{Average} = \frac{V_{High} \times t_{High}}{T} = V_{High} \times t_{High} \times f = kf \tag{19}$$

In which k = constant length pulse, f= frequency. We can see that the average voltage is determined by constant length pulse k and the input frequency, the more frequently the pulse is called upon the higher the average output voltage as the pulse time low grows smaller with the overall period as illustrated in figure 48.

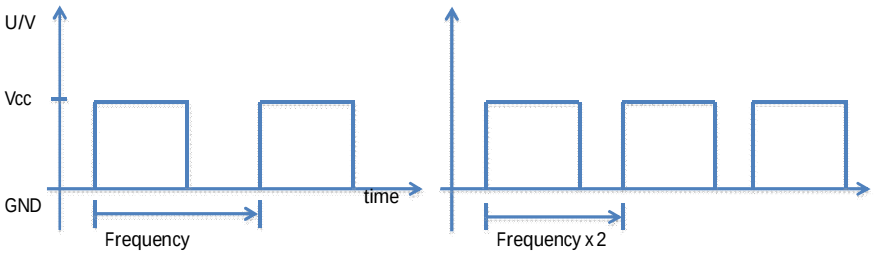



Figure 48 operation principle of the frequency solution

The latter two devices operate on a similar principle but producing a constant length low state pulse on input stimulant. For the constant length low state pulse timer system the average voltage value can be written as

$$V_{Average} = \frac{V_{High} \times t_{High}}{T} = V_{High} - V_{High} \times t_{Low} \times f = V_{High} - pf \quad (20)$$

In which the p=constant length low pulse. The equation above shows that the higher the timer input pulse frequency the lower the average voltage.

As the timer output voltage pulse peak-to-peak value is from ground to its power supply rail value it allowed the integration of the voltage pull-up stage to the timer as the output stage control voltage maximum and minimum were dimensioned as a portion of the timer average output voltage range, furthermore it allowed a possibility to use system calibration without sacrificing output current resolution.

The filter stage operational amplifier was upgraded and slight experimentation was done with the filter frequency selective network resistor values to study the quality of the transfer of the DC voltage while keeping the cut off frequency practically unchanged by altering the capacitor values.

### 4.1.3 Prototype Designing Simulations

Simulations were carried out to ensure the correct operation of the re-dimensioned output stages and the MOSFET switches. As there was no correct timer PSpice model available, the frequency solutions were simulated using a generic device only to ensure the validity of the conversion method.

The MOSFET switches were tested for optimum performance using different resistor values and digital high switching performance N-type and P-type MOSFETs. The testing circuit is given in appendix 14.

The switches were tested using the duty cycle pulse train of which theoretical averaged voltage outcomes 7,5V and 2,5V were known and the filter was given ample averaging

time of 10ms. The input stimulants were set to emulate the signals coming from the respective optocoupler in each solution. The rise and fall time for solution 1 were selected according to the observations done in laboratory and for the new optocoupler the values were evaluated from the device datasheet.

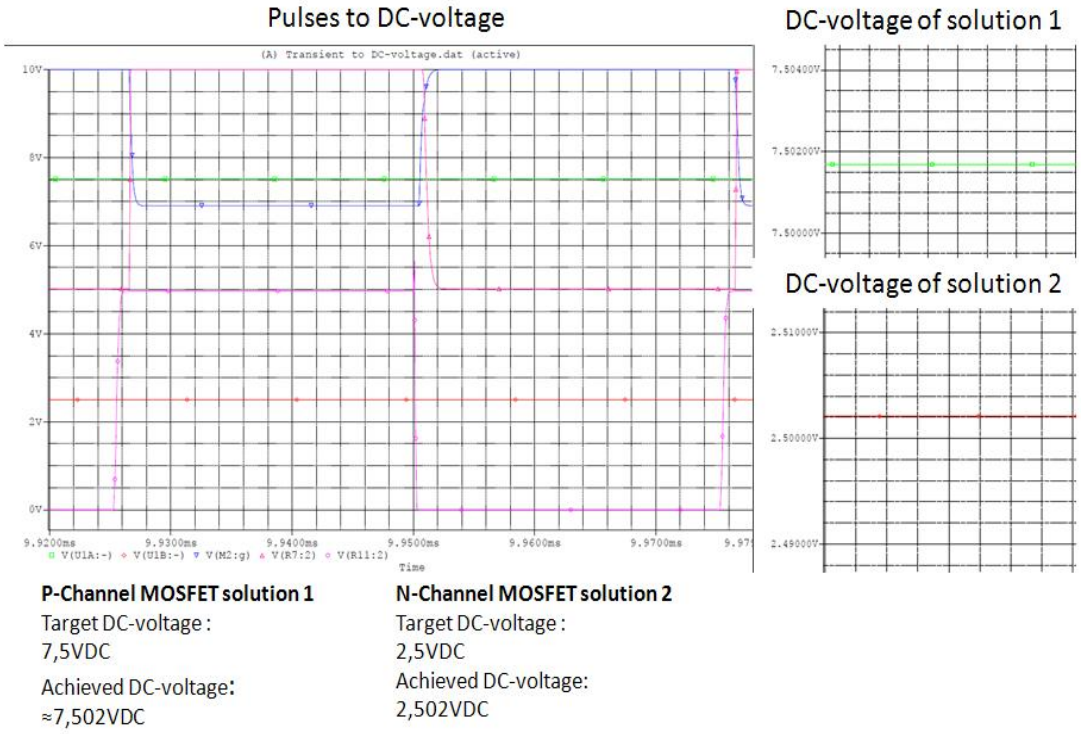



Figure 49 MOSFET switching system's simulation results

The simulation results in figure 49 show success in achieving the correct DC values for both of the switching solutions, the simulation results are also provided in appendix 15 with better resolution.

All output stage configurations were simulated to verify the proper functionality of each circuit after the feedback balancing modification, resistor value and reference voltage requirements were dimensioned. All stages functioned properly.

## 4.2 Testing of the Prototype

### 4.2.1 Output Current Error Measurements

A group of five randomly selected prototype boards were corrected from design faults as much as possible and prepared for testing. The P-channel MOSFET design in solution 1 was found to be inefficient to produce any usable measurement data and was therefore left out of the main measurements. Later on a single solution 1 circuit on a heavily altered test board was modified with a N-channel MOSFET design as found in solution 2 and was brought to full operation and measured to gather some guideline data.

The testing configuration was kept identical to the setup used in the preceded laboratory work around the original design. The testing setup is illustrated in figure 27 in section 3.3.2. In addition the testing equipment was kept identical with the initial configuration with the exception of output current measuring multi-meter which was changed to Fluke 87 true RMS.

The input stimulant settings were adjusted according to the solution topology. Solutions 1 and 2 which use the duty cycle approach were given a pulse width sweep from 0s to 49µs with steps of 1us using a constant frequency of 20kHz, whereas the frequency utilizing solution 3 was given a frequency sweep with steps of 100Hz using a constant 50% duty cycle. The amplitude for both signals was set to emulate a microcontroller PWM output signal level.

The frequency solution timer 1 was altered from the initial design to operate with any pulse width as opposed to the initial design of high frequency range with limited 10µs pulse width. The conversion lowered the frequency to range from 6kHz to 12kHz but allowed a pure frequency control independent from pulse width. The second frequency conversion system ranged from around 10kHz to 20kHz while the last circuit ranged from around 8kHz to 16kHz.

Due to the timing network component tolerances of the timer device, the frequency range had fluctuations between boards. The starting point of every frequency sweep

had to be determined individually so that the sweep starting point corresponded with the output stage current starting point. In addition, the fluctuations in the timer frequency range also meant that the amount measuring points varied slightly when using a constant 100Hz stepping throughout the measurements. Therefore the output current range was scaled individually between the measurements to accommodate the corresponding amount of collected 100Hz data points.

The final output current error data in solutions 1 and 2 was obtained by using the equation (21) to calculate the ideal output current and then subtracting it from the measured output current data.

$$I_{out} = k'D \tag{21}$$

$$I_{out} = k'\frac{p}{p_{tot}} \tag{22}$$

In which k'=constant, D=duty cycle, p=data point, $p_{tot}$=total amount of data points

In solution 3 the error data was acquired similarly but using the equation (22) instead.

### 4.2.2 Output Current Error Measurements Carried Out by a Neutral Operator

The experiment introduced in previous section was repeat by two nonaligned operators two remove possible bias introduced to the measuring results by the original operator, produce repeatability to the results and he obtained data would bring valuable statistic aspect in defining the accuracy of the prototype.

The operators were given oral instructions how to operate the equipment and how to conduct the sweep to each board and the author of this thesis operated as the experiment supervisor. The sweeps were conducted initially to boards 1-3 selected by the first operator and the second operator then continued with the selected boards. To save time a 200Hz stepping was used for the frequency systems to carry out the measurements in a brief time. The data was collected and processed by the author.

### 4.2.3 Performance in Various Temperatures

Two solutions, one of each topology of pulse width and frequency conversion, were selected from a randomly selected board to be tested in the product specification dictated temperature range of 0°C to 85°C. The selected systems were the solutions built around the new optocoupler and the dual timer device of whose two frequency ranges the higher 10kHz to 20kHz was deployed. Each solution's performance was tested at the extreme ends of the temperature range and in a typical system operation condition temperature of 50°C.

The measurement setup was kept consistent with the early temperature experiments described in section 3.3.5 with an exception of the signal generator feeding two signal paths in parallel and two multi-meters reading the corresponding current outputs. This modification allowed data collection from signal paths in turns without interrupting the climate device. A Fluke 175 was assigned to measure the duty cycle based solution while a Fluke 87 was monitoring the frequency converting system. An additional 516Ω resistive load was also introduced to the setup as the load for the frequency system.

The climate device was set to alter the temperature only and after the desired temperature was present in the climate cabinet the prototype board was allowed to accommodate the ambient temperature for approximately 20 minutes before the data collection. A full duty cycle sweep with 1us steps or frequency sweep with 200Hz steps was carried out to corresponding solution at a time and the data was gathered in to an excel sheet. Additional photographic material was also taken to evaluate the signal transfer quality in the systems.

### 4.2.4 Results of the Prototype Measurements

A common output current error feature to all solutions was a residual current when the systems were driven down. The residual current varied between systems from 0,040mA to 0,090mA depending on the tested board and the circuit topology. The smallest leakage current was measured on the frequency solutions while the duty cycle operated system's leakage was larger and varied slightly.

The single corrected solution 1 circuit showed improvement in maximum error magnitude but the overall performance remained non-linear. The measurement data is showed in the figure below.

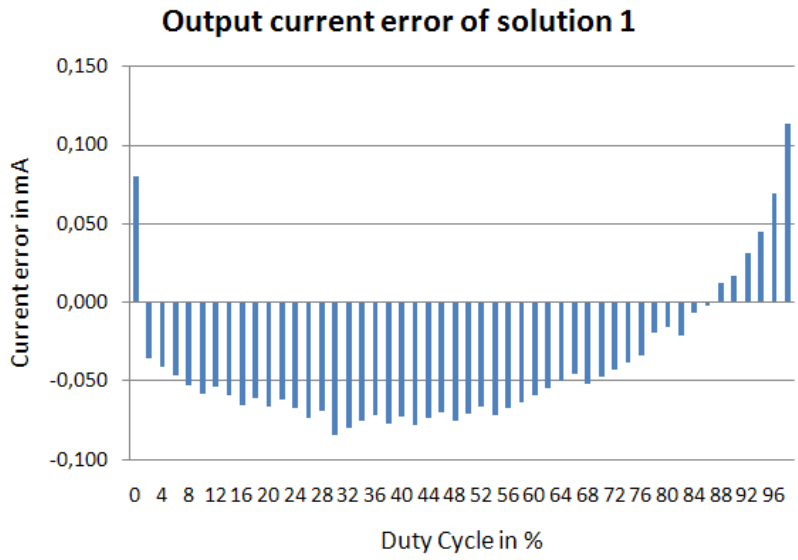



Figure 50 the solution 1 output current error

The output current remained slightly non-linear in the middle of the duty cycle range and the trend has turned from over current to minor under current. The polarity of the error changes in the high end of the range at approximately 80% duty cycle to slight over current. The maximum error of 0,114mA can be found in the end of the sweep at 98% duty cycle.

The solution 2 exhibited two distinctive error patterns as seen in figure 51. Three out of five tested circuits exhibited the output current error trend seen on the left hand side of the figure 51 and remaining two followed the pattern on the right side. The first error pattern on the left resembles closely the error plot already seen in figure 50 which was measured from the solution 1 whereas the right hand side error curve seems more linear after a certain critical point.

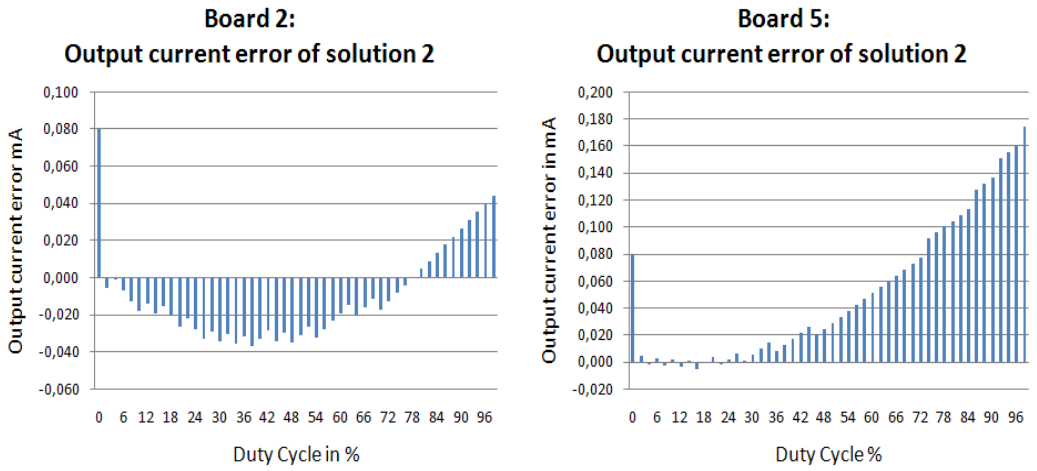



Figure 51 solution 2 output current error patterns

The maximum error found in the individuals shown in the figure above was found to be 0,080mA in board 2 and 0,174mA in board 5. In all solution 2 circuits the off-state leakage current varied between 0,080mA to 0,090mA.

A typical output current error curve for the single timer frequency operated system is given in figure 52.

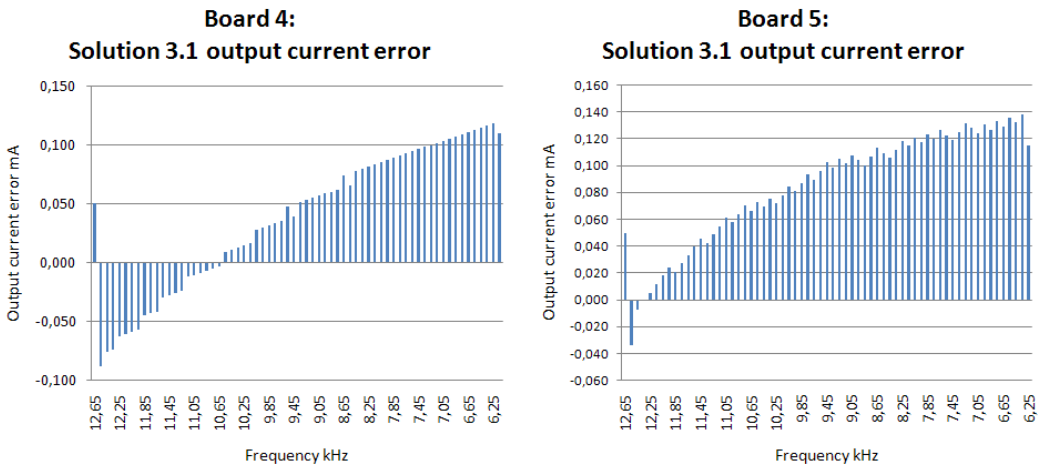



Figure 52 output error pattern of solution 3

As the output current starting point was always estimated the output current error could change in magnitude and polarity but a distinctive error pattern can still be ob-

served in figure 52, furthermore, it shows that the linearity improvement is minor but the maximum error magnitude seems drastically decreased. In the example boards 4 and 5 the maximum under currents of 0,118mA and 0,138mA were found in the ends of the frequency range.

The final frequency solutions 3.2 and 3.3 output current error characteristics varied only slightly and only two systems out of ten exhibited the pattern shown on the left side in the figure below while the rest fell to the pattern on the right side, furthermore the scarcer pattern was only encountered in the solution 3.2 which used the higher frequency range.

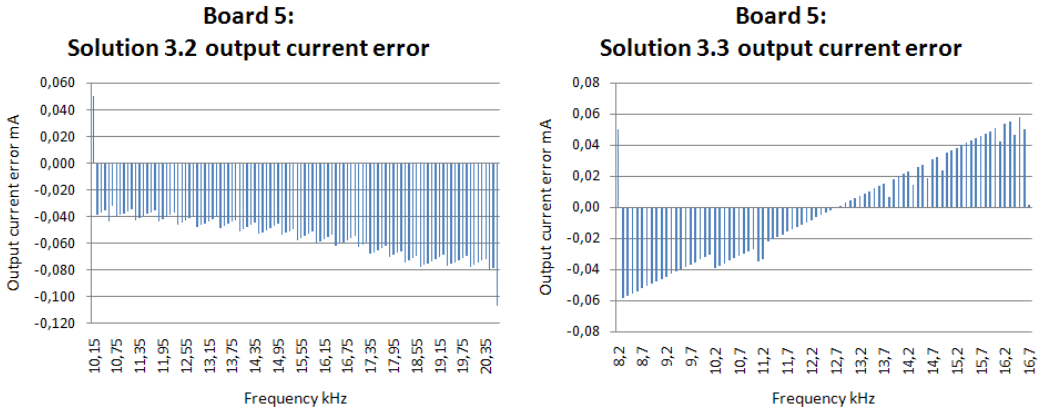



Figure 53 output current error characteristics of solution 3.2 and 3.3

Both systems exhibited major improvement in both linearity and total system error. Figure 53 also shows that both patterns are very linear especially the pattern seen on the right side. In addition the initial measurements show significant improvement in error. In this particular board the absolute values of the maximum error were found to be 0,107mA for solution 3.2 and 0,060mA for solution 3.3 respectively.

The randomly chosen board for the temperature measurements was board 5 and the temperature measurement results collected from solution 2 are gathered in to a collage in figure 54.

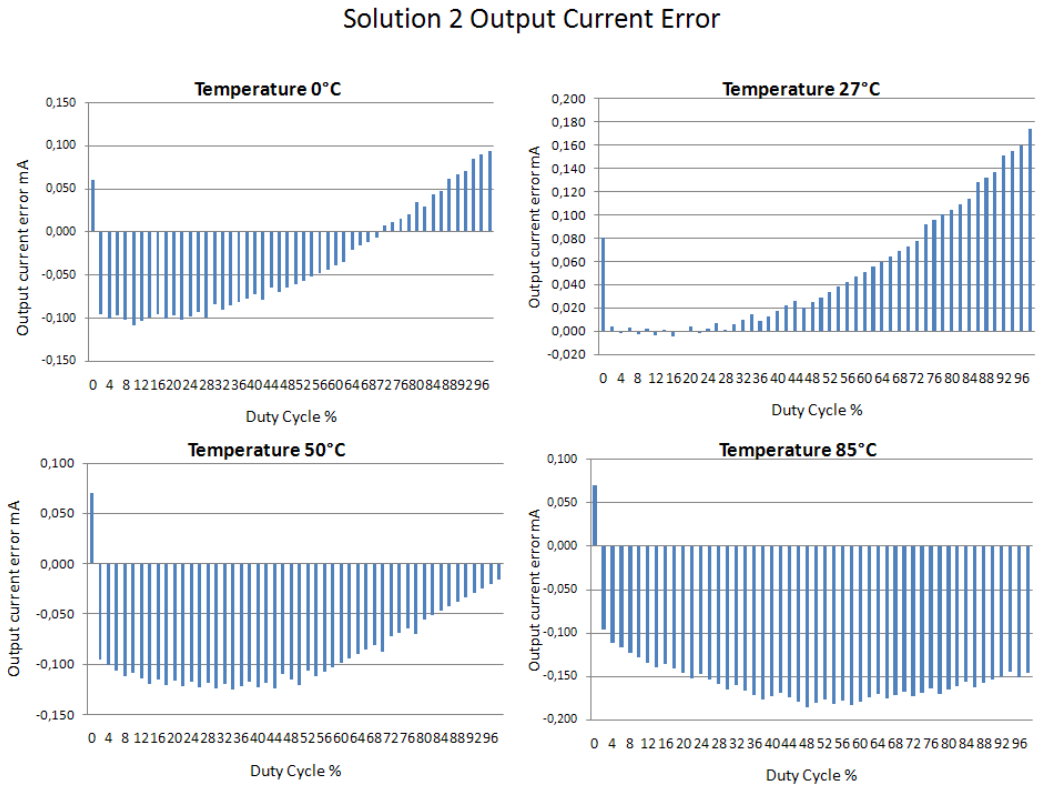



Figure 54 temperature behaviour of solution 2

The thermal behaviour of the system indicates a moderate inaccuracy fluctuation throughout the measurement. The system response becomes very non-linear in low end of 0°C and 50°C onwards as the curve shape changes and the maximum error location varies greatly. On the other hand, the magnitude of the maximum error does not vary as violently. We can also see that the output current error changes polarity from moderate over current to under current as the temperature increases and in low temperature the output current error can change at some point of the duty cycle range, in this particular system the polarity change occurred at around 70% duty cycle. The full-scale error remained under the target of +/-1% throughout the temperature sweep with minimum and maximum values of -0,54% and -0,94% respectively.

The frequency solution temperature sweep results are shown in figure 55.

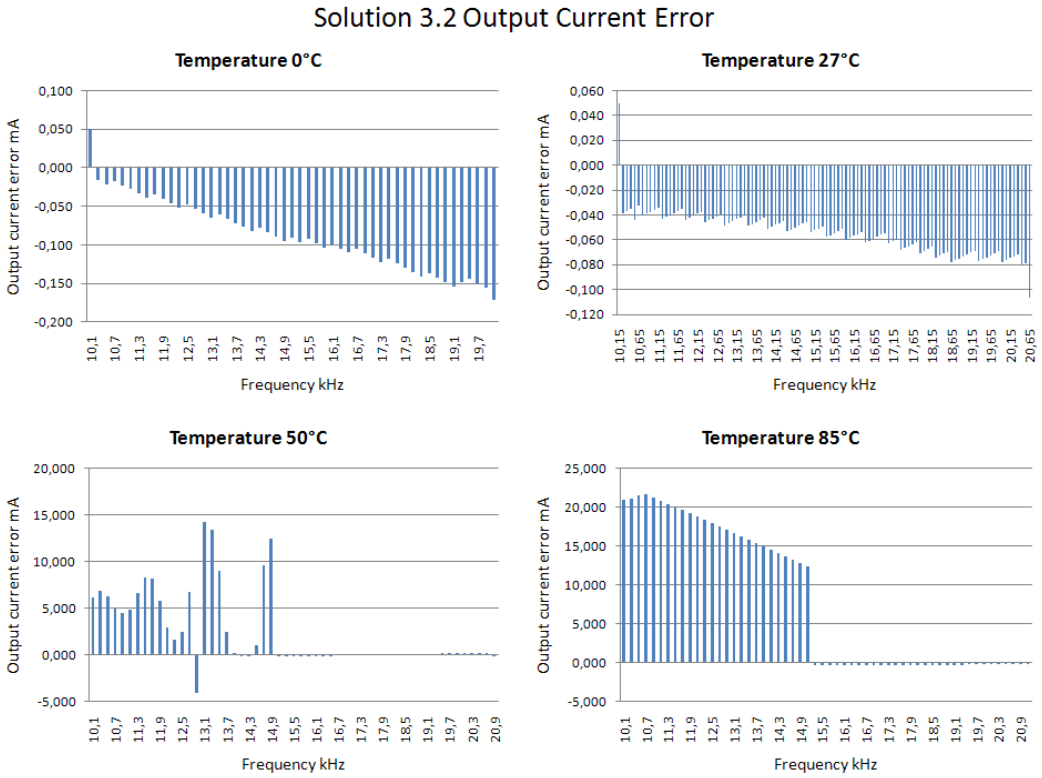



Figure 55 temperature behaviour of solution 3.2

figure 55 indicates that the frequency conversion system operation is susceptible to temperature variations. At low temperatures the overall system error remained linear and its magnitude in reasonable proportions but the higher end of the frequency range contracted from 20,65kHz measured in room temperature to 20,3kHz.

When the temperature was increased the system was found to be unstable. In 50°C the system operation went haywire at low frequencies of the sweep range. The output current fluctuated uncontrollably between unreasonable figures of which some was collected and processed as given in figure 55. Later on at higher frequencies around 15kHz the operation stabilized and reasonable measuring data was obtained.

The same phenomenon occurred again at 85°C and similarly the operation stabilized at around 15kHz. As the system was not fully functional at high temperatures the high end data is not presented here. Instead visual material from the malfunction is pre-

sented in figure 57. The measurement data graphs from the stabilized operation can be found in appendix 14, however.

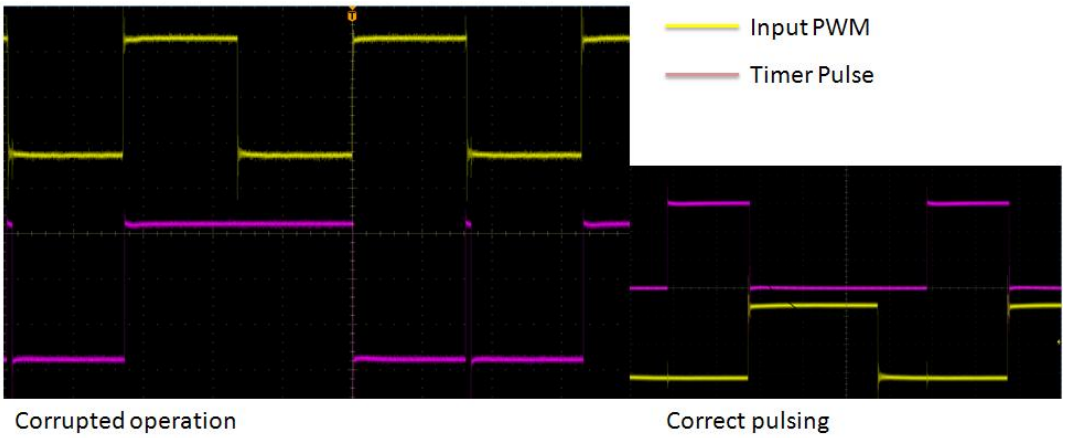



Figure 56 the solution 3.2 waveform in 50°C

The figure above, taken from low frequency operation at 50°C, shows that the system missed and introduced random additional pulses. Furthermore, its operation was even inversed for some trigger edges.

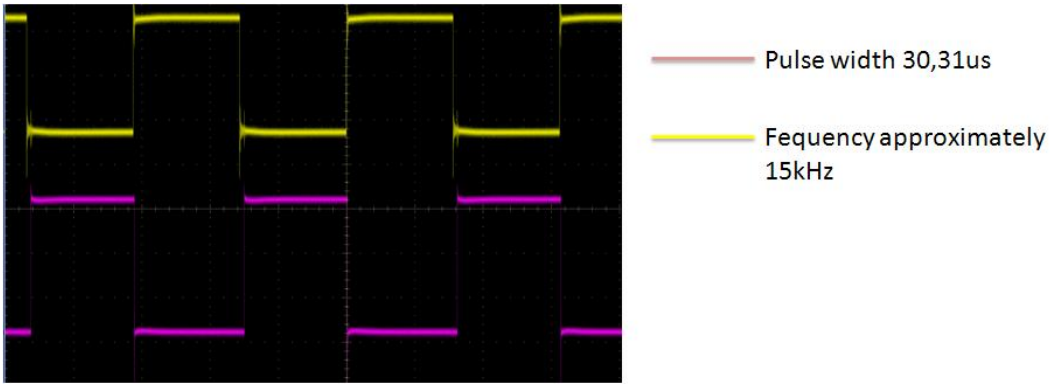



Figure 57 the solution 3.2 stabilized operations above 15kHz in 50°C

The system stabilized to normal operation after around 15kHz as seen in figure 57 and the output current error curves followed normal behaviour.

### 4.2.5 Full-scale Error Performance of the Prototype against the Current Solution

The output current error data collected in 27°C was processed to determine the full-scale error in each solution. The obtained output current error data was scaled against the output current range maximum to determine the full-scale error of the solution.

The definition for full-scale error is given in section 1.4.3, however for revision the total system error is defined as the ratio in percentage of the maximum error found in the system against the nominal maximum output current of 20mA as described below.

$$Error-\%_{Full-Scale}=\frac{Error_{MAX}\left(mA\right)}{20mA}\times 100\%$$

The full-scale error in percentage for each tested solution with the results of the old design circuit incorporated in each test board as a reference are gathered in the table below. May it be reminded that only solutions 2 and 3.1-3 were measured by the two unaligned operators and the reference circuit and the solution 1 results are included from the previous measurement results illustrated in table 3.

Table 3 full-scale error in tested boards

Full-scale Error in Percent in each Test Board

| | Reference | Solution 1 | Solution 2 | Solution 3.1 | Solution 3.2 | Solution 3.3 |
|---|---|---|---|---|---|---|
| Test board 1 | 1,82 | 0,57 | 0,40 | 0,57 | -0,47 | 0,25 |
| Test board 2 | 1,18 | n/a | 0,40 | 0,37 | 0,30 | 0,29 |
| Test board 3 | 1,70 | n/a | 1,07 | 0,58 | 0,49 | 0,40 |
| Test board 4 | 1,74 | n/a | 0,45 | 0,53 | 0,37 | 0,25 |
| Test board 5 | 2,42 | n/a | 0,87 | 0,62 | -0,53 | 0,29 |
| Mean | 1,772 | 0,57 | 0,638 | 0,534 | 0,432 | 0,296 |

In general we can see that all the solutions gained substantial improvement in total system error in comparison to the old circuit topology. The target accuracy of +/-1% is clearly achieved with the frequency conversion solutions while the pulse width systems need more study but fared admirably.

As only one solution 1 circuit was brought to full operation its statistical performance remains unclear and its performance must be studied further, nevertheless its measurement data provided valuable knowledge about the direction of the design success.

Two unaligned operators measured selected boards 1, 3 and 5 obtaining accuracy results given in table 4.

Table 4 unbiased operator measurement results

| Full-scale Error in Percent Tested by Two Unaligned Operators | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Reference | Solution 1 | Solution 2 | Solution 3.1 | Solution 3.2 | Solution 3.3 |
| Operator1 | Test board 1 | 1,82 | n/a | 0,47 | -0,75 | 0,31 | -0,32 |
| | Test board 3 | 1,70 | n/a | 1,12 | 0,79 | 1,45 | -0,97 |
| | Test board 5 | 2,42 | n/a | 0,77 | 1,24 | 0,25 | -1,90 |
| Operator 2 | Test board 1 | 1,70 | n/a | 0,42 | -0,6 | -0,63 | -0,83 |
| | Test board 3 | 2,42 | n/a | 1,07 | 0,6 | 0,89 | -0,28 |
| | Test board 5 | 2,58 | n/a | 0,72 | 0,64 | 2,29 | 2,1 |
| | Mean | 2,11 | n/a | 0,76 | 0,77 | 0,97 | 1,07 |

We can see that there is broad deviation in accuracy but the average accuracy remains around 1%. The duty cycle operated solution 2 results have the smallest deviation while the frequency operated systems in some cases even fall out of the target accuracy.

The mean values in tables 3 and 4 were obtained by using equation (23).

$$Mean = \frac{\sum |accuracy - \%|}{n} \tag{23}$$

In which, accuracy-% is the circuit full-scale accuracy

n=total amount of tested identical solutions

### 4.2.6 Comments on the Prototype Experiments and Error Considerations

The measuring equipment was kept as identical as possible to the initial root cause analysis measurements to retain the integrity and comparability of the measurements. Changing the multi-meter to a more accurate one than the initial device may have caused some deviation to the results but it should not be crucial to the study outcome as both devices are of high quality and accurate measuring equipment.

An important humane factor that may have caused bias to the results is the scaling procedure conducted to the frequency solutions even though two unbiased operators were involved as the author processed all the data. This may have caused accuracy variation for better or worse. Had the frequency range been always the same between the boards, the comparison would have been easier and more reliable. Nevertheless the topology has proved to be worthwhile to study as it clearly showed excellent response in both linearity and accuracy wise, reaching the target with flying colours.

The inaccuracy of some of the frequency solutions studied in unaligned operator measurements was explained by a stepping error. After checking the stepping on each measurement the operator 1 measurements board 3/solution 3.2 and board 5/solution 3.3 had frequency step error as the calculated current step had dropped at one point from 450µA to 230µA meaning that there was a half frequency step of 100Hz at the measuring point instead of the nominal 200Hz.

The operator 2 had two similar errors in his measurement records. On board 5 the solutions 3.2 and 3.3 had stepping errors in the beginning of the sweep. The measurement current increase was 900µA instead of correct step of 450µA. This is due to poorly determined starting point of the slope or a missed data point, in any case the data is valuable and the systems still fared well.

A lesson learned would be a more proper introductory to the operation principles of the frequency system for the unbiased operators. On the other hand the information how the system works in untrained hands seems more valuable as it somewhat reflects the worst case scenario of the system accuracy.

It came as a complete surprise that the frequency conversion system turned out to be unstable at high temperatures. Nevertheless all hope is not lost on it as it returned to normal operation at high frequencies beyond 15kHz.

It is most likely that, due to the more simple nature of the solution 2 over the frequency solutions and to the simplicity its measurement procedure, the data collected from it is more consistent and reliable than the data collected from solution 3.2-3.

# 5 Discussion and Conclusions

Even though the solution 1 was not studied extensively its performance indicated outstanding improvement as its full-scale error was found to be well under the target set for the project. The maximum system error of 0,114mA was found on the maximum end of the sweep which is not as critical as if it would have occurred in the middle of the sweep. This is due to the reason that the middle portion of the range is more commonly used and over range beyond 20mA is only used if the system is unable to achieve 20mA in normal conditions. If the over range error is excluded the system maximum error was located at 30% duty cycle with -0,084mA which specifies the system to -0,47% full-scale error.

The full-scale error was significantly improved but the non-linear transfer remained. This was somewhat expected as the optocoupler and comparator stage performance is limited as it was discovered in the initial AO-1 measurements. The error changed to expected negative polarity but the pattern however came as a surprise. It remains unclear why the error pattern shown in figure 50 changes polarity at some point of the sweep but it is expected to be for some part the result of the pulse width distortion caused by the optocoupler, comparator and the MOSFET stage.

Due to the fact that only one solution 1 circuit was measured, a more thorough study on the system with the altered MOSFET switching system is recommended to determine the statistical performance due to component variations and the system should also be tested in the climate device to ensure the stability of the accuracy in extreme

temperatures. However a careful performance estimate is that the system error will start to increase as it was discovered in the AO-1 thermal measurements that both the optocoupler and the comparator device outputs will start to fluctuate as shown in figure 33, however the magnitude of the increased error is uncertain.

The solution 2 exhibited similar error pattern as solution 1 as we can conclude by comparing the figure 50 and figure 51. We can also see that the error in solution 2 seems to have variation in offset. More linear performance was expected from this solution. The non-linearity is surmised to be the result of the optocoupler device tolerances and the performance of the MOSFET switching system similarly as in solution 1.

The waveform at MOSFET circuit was monitored in the temperature and initial prototype measurements and found that it introduces PWD as the PWM falling edge is created actively and the rising edge passively. The MOSFET was set sufficiently high to ensure proper logic values for the PWM but regardless of chosen load the peak values did not reach desired accuracy. A further increase slowed the pull-up causing more harm than good and decreasing the load provider poorer logic levels.

Solution 2 almost fully met the target of 1% in terms of accuracy with only one circuit barely falling out of the specification. The reason for this was that the offset of the error pattern. The maximum error was consistently found at the end of the sweep in room temperature and as it was large shifting the slope fully to the positive y-axis, it emphasized the magnitude of the maximum error. This phenomenon was also observed on one additional board which was second most inaccurate. Why the pattern level shifts is unclear and is highly recommended to be investigated as it would also possibly bring additional information about solution 1 behaviour.

Solution 2 also proved itself to be a sturdy design even in extreme temperatures as the tested circuit maintained the target accuracy of 1%. However, the circuit had a tendency of producing under current in both low and high temperatures and the linearity fluctuated moderately. The output current behaviour translates to a decreased control voltage seen by the output stage which speaks of PWD and poorly defined PWM logic levels.

The solution 3.1 results show that the system can produce accurate output current and the system also fared well in the unaligned operator measurement but as we can see from figure 52 the error pattern is slightly non-linear and has similar offset quality as the duty cycle solutions. Although the system fared well a major drawback in the design is a technical parameter of the timing device which limits the usable frequency range at least below 15kHz if constant 50% duty cycle is to be used. The frequency can be increased but while doing so the pulse width must be set small which can be undesirable.

Similar error pattern as found in the solution 3.1 was not encountered in the other frequency conversion system which indicates that as they all shared the same output stage the timing device itself produces the non-linear response. Nevertheless in comparison to all duty cycle solutions the frequency systems provided good linearity regardless of the converting device.

The maximum output current error in all frequency solutions seems very much dependent on how the sweep starting point was determined and therefore the maximum output current error varies. Therefore more independent data from the measurement method on the frequency topologies would be achieved by using small tolerance timing components which would fix the sweep range and starting point to a single static point.

It is unfortunate that due to lack of time only two solutions and one board were studied in various temperatures because it remains unknown how the single timer device in solution 3.1 withstands temperature fluctuations and how good the statistical performance of all solutions over the temperature range is. Therefore it is recommended that the solution 3.1 would undergo a thorough temperature testing if it is considered to be implemented.

For the most part, solution 3.2-3 suffers from the same drawbacks as the first frequency conversion system. However the different timing device allowed a broader frequency range and the system response was much more linear. Comparing the output current error of the solution 3.2 figure 53 to the corresponding error of duty cycle sys-

tems the difference in linearity is enormous. However, as it was later observed the system became unstable at higher temperatures, which is a major drawback from production point of view. On the other hand, the system did return to normal operation at higher frequencies above 15kHz as seen in figure 57 and it is therefore advisable that the system timing components should be revised to obtain higher operational frequency range and the system performance studied in range beyond the critical frequency.

As we can see from the table 3 accuracy target was met with all solutions with the exception of one solution 2 circuit falling out. From a statistical point of view only solution 2 can be said to meet the requirements for reducibility to some extent.

All in all the project method was found to be sound for the study purposes. The simulation software was not as useful as expected in determining the causes of error but in the design process it was found to be valuable tool. However, even though the simulation was useful the time use could still have been emphasised more on laboratory work as it provided the most prolific results about both the old and new designs. Furthermore due to lack of time many aspects about the new designs were left without study. Nevertheless, considering the amount of time in which the research and development study with a full working prototype was conducted the achieved results are excellent.

# 6 Solution Evaluation

The solutions were evaluated in respect to the key aspects of cost efficiency, accuracy, component availability and physical foot print on the actual circuit board along with solution individual weaknesses and strengths discovered in the testing. In addition, a cost estimate was calculated for each solution and added to the evaluation tables using an international component supplier prices for modest component bulks. The cost estimate calculations are provided in appendices 15-16.

The evaluation of solution 1 is shown in table 5.

Table 5 the strengths and weaknesses of solution 1

| Solution 1 | |
|---|---|
| Strengths: | - Only few modifications and additional components<br>- Carefully selected inexpensive components have vast availability that avoids possible sourcing issues.<br>- Excellent initial accuracy performance |
| Weaknesses: | - Design fault left the overall statistical performance uncertain.<br>- Added components mean costs and increased foot print<br>- Stability over temperature is unknown |
| Cost: | 2,15USD (Current solution 2,01USD) |

The initial results after corrective actions show that the system can produce good results with modest repairs. From sourcing point of view the solution 1 is sound choice as its components are widely available, on the other hand, the added components increased the circuit costs by 6,5%. Furthermore adding components means that the circuit requires more board space.

Table 6 the strengths and weaknesses of solution 2

| | |
|---|---|
| Solution 2<br>Strengths: | - Design eliminated the comparator stage thus relieving board space.<br>- The removed comparator stage brought cost savings<br>- Excellent statistical accuracy performance<br>- Robust and accurate over the specified system temperature range. |
| Solution 2<br>Weaknesses: | - Error pattern remained slightly non-linear for some units<br>- Second source for the optocoupler is uncertain<br>- Selected solution 2 optocoupler requires its own low voltage power supply |
| Cost: | 1,91USD (Current solution 2,01USD) |

The solution 2 evaluation is given in table above. The solution 2 performed admirably in all tests proving to be accurate and reliable even in extreme circumstances. The design is somewhat smaller and simpler than the original and therefore it brought cost

savings of 5% and is expected to relieve some board space. However, it was discovered that the assumed second source device does not provide an alternative for the current device therefore sourcing may become an issue.

The frequency to voltage conversion system was found out to be a promising design and its evaluation is given in table 7. Its accuracy can be superior if configured properly and if the timing components are upgraded with proper tolerance devices the frequency range can be stabilized.

Table 7 the strengths and weaknesses of solution 3 (single)

| | |
|---|---|
| Solution 3 (single 3.1) Strengths: | - Simple design which embeds all the stages in old design to one device<br>- Relieves physical board space long with the stage integration<br>- GND to VCC voltage enables system calibration<br>- Superior statistical accuracy and adequately linear performance<br>- Simple common components ease sourcing<br>- May be used in systems in which a single analogue output is needed<br>- Dual device also available for multiple analogue output circuits<br>- Dual device available for same price as single device |
| Solution 3 (single 3.1) Weaknesses: | - Timing component tolerances affect the frequency range<br>- Accurate timing components may be expensive<br>- Limited operational frequency range<br>- Performance in extreme temperatures is unknown |
| Cost: | 2,07USD (Current solution 2,01USD) |

The design is about the use of common components, integration and simplicity. From this point of view the frequency conversion system is the preferred choice. Even though the design is simple it is not the cheapest which came as a surprise. In addition, the microprocessor properties form a big factor whether the system can be used or not and how accurate and well controlled the analogue output will be. With the current component tolerances the importance of the microcontroller PWM-output capabilities are further exaggerated as the frequency sweep must be configured to match the output stage current sweep. This aspect holds true on the dual device frequency con-

version system as well. Nevertheless, the solution was shown to be accurate and more linear than the old solution.

Table 8 the strengths and weaknesses of solution 3 (dual)

| | |
|---|---|
| Solution 3 (dual 3.2-3) Strengths: | - Simple design which embeds all the stages in old design to one device<br>- Less restricted frequency range<br>- Relieves much physical board space long with the stage integration<br>- Superior statistical accuracy and very linear performance<br>- Simple common components ease sourcing |
| Solution 3 (dual 3.2-3) Weaknesses: | - Timing component tolerances affect the frequency range<br>- Accurate timing components may be expensive<br>- Extreme temperatures may cause instability! |
| Cost: | 2,05USD (Current solution 2,01USD) |

The solution 3.2-3 comparisons are shown above. It is preferred over the solution 3.1 for its less restricted frequency range and more linear performance. In other respects all frequency solutions have very similar strengths. However, the circuit is slightly cheaper than solution 3.1.

Currently the system was found to be unstable below the critical frequency at high temperatures and in addition as the solution 3.2-3 relies currently also on versatile microcontroller it suffers in this respect from the same requirements as solution 3.1.

# 7 Project Summary

The main objectives of the project were to find cost efficient solutions which would improve the linearity and accuracy of the previous analogue output circuitry design in the old generation frequency converter control board. The target set for the project was to enhance the linearity of the analogue output system and improve its accuracy from the old specification of +/-3% to +/-1%. The design parameters set for the design were cost efficiency, circuit board footprint and component availability also the critical galvanic isolation stage must be implemented.

The previous generation analogue output was analyzed using theory, simulation and hands on work in a laboratory. The simulations and laboratory work suggested that the main bottlenecks in the circuit were the optocoupler and the comparator circuit. In addition the output stage feedback network design was found to be unbalanced.

Using the knowledge gathered from the initial study three corrective solutions were designed and implemented on a printed circuit board. Two solutions (1 and 2) used PWM pulse width as the control signal and the third solution (3.1 and 3.2-3) introduced a new approach in the form of frequency conversion to control voltage.

All implemented solutions were tested for output current accuracy and linearity and with exception of solution 1 were tested for five board statistics and three board unaligned operator statistics, in addition two solutions (2 and 3.2-3) were tested in a product specified temperature range of 0°C to 85°C.

Initially almost every solution achieved the 1% accuracy target with an exception of one solution 2 circuit which reached 1,1% in the designer performed initial measurement. When two unaligned measurement operators were called to carry out the accuracy measurement the results were more inaccurate and more boards fell out of the target. However, many of them were explained by a measurement error.

The error pattern in duty cycle solutions remained slightly non-linear but the frequency solutions especially the dual timer solution provided highly linear response. The temperature sweep proved the solution 2 robust against temperature fluctuations whereas the frequency conversion system was found to be unstable in high temperatures under 15kHz frequencies.

At the end of the project the solutions were evaluated in respect of the design parameters to provide comparison data of which to choose for individual case needs, however, many solutions were recommended to be placed under improvement scheme. Despite the frequency solution drawback experienced in the temperature measurements, the project was a success in general as the target accuracy was reached within the design parameters.

## References


1 Asea Brown Boveri(2011) *Our businesses*, (January 27th 2011) [WWW document] http://www.abb.com/cawp/abbzh252/a92797a76354298bc1256aea00487bdb.aspx (accessed 1.4.2010)

2 Mäkelä, Vesa. Discussions with ABB Design Engineer (January 4th through May 15th, 2011) Asea Brown Boweri, Helsinki Pitäjänmäki

3 Analog Devices (2011) *Analog Wizard Definition of Terms*, [WWW document] http://www.analog.com/Wizard/bridge/bridgeHelp.asp (accessed 20.5.2011)

4 Asea Brown Boveri. (2008) *ABB technical guide book,* Revision D

5 Asea Brown Broveri. Previous generation frequency converter product catalogue

6 Asea Brown Boveri. Previous generation frequency converter manual

7 IEC (2007). *IEC standard 61800-5-1.* Switzerland, IEC Head Office

8 American Power Conversion Incorporated (2002) *Description of Galvanic isolation,*(May 17th, 2001) [WWW document] http://emea-en.apc.com/app/answers/detail/a_id/1117/~/description-of-galvanic-isolation (Accessed February 20th, 2011)

9 Broskie, John (2007) *Shunt Regulators,*(June 3rd, 2007) [WWW document] http://www.tubecad.com/2007/06/blog0109.htm (Accessed March 6th, 2011)

10 Cage, S. et al.(1977) *HP Optocoupler Applications Manual.* New York: McGraw-Hill

11 Sedra, A.S., Smith, K.C. (2011) *Microelectronic Circuits,* international 6th edition. New York: Oxford University Press

12 Daycounter Incorporated (2004) *Sallen-Key Low Pass Filter Design Equations.* [WWW document] http://www.daycounter.com/Filters/SallenKeyLP/Sallen-Key-LP-Filter-Design-Equations.phtml (Accessed March 17th, 2011)

13 Floyd, Thomas. L. (2004) *Electronic Devices International edition,* 7th edition. United States of America: Pearson Prentice-Hall

14 Wikiperdia.org (2011) *Pulse-width Modulation,* (April 27th,2011) [WWW document] http://en.wikipedia.org/wiki/Pulse-width_modulation (Accessed April 6th,2011)

15 Wolfram Research (2011) *Fourier Series,* (May 18th, 2011) [WWW document] http://mathworld.wolfram.com/FourierSeries.html (Accessed March 20th, 2011)

16 Baills, T (2011) *Signals and systems, Fourier Series 2.* Lecture power point presentation. Helsinki: Metropolia University of Applied Sciences

17 Esorol Technologies (2007) *Fourier analysis of PWM signal* (October 31st ,2007) Published by Brussels Management School. Downloaded at

http://icheccampus.ichec.be/claroline/backends/download.php?url=L0xpZW5zX2V0X2F1dHJlc19zb3VyY2VzL1NwZWN0cmFsX2FuYWx5c2lzX29mX2FfUFdNX3NpZ25hbC5wZGY%3D&cidReset=true&cidReq=ELEC (Accessed March 20th, 2011)

18 All about circuits.com. *Current signal systems.* [WWW document] http://www.allaboutcircuits.com/vol_1/chpt_9/3.html (Accessed March 25th, 2011)

19 University of Guelph (2011) *Kirchoff's culrrent law.* [WWW document] http://www.physics.uoguelph.ca/tutorials/ohm/Q.ohm.KCL.html (Accessed May 17th, 2011)

20 University of Guelph (2011) *Kirchoff's voltage law.* [WWW document] http://www.physics.uoguelph.ca/tutorials/ohm/Q.ohm.KVL.html (Accessed May 17th, 2011)

21 Niskanen, Simo. Discussion with Asea Brown Boveri Personnel (April 8th, 2011) Asea Brown Boweri, Helsinki Pitäjänmäki

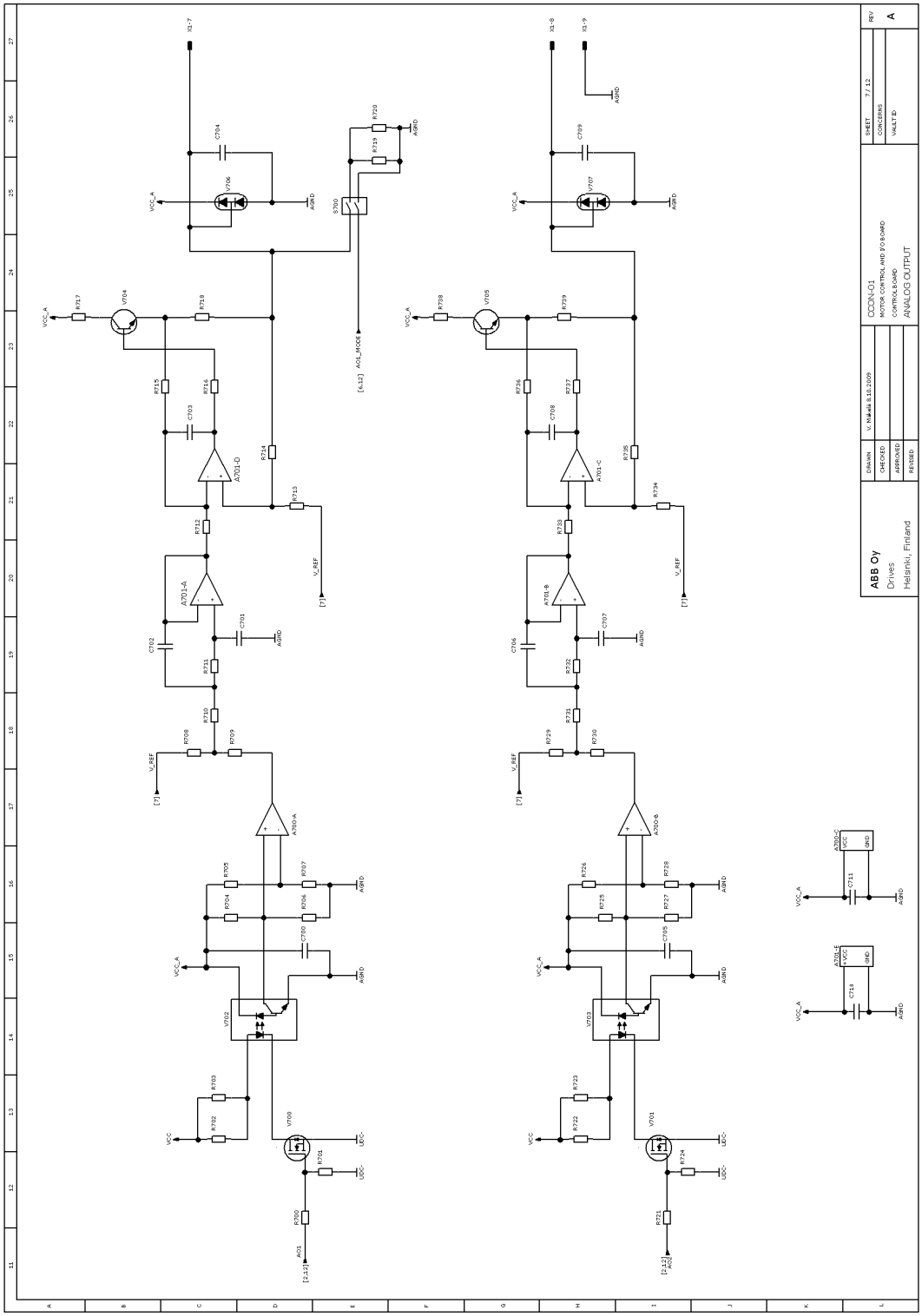
22 Baddeley, G. (2007) *Baker clamp,* (November 1st, 2009) [WWW document] http://home.pacific.net.au/~gnb/audio/bakerclamp.html (Accessed April 26th, 2011)

23 Digikey(2011) *Electronic components.* [WWW document] www.digikey.com (Accessed May 19th, 2011)

## Initial Simulation AO-1 Results

| Ton(us) | | Calculated current | Simulated Iout mA | Difference |
|---|---|---|---|---|
| 50 | 0,000453 | 0,453 | 0 | 0,537 |
| 49 | 0,000905 | 0,905 | 0,99 | 0,595 |
| 48 | 0,001358 | 1,358 | 1,50 | 0,612 |
| 47 | 0,001811 | 1,811 | 1,97 | 0,619 |
| 46 | 0,002263 | 2,263 | 2,43 | 0,627 |
| 45 | 0,002716 | 2,716 | 2,89 | 0,634 |
| 44 | 0,003169 | 3,169 | 3,35 | 0,641 |
| 43 | 0,003622 | 3,622 | 3,81 | 0,648 |
| 42 | 0,004074 | 4,074 | 4,27 | 0,646 |
| 41 | 0,004527 | 4,527 | 4,72 | 0,653 |
| 40 | 0,00498 | 4,980 | 5,18 | 0,650 |
| 39 | 0,005432 | 5,432 | 5,63 | 0,668 |
| 38 | 0,005885 | 5,885 | 6,10 | 0,655 |
| 37 | 0,006338 | 6,338 | 6,54 | 0,652 |
| 36 | 0,00679 | 6,790 | 6,99 | 0,670 |
| 35 | 0,007243 | 7,243 | 7,46 | 0,667 |
| 34 | 0,007696 | 7,696 | 7,91 | 0,664 |
| 33 | 0,008148 | 8,148 | 8,36 | 0,652 |
| 32 | 0,008601 | 8,601 | 8,80 | 0,654 |
| 31 | 0,009054 | 9,054 | 9,26 | 0,646 |
| 30 | 0,009507 | 9,507 | 9,70 | 0,643 |
| 29 | 0,009959 | 9,959 | 10,15 | 0,631 |
| 28 | 0,010412 | 10,412 | 10,59 | 0,628 |
| 27 | 0,010865 | 10,865 | 11,04 | 0,615 |
| 26 | 0,011317 | 11,317 | 11,48 | 0,603 |
| 25 | 0,01177 | 11,770 | 11,92 | 0,600 |
| 24 | 0,012223 | 12,223 | 12,37 | 0,587 |
| 23 | 0,012675 | 12,675 | 12,81 | 0,575 |
| 22 | 0,013128 | 13,128 | 13,25 | 0,562 |
| 21 | 0,013581 | 13,581 | 13,69 | 0,539 |
| 20 | 0,014033 | 14,033 | 14,12 | 0,527 |
| 19 | 0,014486 | 14,486 | 14,56 | 0,514 |
| 18 | 0,014939 | 14,939 | 15,00 | 0,501 |
| 17 | 0,015392 | 15,392 | 15,44 | 0,478 |
| 16 | 0,015844 | 15,844 | 15,87 | 0,456 |
| 15 | 0,016297 | 16,297 | 16,30 | 0,443 |
| 14 | 0,01675 | 16,750 | 16,74 | 0,420 |
| 13 | 0,017202 | 17,202 | 17,17 | 0,398 |
| 12 | 0,017655 | 17,655 | 17,60 | 0,375 |
| 11 | 0,018108 | 18,108 | 18,03 | 0,352 |
| 10 | 0,01856 | 18,560 | 18,46 | 0,330 |
| 9 | 0,019013 | 19,013 | 18,89 | 0,307 |
| 8 | 0,019466 | 19,466 | 19,32 | 0,284 |
| 7 | 0,019919 | 19,919 | 19,75 | 0,261 |
| 6 | 0,020371 | 20,371 | 20,18 | 0,239 |
| 5 | 0,020824 | 20,824 | 20,61 | 0,206 |
| 4 | 0,021277 | 21,277 | 21,03 | 0,183 |
| 3 | 0,021729 | 21,729 | 21,46 | 0,211 |
| 2 | 0,022182 | 22,182 | 21,94 | 0,028 |

# Current Analogue Output Schematics (AO-1 & AO-2)



MOSFET Device Datasheet

**Electrical Characteristics** $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 10 µA | All | 60 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V | | | | 1 | µA |
| | | $T_J$=125°C | | | | 1 | mA |
| | | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | | 1 | µA |
| | | $T_J$=125°C | | | | 0.5 | mA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | | | | 10 | nA |
| | | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -15 V, $V_{DS}$ = 0 V | | | | -10 | nA |
| | | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 1) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA | | 0.8 | 2.1 | 3 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 1 | 2.1 | 2.5 | |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 500 mA | | | 1.2 | 5 | Ω |
| | | $T_J$ =125°C | | | 1.9 | 9 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 75 mA | | | 1.8 | 5.3 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 500 mA | | | 1.2 | 7.5 | |
| | | $T_J$ =100°C | | | 1.7 | 13.5 | |
| | | $V_{GS}$ = 5.0 V, $I_D$ = 50 mA | | | 1.7 | 7.5 | |
| | | $T_J$ =100C | | | 2.4 | 13.5 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 500 mA | | | 1.2 | 2 | |
| | | $T_J$ =125°C | | | 2 | 3.5 | |
| | | $V_{GS}$ = 5.0 V, $I_D$ = 50 mA | | | 1.7 | 3 | |
| | | $T_J$ =125°C | | | 2.8 | 5 | |
| $V_{DS(ON)}$ | Drain-Source On-Voltage | $V_{GS}$ = 10 V, $I_D$ = 500 mA | | | 0.6 | 2.5 | V |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 75 mA | | | 0.14 | 0.4 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 500mA | | | 0.6 | 3.75 | |
| | | $V_{GS}$ = 5.0 V, $I_D$ = 50 mA | | | 0.09 | 1.5 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 500mA | | | 0.6 | 1 | |
| | | $V_{GS}$ = 5.0 V, $I_D$ = 50 mA | | | 0.09 | 0.15 | |

# DUAL DIFFERENTIAL COMPARATORS

SLCS005K – JUNE 1976 – REVISED JUNE 2002

## electrical characteristics at specified free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$† | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = 5 V to 30 V, $V_O$ = 1.4 V, $V_{IC}$ = $V_{IC(min)}$ | | 25°C | | 2 | 5 | | 2 | 5 | mV |
| | | | | Full range | | | 9 | | | 9 | |
| $I_{IO}$ | Input offset current | $V_O$ = 1.4 V | | 25°C | | 3 | 25 | | 5 | 50 | nA |
| | | | | Full range | | | 100 | | | 250 | |
| $I_{IB}$ | Input bias current | $V_O$ = 1.4 V | | 25°C | | –25 | –100 | | –25 | –250 | nA |
| | | | | Full range | | | –300 | | | –400 | |
| $V_{ICR}$ | Common-mode input voltage range‡ | | | 25°C | 0 to $V_{CC}$–1.5 | | | 0 to $V_{CC}$–1.5 | | | V |
| | | | | Full range | 0 to $V_{CC}$–2 | | | 0 to $V_{CC}$–2 | | | |
| $A_{VD}$ | Large-signal differential-voltage amplification | $V_{CC}$ = 15 V, $V_O$ = 1.4 V to 11.4 V, $R_L$ ≥ 15 kΩ to $V_{CC}$ | | 25°C | 50 | 200 | | 50 | 200 | | V/mV |
| $I_{OH}$ | High-level output current | $V_{OH}$ = 5 V, | $V_{ID}$ = 1 V | 25°C | | 0.1 | | | 0.1 | 50 | nA |
| | | $V_{OH}$ = 30 V, | $V_{ID}$ = 1 V | Full range | | | 1 | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, | $V_{ID}$ = –1 V | 25°C | | 150 | 400 | | 150 | 400 | mV |
| | | | | Full range | | | 700 | | | 700 | |
| $I_{OL}$ | Low-level output current | $V_{OL}$ = 1.5 V, | $V_{ID}$ = –1 V | 25°C | 6 | | | 6 | | | mA |
| $I_{CC}$ | Supply current | $R_L$ = ∞ | $V_{CC}$ = 5 V | 25°C | | 0.8 | 1 | | 0.8 | 1 | mA |
| | | | $V_{CC}$ = 30 V | Full range | | | 2.5 | | | 2.5 | |

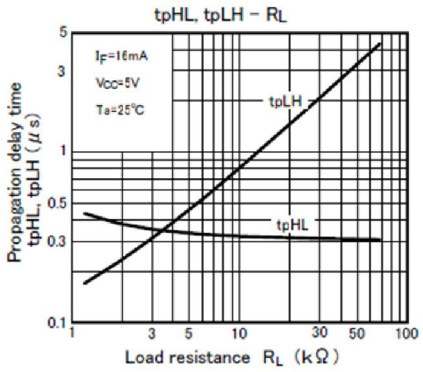
# Optocoupler Device Datasheet

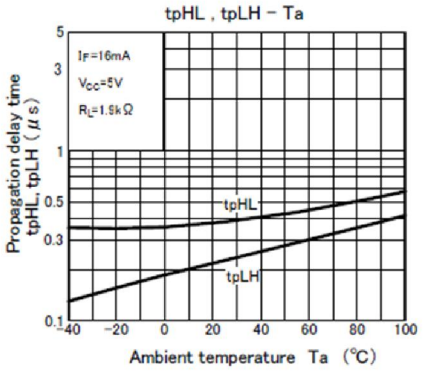
## Electrical Characteristics (Ta = 25 °C)

| | Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| LED | Forward voltage | $V_F$ | $I_F$ = 16 mA | | 1.65 | 1.85 | V |
| LED | Forward voltage Temperature coefficient | $\Delta V_F / \Delta Ta$ | $I_F$ = 16 mA | — | −2 | — | mV / °C |
| LED | Reverse current | $I_R$ | $V_R$ = 5 V | — | — | 10 | μA |
| LED | Capacitance between terminals | $C_T$ | $V_F$ = 0 V , f = 1 MHz | — | 45 | — | pF |
| Detector | HIGH-level output current | $I_{OH\ (1)}$ | $I_F$ = 0 mA , $V_{CC}$ = $V_O$ = 5.5 V | — | 3 | 500 | nA |
| Detector | HIGH-level output current | $I_{OH\ (2)}$ | $I_F$ = 0 mA , $V_{CC}$ = 30 V $V_O$ = 20 V | — | — | 5 | μA |
| Detector | HIGH-level output current | $I_{OH}$ | $I_F$ = 0 mA , $V_{CC}$ = 30 V $V_O$ = 20 V, Ta = 70 °C | — | — | 50 | μA |
| Detector | HIGH-level supply current | $I_{CCH}$ | $I_F$ = 0 mA , $V_{CC}$ = 30 V | — | 0.01 | 1 | μA |
| Detector | Supply voltage | $V_{CC}$ | $I_{CC}$ = 0.01 mA | 30 | — | — | V |
| Detector | Output voltage | $V_O$ | $I_O$ = 0.5 mA | 20 | — | — | V |

## Switching Characteristics (Ta = 25 °C, $V_{CC}$ = 5 V)

| Characteristic | Symbol | Test Circuit | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time (H→ L) | $t_{pHL}$ | Fig1 | $I_F$ = 0→ 16 mA $R_L$ = 1.9kΩ | — | — | 0.8 | μs |
| Propagation delay time (L→ H) | $t_{pLH}$ | Fig1 | $I_F$ = 16→ 0 mA $R_L$ = 1.9kΩ | — | — | 0.8 | μs |
| Common mode transient immunity at logic HIGH output (Note 8) | $CM_H$ | Fig2 | $I_F$ = 0 mA $V_{CM}$ = 400 Vp−p $R_L$ = 1.9kΩ | 10000 | — | — | V / μs |
| Common mode transient immunity at logic LOW output (Note 8) | $CM_L$ | Fig2 | $I_F$ = 16 mA $V_{CM}$ = 400 Vp−p $R_L$ = 1.9 kΩ | −10000 | — | — | V / μs |



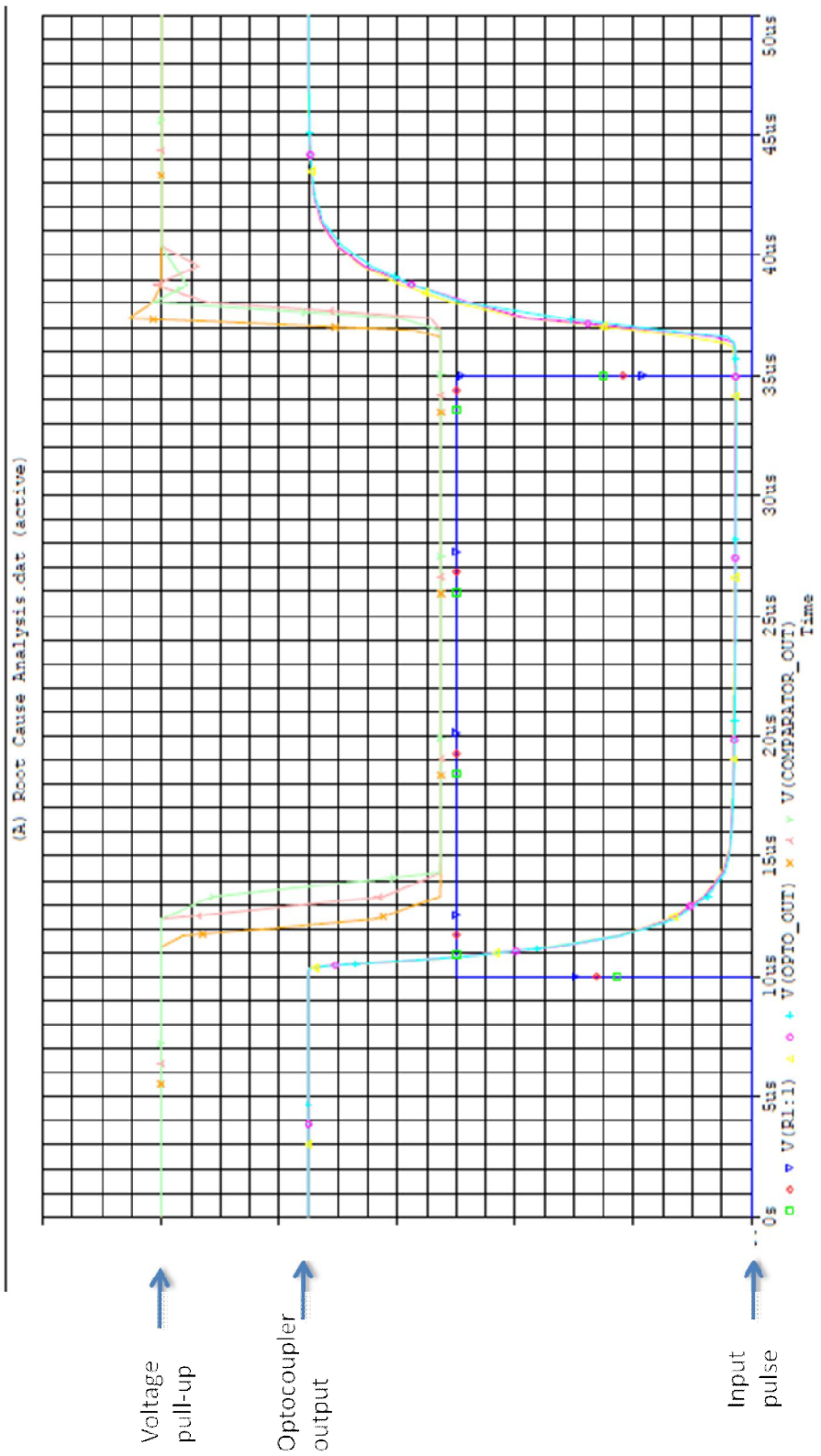
Operational Amplifier Device Datasheet

## Electrical Characteristics (Continued)

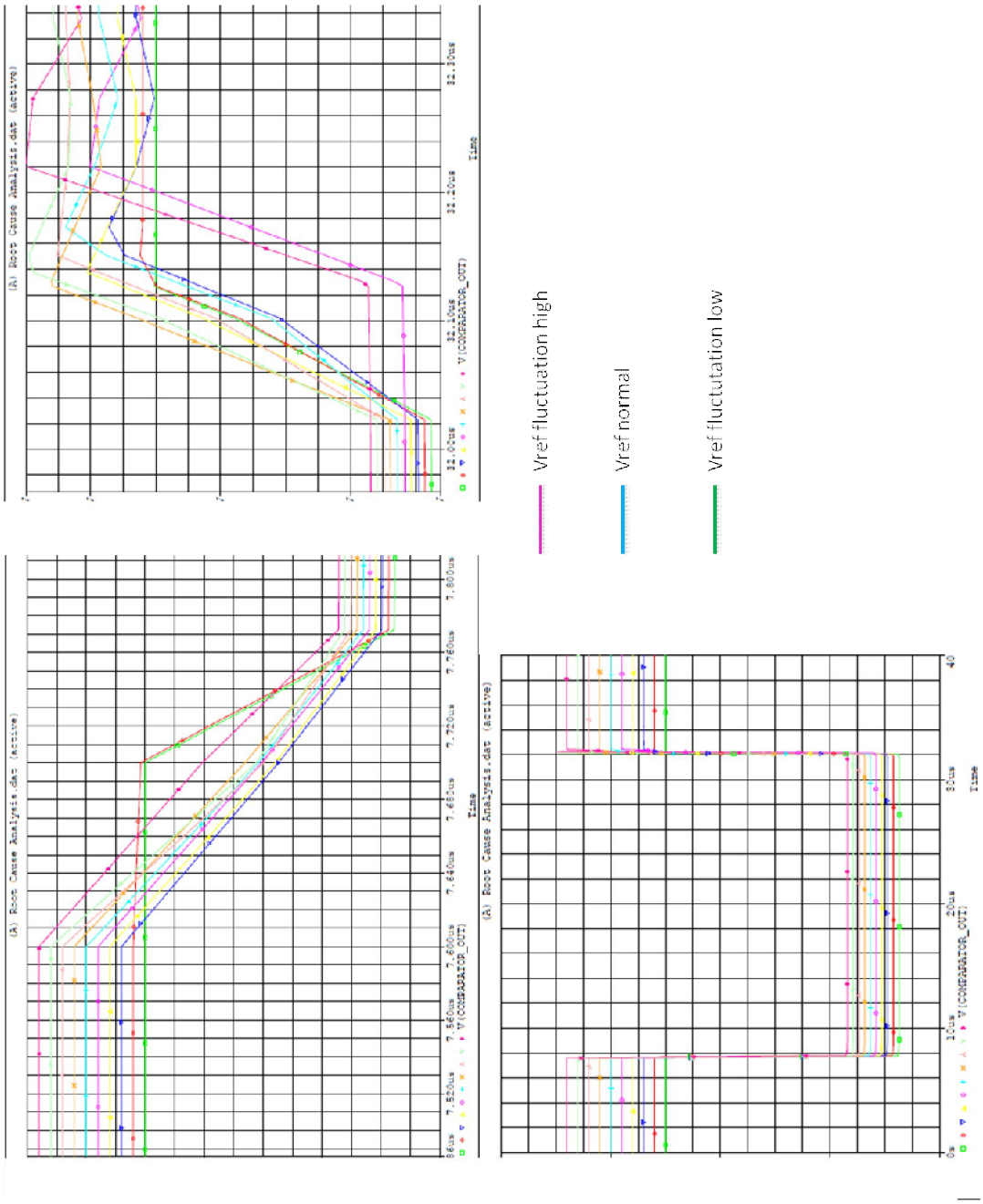
$V^+$ = +5.0V, (Note 7), unless otherwise stated

| Parameter | | Conditions | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Supply Current | | Over Full Temperature Range<br>$R_L = \infty$ On All Op Amps<br>$V^+ = 30V$ $V^+ = 26V$)<br>$V^+ = 5V$ | | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | | 1.5<br>0.7 | 3<br>1.2 | mA |
| Large Signal Voltage Gain | | $V^+ = 15V$, $R_L \geq 2k\Omega$, ($V_O$ = 1V to 11V), $T_A = 25°C$ | | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |
| Common-Mode Rejection Ratio | | DC, $V_{CM}$ = 0V to $V^+ - 1.5V$, $T_A = 25°C$ | | 70 | 85 | | 65 | 85 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | | $V^+$ = 5V to 30V<br>$V^+$ = 5V to 26V),<br>$T_A = 25°C$ | | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |
| Amplifier-to-Amplifier Coupling (Note 11) | | f = 1 kHz to 20 kHz, $T_A = 25°C$<br>(Input Referred) | | | −120 | | | −120 | | | −120 | | dB |
| Output Current | Source | $V_{IN}^+ = 1V$, $V_{IN}^- = 0V$,<br>$V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$ | | 20 | 40 | | 20 | 40 | | 20 | 40 | | mA |
| | Sink | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$,<br>$V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$ | | 10 | 20 | | 10 | 20 | | 10 | 20 | | |
| | | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$,<br>$V^+ = 15V$, $V_O$ = 200 mV, $T_A = 25°C$ | | 12 | 50 | | 12 | 50 | | 12 | 50 | | µA |
| Short Circuit to Ground | | (Note 5) $V^+ = 15V$, $T_A = 25°C$ | | | 40 | 60 | | 40 | 60 | | 40 | 60 | mA |
| Input Offset Voltage | | (Note 8) | | | | 7 | | | 9 | | | 10 | mV |
| $V_{OS}$ Drift | | $R_S = 0\Omega$ | | | 7 | | | 7 | | | 7 | | µV/°C |
| Input Offset Current | | $I_{IN(+)} - I_{IN(-)}$, $V_{CM}$ = 0V | | | | 100 | | | 150 | | 45 | 200 | nA |
| $I_{OS}$ Drift | | $R_S = 0\Omega$ | | | 10 | | | 10 | | | 10 | | pA/°C |
| Input Bias Current | | $I_{IN(+)}$ or $I_{IN(-)}$ | | | 40 | 300 | | 40 | 500 | | 40 | 500 | nA |
| Input Common-Mode Voltage Range (Note 10) | | $V^+$ = +30V<br>$V^+$ = 26V) | | 0 | | $V^+-2$ | 0 | | $V^+-2$ | 0 | | $V^+-2$ | V |
| Large Signal Voltage Gain | | $V^+$ = +15V ($V_O$Swing = 1V to 11V)<br>$R_L \geq 2$ kΩ | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_{OH}$ | $V^+$ = 30V | $R_L$ = 2 kΩ | 26 | | | 26 | | | 22 | | | V |
| | | $V^+$ = 26V) | $R_L$ = 10 kΩ | 27 | 28 | | 27 | 28 | | 23 | 24 | | |
| | $V_{OL}$ | $V^+$ = 5V, $R_L$ = 10 kΩ | | | 5 | 20 | | 5 | 20 | | 5 | 100 | mV |
| Output Current | Source | $V_O$ = 2V | $V_{IN}^+$ = +1V,<br>$V_{IN}^-$ = 0V,<br>$V^+$ = 15V | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | Sink | | $V_{IN}^-$ = +1V,<br>$V_{IN}^+$ = 0V,<br>$V^+$ = 15V | 5 | 8 | | 5 | 8 | | 5 | 8 | | |

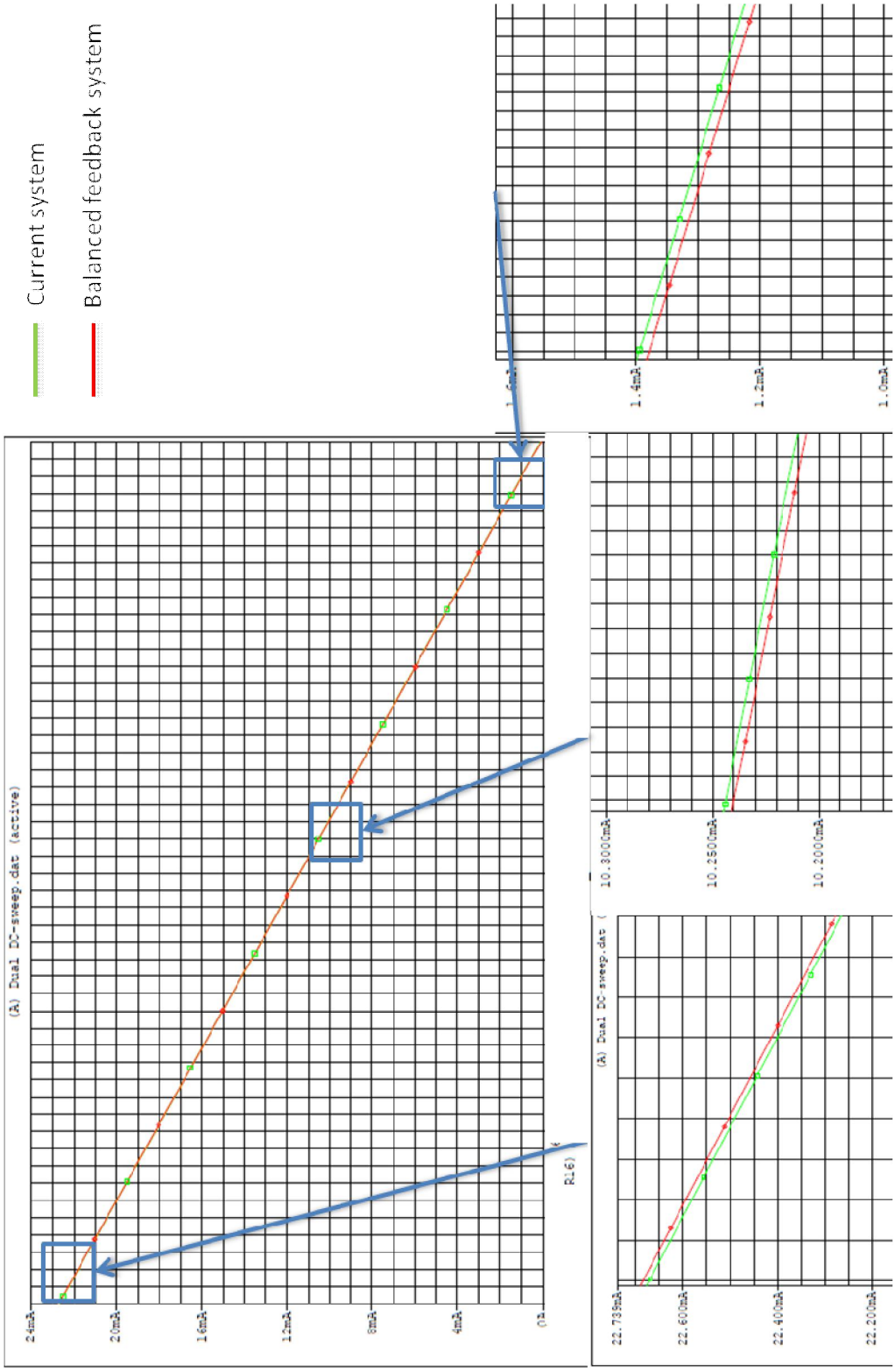
# Temperature Simulation Results



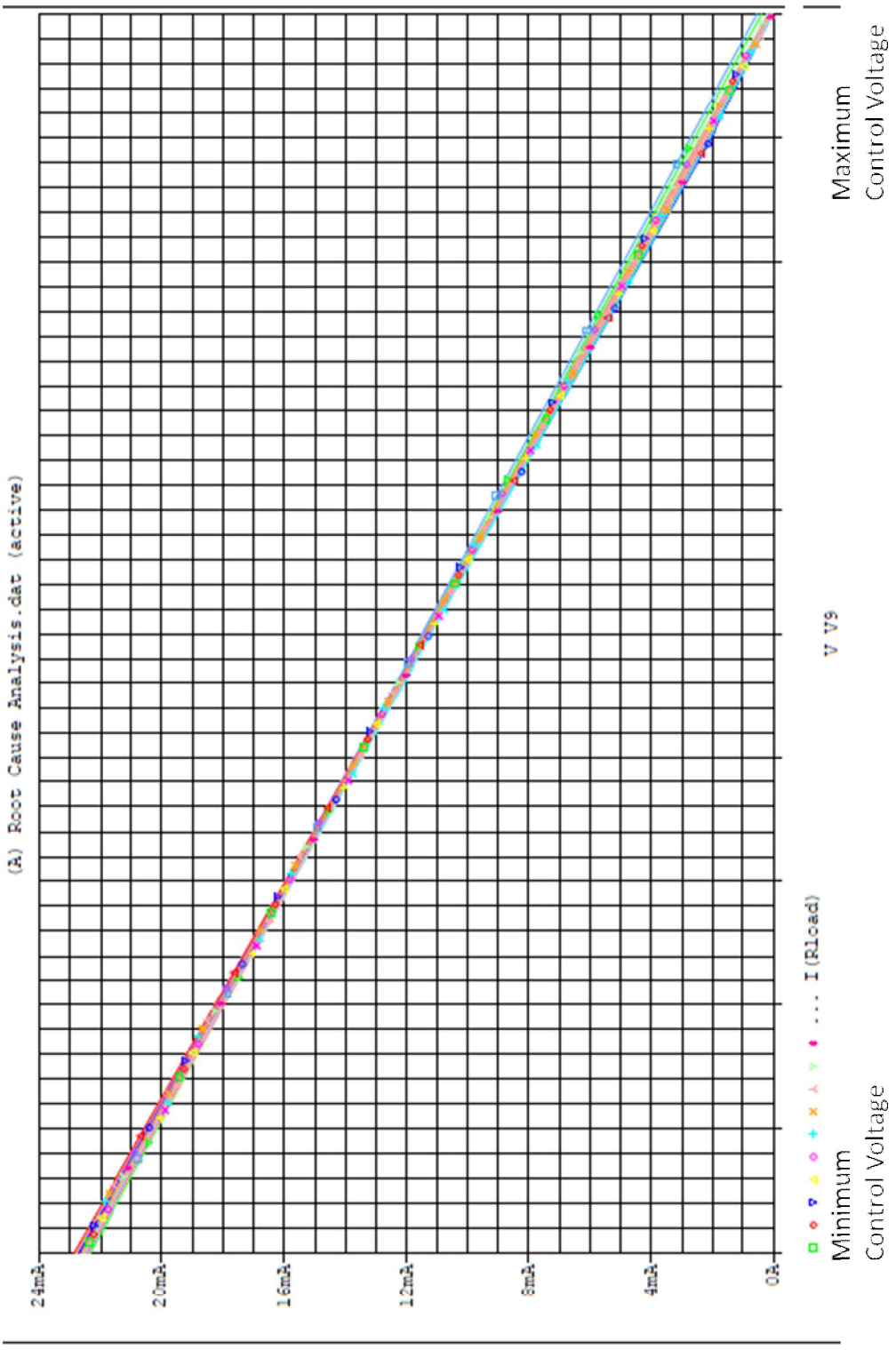
# Voltage Pull-up Reference Voltage Simulation Results



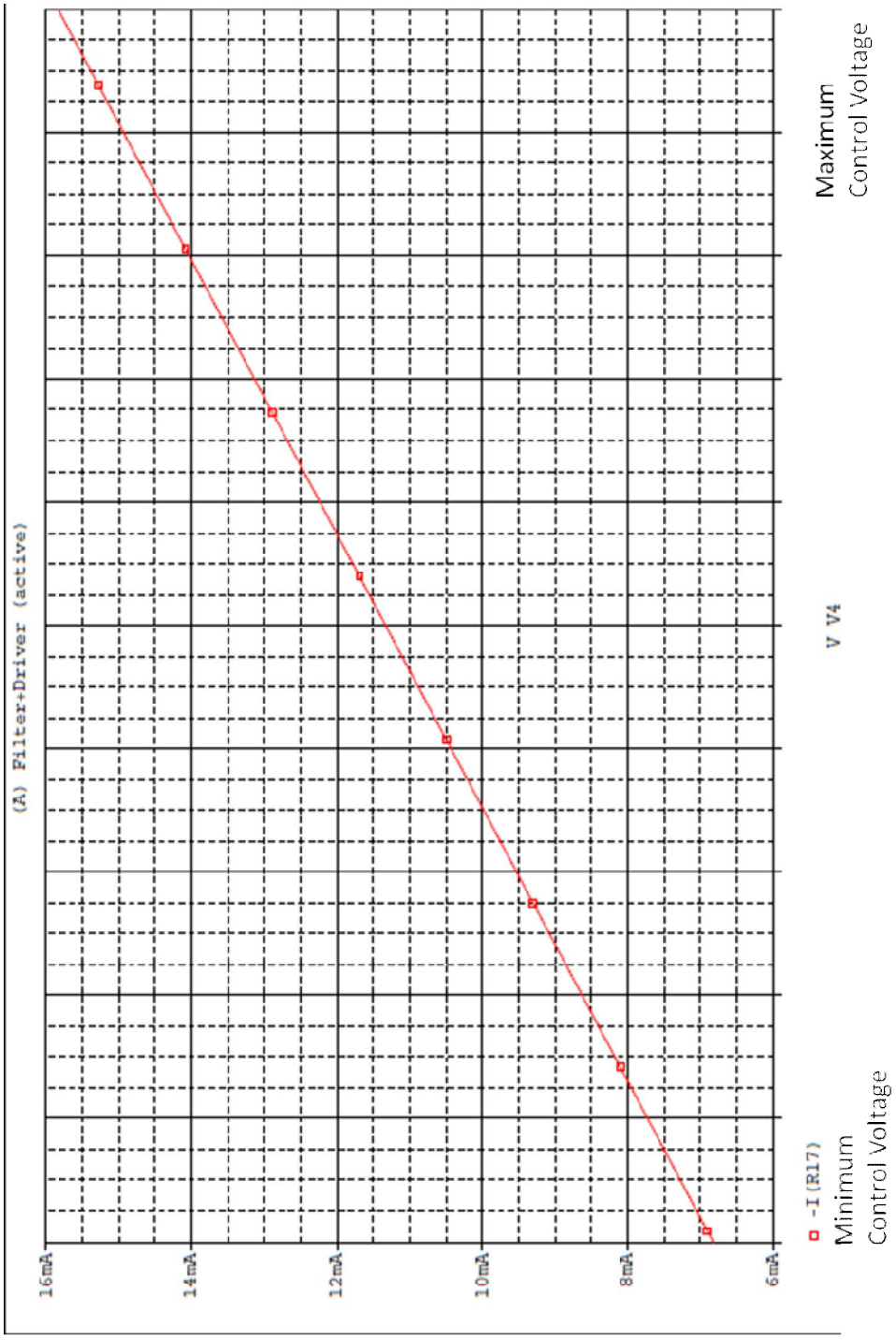
# Balanced Feedback in Comparison to Current Output Stage



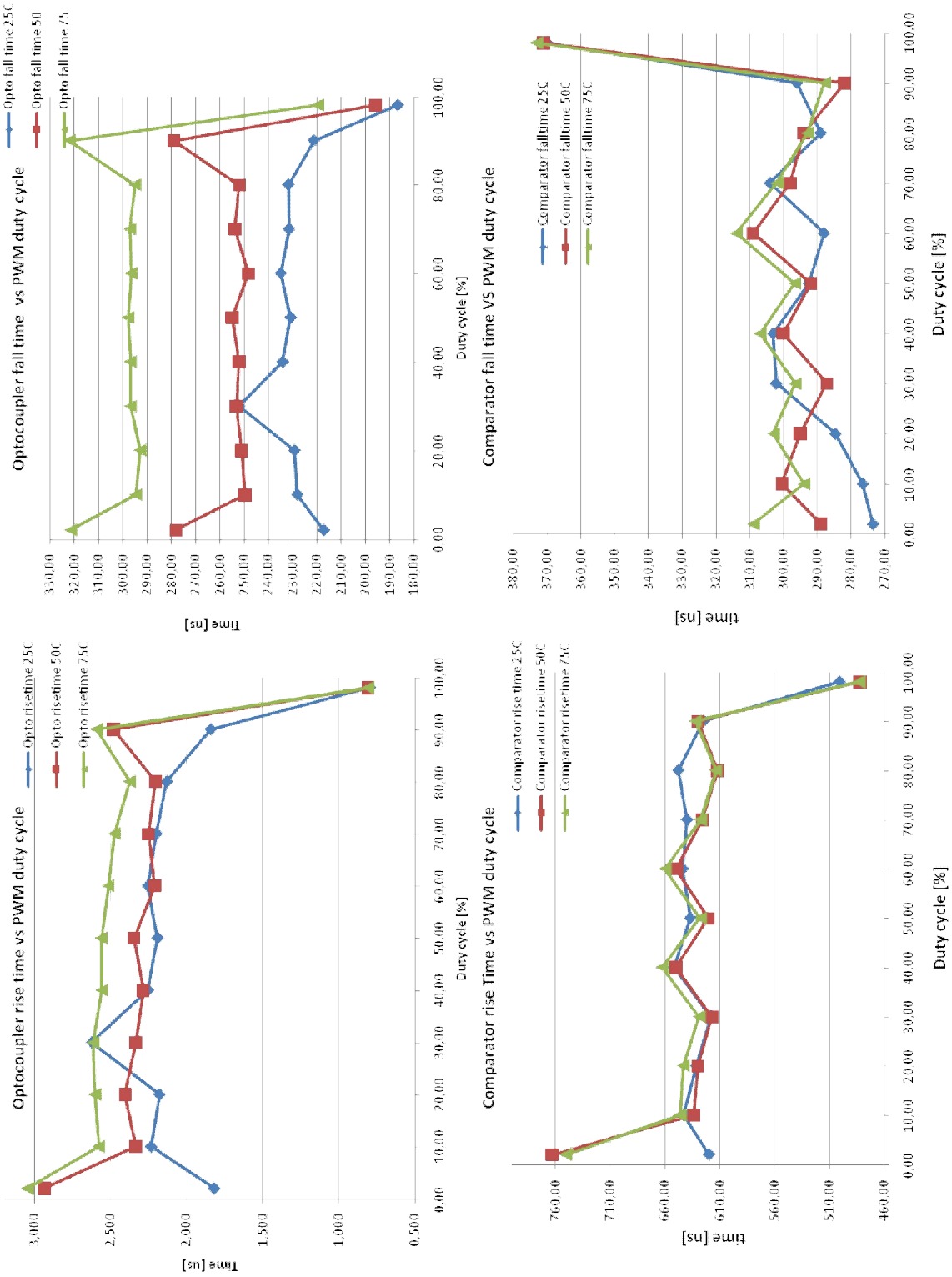
# Output Stage Unity Form Monte Carlo Simulation Results



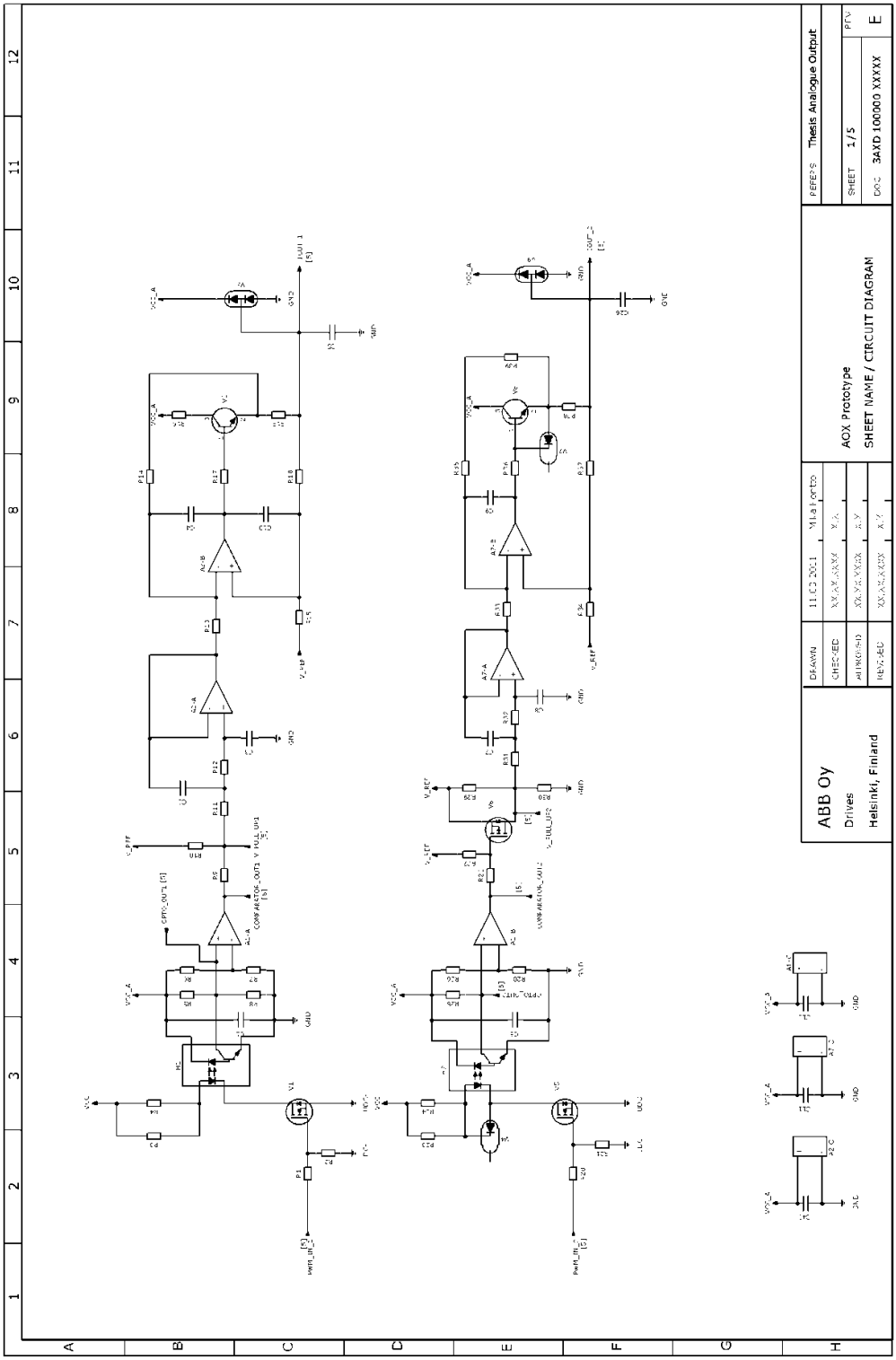
# Output Stage Reference Voltage Simulation Results



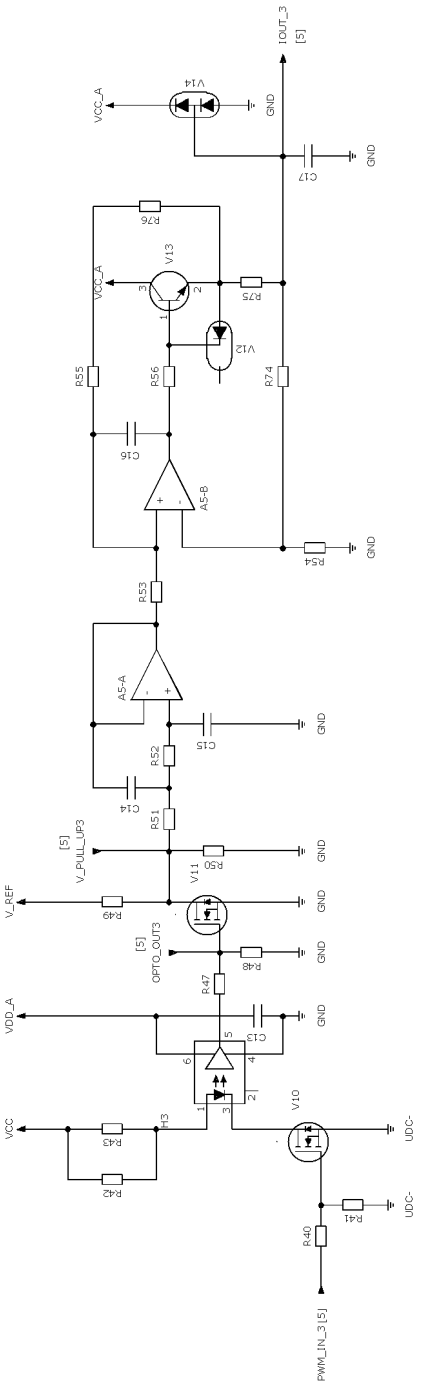
# Thermal Measurement Pulse Behaviour Data



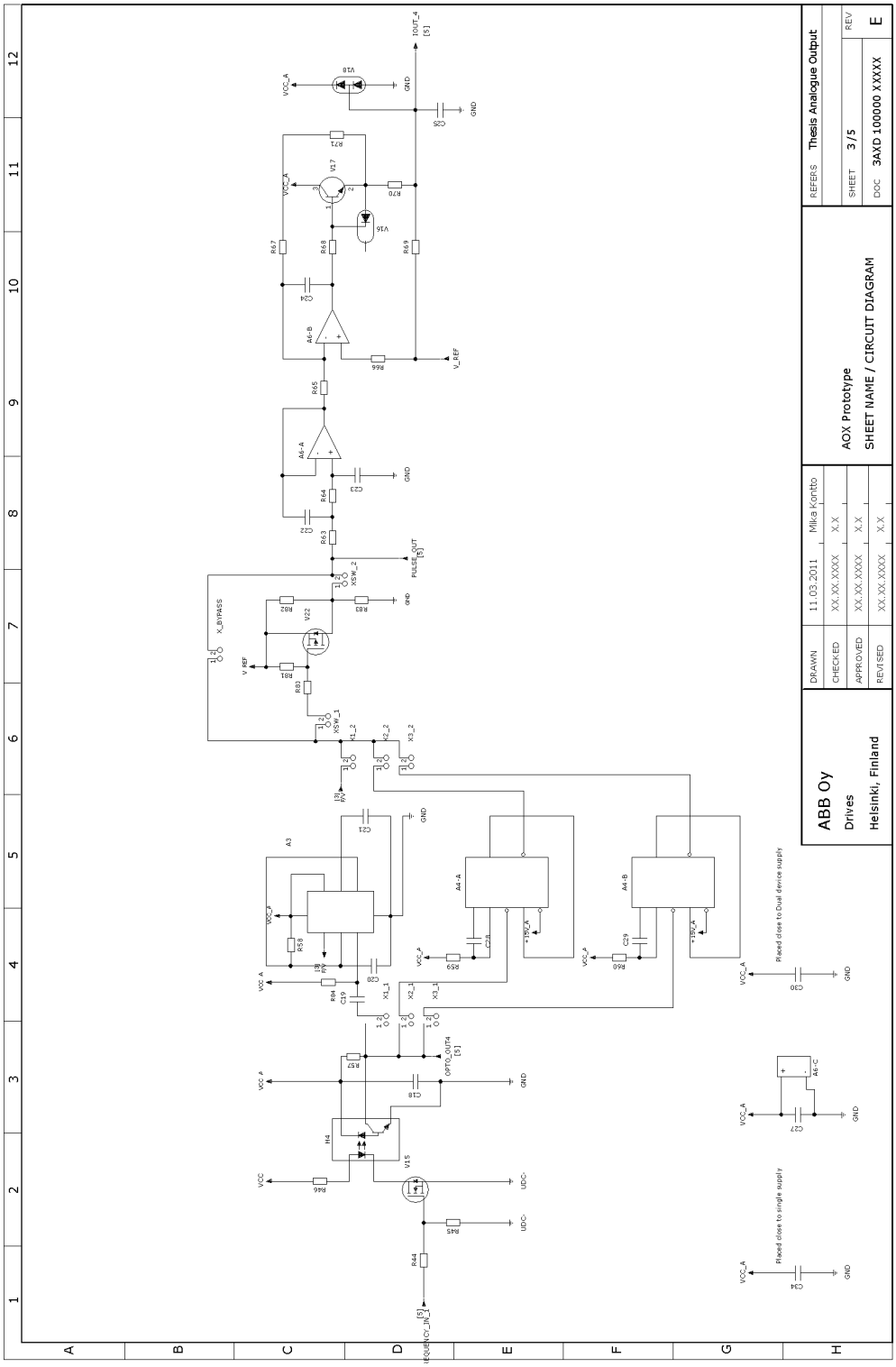
Prototype Schematics (Old AO-1 above and Solution 1 below)



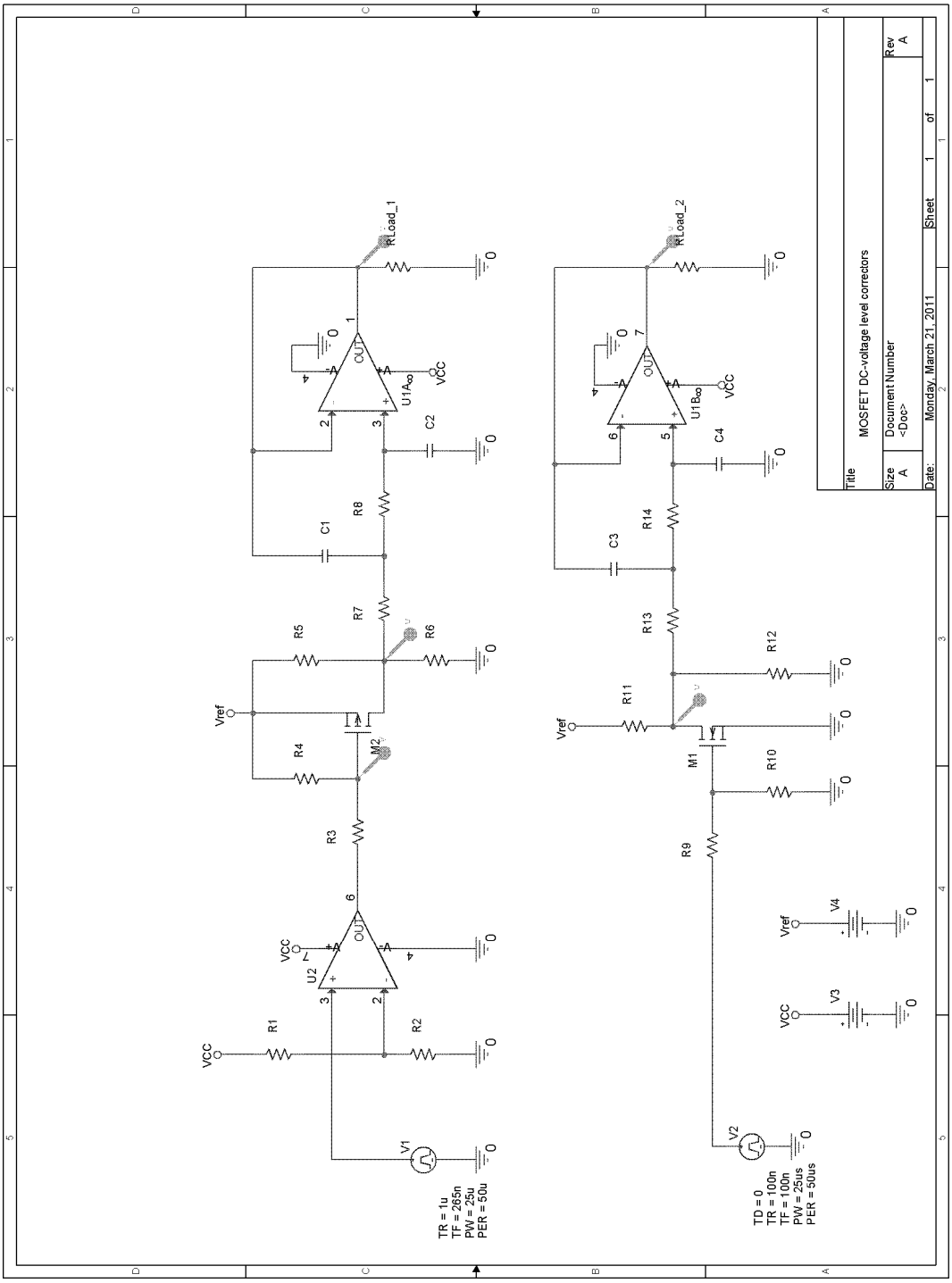
Prototype Schematics (Solution 2)



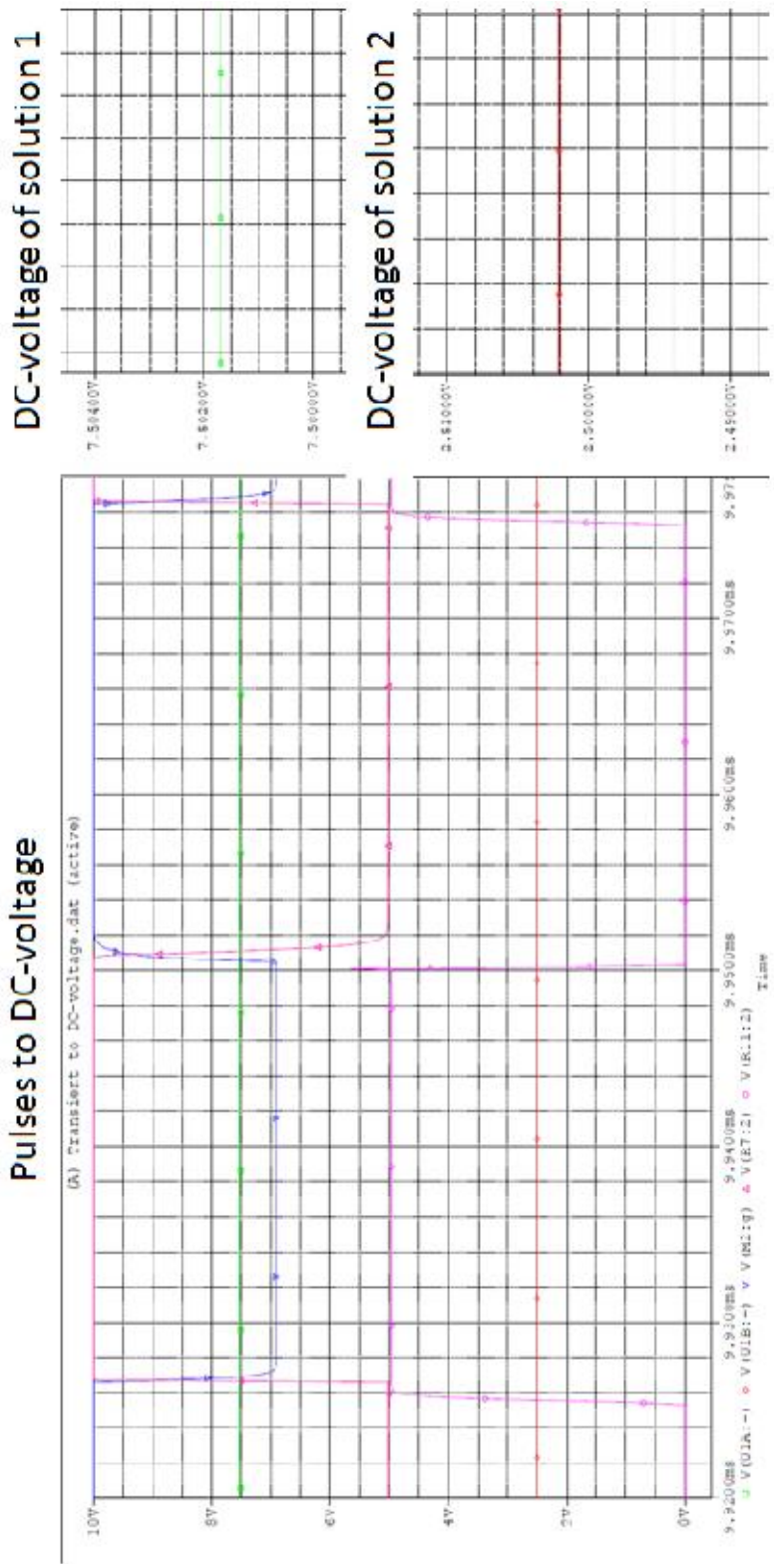
Prototype Schematics (Solution 3.1 device above, 3.2-3.3 device below)



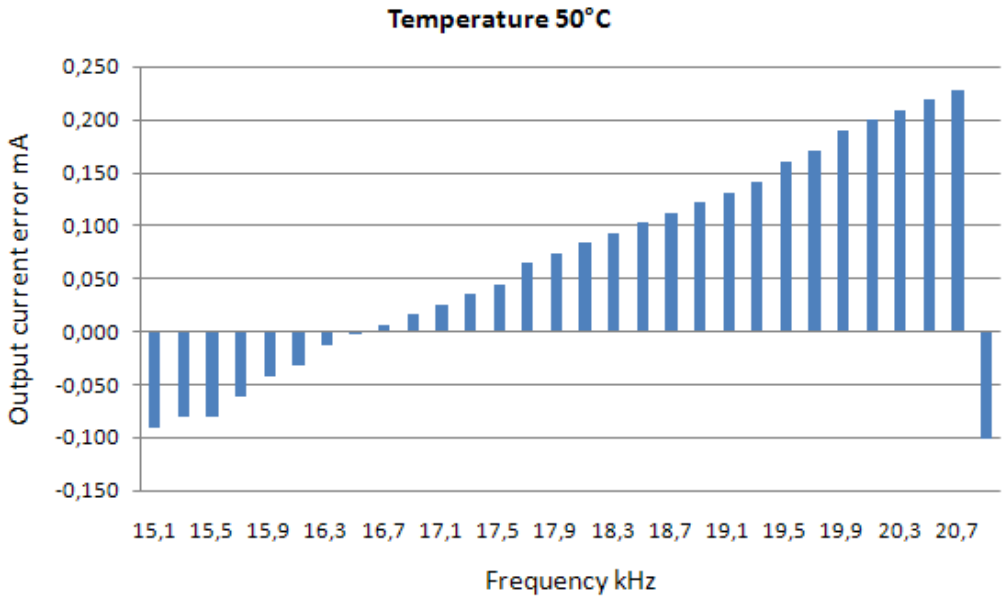
# Prototype MOSFET DC-corrector Simulation Setup

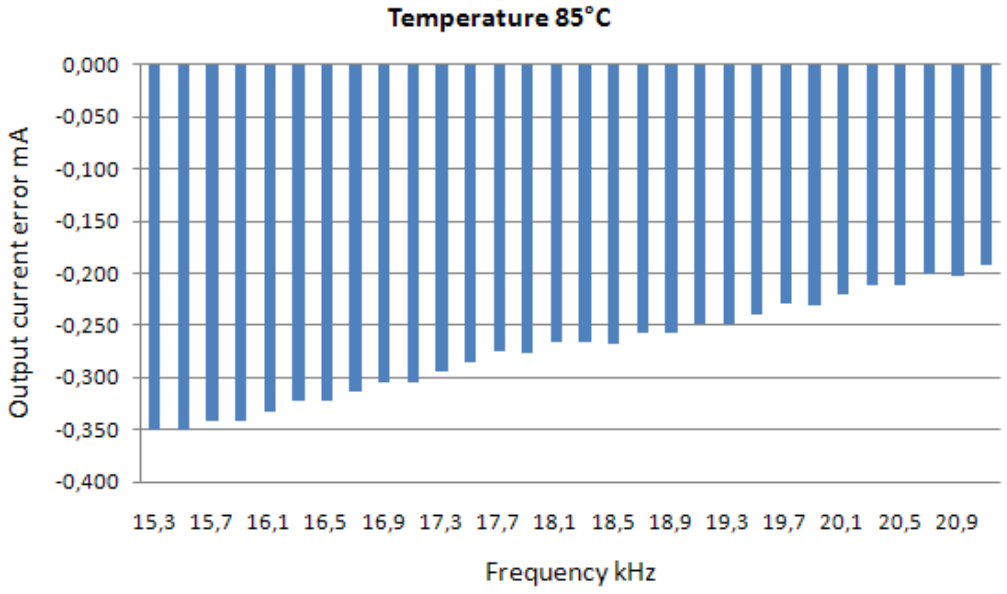


MOSFET-Switch Simulation Results



Stabilized Operation of Solution 3.2 in Thermal measurement



Estimated Component Costs

Estimated Component Cost

| | Digikey Component | Order minimum amount | Price 1pc / USD |
|---|---|---|---|
| Passive: | Resistor (1%, 100ppm) | 10 000 pcs | 0,04 |
| | Capacitor (+/-5%) | 4000 pcs | 0,004 |
| Active: | Operational Amplifier (dual) | 2500 pcs | 0,17 |
| | Comparator (Dual) | 2500 pcs | 0,11 |
| | MOSFET N-Channel | 3000 pcs | 0,04 |
| | Bipolar Transistor NPN | 3000 pcs | 0,03 |
| | Diode | 3000 pcs | 0,03 |
| | Diode (protection) | 3000 pcs | 0,04 |
| | Zener diode | 3000 pcs | 0,03 |
| | Optocoupler (current device) | 1500 pcs | 0,83 |
| | Optocoupler (upgraded device) | 1500 pcs | 0,83 |
| | Single timing device | 2500 pcs | 0,29 |
| | Dual timing device | 2500 pcs | 0,32 |

# Estimated Solution Cost

Estimated Solution Cost

| Component | Old solution | | Solution 1 | | Solution 2 | | Solution 3.1 | | Solution 3.2-3 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Amount | Price | Amount | Price | Amount | Price | Amount | Price | Amount | Price |
| Resistor (1%, 100ppm) | 19 | 0,76 | 20 | 0,8 | 17 | 0,68 | 15 | 0,6 | 14 | 0,56 |
| Capacitor (+/-5%) | 7 | 0,03 | 7 | 0,03 | 6 | 0,02 | 10 | 0,04 | 8 | 0,03 |
| | | | | | | | | 0 | | 0 |
| Operational Amplifier (dual) | 1 | 0,17 | 1 | 0,17 | 1 | 0,17 | 1 | 0,17 | 1 | 0,17 |
| Comparator (Dual) | 1 | 0,11 | 1 | 0,11 | 0 | 0 | 0 | 0 | 0 | 0 |
| MOSFET N-Channel | 1 | 0,04 | 2 | 0,08 | 2 | 0,08 | 1 | 0,04 | 1 | 0,04 |
| Bipolar Transistor NPN | 1 | 0,03 | 1 | 0,03 | 1 | 0,03 | 1 | 0,03 | 1 | 0,03 |
| Diode | 0 | 0 | 2 | 0,06 | 1 | 0,03 | 1 | 0,03 | 1 | 0,03 |
| Diode (protection) | 1 | 0,04 | 1 | 0,04 | 1 | 0,04 | 1 | 0,04 | 1 | 0,04 |
| Zener diode | 0 | 0 | 0 | 0 | 1 | 0,03 | 0 | 0 | 0 | 0 |
| Optocoupler (current) | 1 | 0,83 | 1 | 0,83 | 0 | 0 | 1 | 0,83 | 1 | 0,83 |
| Optocoupler (upgraded) | 0 | 0 | 0 | 0 | 1 | 0,83 | 0 | 0 | 0 | 0 |
| Single timing device | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0,29 | 0 | 0 |
| Dual timing device | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0,32 |
| | Total: 32 | 2,01 | Total: 36 | 2,15 | Total: 31 | 1,91 | Total: 32 | 2,07 | Total: 29 | 2,05 |