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Reliability Assessment of Millimetre Wave Components for Space Applications

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This thesis was aimed at the objective of designing and producing reliability measurement for millimetre wave components that are designed for high frequencies. The components are designed to function in frequency levels from 70 GHz to 100 GHz. In the design parameters it was taken into consideration that the components may be used in space applications.

The project highlight was testing whether MilliLab – VTT has the capability to run reliability measurements fluently. The first chapters will go through various technologies involved with components under measurements. Next the specific theoretical background is introduced that effect reliability. The theory of radio frequency measurements is also introduced.

The test setup was custom designed for this specific project to introduce the basic idea behind running a reliability measurement. Test was combined with using both a temperature step stress and burn-in reliability testing method. The sample size was small with only one chip being tested so the mathematical analysis behind analysing the probability of an error was disregarded. The test structure was successful and efficient producing results.

The conclusion of this thesis was that reliability measurement with the setup in this thesis was successful and MilliLab – VTT has sufficient capability to run a reliability measurement.

Keywords	reliability, E-band, millimetre wave, thermal step stress

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Abbreviations:

DMM – Digital Multimeter

DUT – Device under Test

ESA – European Space Association

ESCC – European Space Components Coordination

ESCIES – The European Space Components Information Exchange System

ESS – Environmental Stress Screening

FCC – Federal Communications Commission

GPIB - General Purpose Interface Bus

HEMT – high-electron-mobility transistor

IEC – International Electrotechnical Commission

IEEE – The Institute of Electrical and Electronics Engineers

ISO – The International Standards Organization Standards

LCP – Liquid Crystal Polymer

MIL-STD – United States Military Standard

MMIC – Monolithic Microwave Integrated Circuit

RF – Radio Frequency

CTE –Coefficient of Thermal Expansion

VTT – Technical Research Centre of Finland

1 Introduction

VTT Technical Research Centre of Finland and specifically its joint laboratory with Aalto University, MilliLab, has the status of ESA External Laboratory on Millimetre Wave Technology. Its specialised in micro- to sub-millimetre wave frequency measurements. MilliLab - VTT tenders and runs projects for ESA. MilliLab – VTT has a long experience in designing and testing monolithic millimetre wave integrated circuits (MMIC), like low noise amplifiers (LNA), mixers or switching circuits, for space applications. MilliLab - VTT also produces radio frequency MEMS components and circuits including switches, varactors, switched capacitors, filters, power sensors, phase shifters, impedance tuners and matching networks. The newly researched and developed components are then tested in their own laboratories to make sure they are hundred percent suitable for use in space.

Reliability assessment is a continuous process and key element during designing and manufacturing components and systems to be used in space. Different variables have to be taken into account when moved away from the protective atmosphere and climate of planet Earth. The same principles do not always hold true when operating in an almost airless and extremely cold environment. With expensive projects taking years to prepare there is no room for error and extreme precautions must be taken. On top of this power consumption, sensitivity and accuracy have to be taken in careful measure. To make sure product design goals are met perfectly tests must be come up to simulate the harsh environment encountered in space. The testing concept that is used to achieve these goals are referred to as the reliability assessment or space qualification and includes different testing methods in radio frequency, temperature cycling, mechanical stress tests, operational tests and electrical tests.

This thesis concentrates on radio frequency and thermal step stress tests for LCP substrate mounted flip-chip RF SP4T switch in 70GHz to 90GHz range, to test, find and prove, if accelerated aging caused by increased temperature can degrade the chip quality in radio frequency tests.

This thesis is arranged as follows:

The first chapter of the thesis introduces the research concept and more specific focus of the project.

In the second chapter of the thesis the basic idea behind reliability tests are explained. The code of conduct with standards and the project guidelines followed for running the test campaigns will be presented.

The third chapter of the thesis will explain the various semiconductor technologies that are involved in this project and the theory behind them. These include the technologies of HEMT transistor, PIN diode, operating principle of diode and operation of an RFIC switch. The liquid crystal polymer substrate material and its properties are looked into also. The chapter will conclude introducing the test setup and the device under test.

The fourth chapter will include the complete explanation of the test operation with short review on the results.

In the chapter five the test results are explained and analysed. A conclusion is made based on the results.

The sixth chapter will shortly review the test campaigns accuracy and quality, presenting the conclusion of the whole thesis. Improvements are suggested through critiquing different steps of the test.

2 Reliability Measurements

2.1 Reliability

By definition reliability is:

> *An attribute of any system that consistently produces the same results, preferably meeting or exceeding its specifications.* [1]

By definition reliability means that any system always behaves the same way under the same conditions without the performance decreasing by time or after continuous repetition of the process. Reliability is an important factor in the design of electrical components because it affects the manufacturing process. [2] Manufacturing a small batch of R&D components to be tested is usually made with high precision and monitoring. When the same product is moved to mass production and it is not possible to monitor and take away all parts that appear faulty the quality may experience a great degradation. Reliability also limits the usage of the product to certain areas where it has been found by testing and experience to be reliable. The limiting design and usage rules for components usability in different fields of electronics and industry are called standards.

Standards are used to assure safety and reliability when all products are designed under the same guidelines. Standards support setting policies and legislation so that products can be more easily supervised and inspected to be user-friendly and safe. Interoperability of products is made possible by the use of standards. Without standards every company would have to invent their own way of designing and manufacturing devices which could severely harm their interoperability. Products following standards allow more room for innovation and adding new features to designs as all are designed by the same guidelines. It requires new resourceful thinking to “break the boundaries” of these guidelines. Standards give a good basis to start building new innovations on. With interoperability between different products the standards ease consumer choice as they can easily compare the product specifications.

After a product is first designed to follow the industry standard, it has to be tested next. The standards also help in designing the test parameters, for they include accurate specifications that the product should follow. Standardized tests are usually designed to make sure that products are fail-safe against most hazardous malfunctions hampering user reliability or causing hazards for the user.

Standards in electronics industry are maintained and supervised by official associations including: IEC, ESCC, MIL, FCC, and SAE. This document concentrates on the topic of electronics in space which is controlled mainly by ESCC and MIL standards.

2.2 Reliability in Electronics Industry

Reliability testing focuses on improving the product. Testing a product, so that its weak points may be found, can develop it towards a more perfect application. Usually the life cycle of electrical components may be thought as a three-step process: design, manufacturing and operation. Within all of these there are risks that have to be considered and handled. There are three commonly used analysis methods to estimate product reliability: destructive physical analysis, failure analysis and a newer method called construction analysis. [3]

The component features are the first requirements to consider. Usually these requirements include specifications for the size, power consumption, frequency range, impedance and electrical matching. Other requirements that should be also taken into account on top of these electrical properties are the ones that affect the next two steps of the component life cycle. In manufacturing electrical components mass production is usually required to suffice the need of buyers and to make up for the manufacturing and design costs of the products. In manufacturing there are three crucial parameters that are constantly followed: quality, product manufacturing price and manufacturing process time. The final process step, operation, brings a third dimension to component design and therefore reliability. When components are moved away from the manufacturing line, they are first tested that they operate reliably according to their design. After the testing the products are sent to customers, and they are put into use. Here the components meet their final challenges. The challenges in the use of components involve requirements to be taken into account in the design flow. These requirements are: operating temperature, power consumption in the operation temperature, component life time, environmental stresses, electromagnetic distortion, radiation, humidity. To counteract most of these factors the device packaging should be designed so that it protects the most important parts from malfunctions and failures.

The importance of reliability assessment and risk evaluation require even greater consideration when the component is moved to an environment like space. A saying: “get it

right the first time because there are no repairmen in space" - Mike Bernico, MRI head design manager, General Electric - is no understatement when speaking of applications in space. This is why the importance of accurate and diverse reliability tests has a huge role in successful space projects.

2.3 Test Campaign Project

The European Space Agency (ESA) is a big project and funding provider in Europe considering space endeavours. ESA publishes and designs project outlines after which a competitive tendering takes place between facilities capable of completing the projects. The facilities present their own suggestion according to the guidelines how the project is supposed to be carried. Then ESA selects and approves the suggestions and gives the project to the most suitable facility. This thesis is based on testing a flip-chip SP4T switch component that was used in a VTT project to control electrical beam steering of a lens antenna for W-band. [4] The tests performed at this thesis and their design was meant to function as preparatory investigation for an upcoming project. For this motivation the thesis uses as it's guideline to design and run reliability tests the upcoming project document made by MilliLab - VTT.

2.3.1 Running the Test Campaign

The test designed and performed in this thesis was designed to find hidden or unknown failures during a temperature step stress test for a component already in use in an application that was published in a paper [4]. In the application this type of switches are being used to select a feed array element from a radio antenna lens to produce the main beam of transmission in the element relative direction. The difference between the application described in [4] and the circuit under test was that the application was assembled on a LTCC substrate and the test circuit on a LCP substrate. A different substrate has different thermal and radio frequency properties, and because of this the circuit required a temperature stress test. The test was run at MilliLab - VTT test laboratory. The test was conducted by inflicting an increasing thermal stress in steps and testing the radio frequency parameters before and after each step. During the thermal stress the device under test (DUT, a SP4T switch) was biased to activate the active semiconducting diodes inside the component.

3 Materials and Technologies at Millimetre Wave Frequencies

The materials and measurement equipment is highly involved with determining the reliability of the product. The reliability is in everything for the failures may occur anywhere. To be able to understand where the failures may occur, different sides and aspects of the device under test must be inspected. The focus will be on active components. Reliability for passive components like resistors and capacitors is as important as with active, but many manufacturers offer passive components qualified for use in space. Availability for active components qualified for use in space is limited, and usually the user must verify their reliability. Naturally this is the case when the components are designed by the user. MMIC-circuits designed by MilliLab – VTT are typically designed with transistor and diodes for the particular waveband in use. MEMS components are left outside of this thesis.

3.1 MMIC HEMT and PIN Technologies

The active components in millimetre wave frequencies are based on diodes and transistors like in more traditional electronics. As the active components are designed and manufactured in more traditional electronics to make integrated circuits and MMIC's. The same type of components may be used to make integrated circuits in millimetre wave bands, so-called MMIC stands for monolithic microwave integrated component. The name is quite self-explanatory. The main characteristic of a MMIC also known as "mimic" is that its size is small and suitable for millimetre wavelength. The monolithic means that the part is fabricated out of one piece of semiconductor material (Gallium Arsenide (GaAs) or Silicon Germanium (SiGe)) which contains all the functionalities of the component, and because it may be easily attached to substrates.

When the frequency becomes higher and the wavelength grows shorter more concentration should be given to details because the factors that usually cause operational errors become smaller as the size of components grows smaller and are harder to notice. The following sections introduce typical active component technologies at micro- and millimetre wave frequencies and methods and instruments relevant for their testing.

3.1.1 HEMT transistors

HEMT is an abbreviation for high-electron-mobility transistor, which is used often in MMICs. It is a special application of a field-effect transistor but the structure how it is built is different due to doped conduction band E_c inside. The structure of a HEMT is shown in the Figure 1. The higher mobility of electrons is achieved by a creation of a two dimensional electron gas (2DEG) which creates the channel where electrons now have higher mobility.

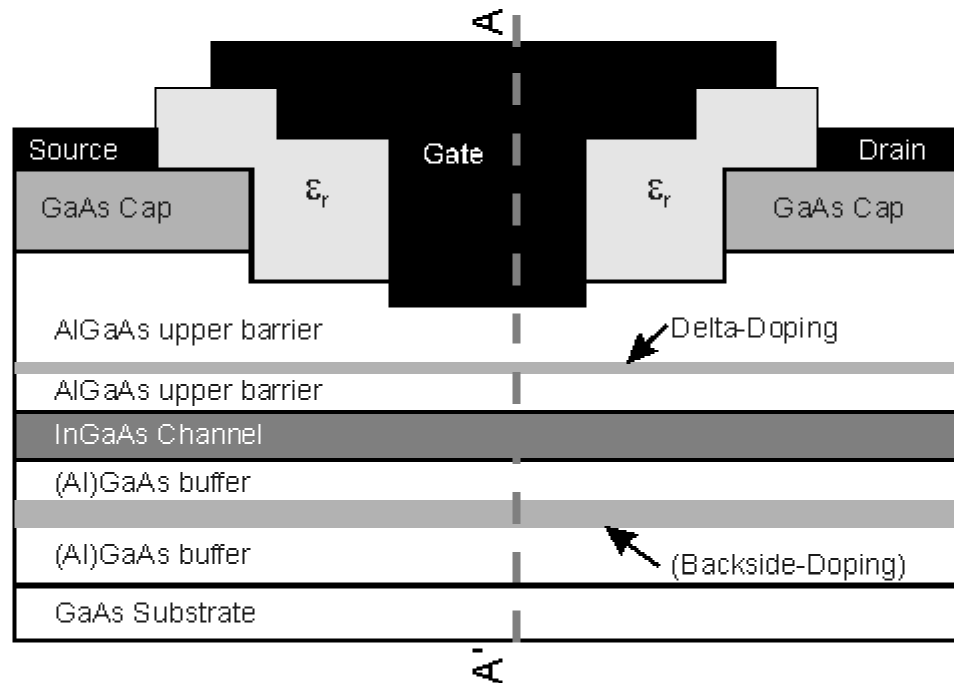

Figure 1. The structure of a GaAs HEMT reprinted from Brech 1998 [5]

Further inspection of HEMT technology is out of spec of this thesis. The basic principle behind this special FET is enough to understand the technology how the LNA chip functions.

3.1.2 PIN diodes

PIN diode is conductivity modulated diode. The basic principle is the same as with regular diode but it has a middle region that has much lower doping concentration compared to the outer p- and n-layers around it. This decreases the resistance while the diode is forward biased in the ON-state. In the DUT in this thesis, this is used to an

advantage to produce a low loss switch. On the other hand the OFF-state resistance increases due to this modulation giving the diode higher voltage blocking ability. DUT manufacturer TriQuint does not tell specifically what kind of PIN diode they are using but the basic principle is the same nonetheless. The “I”-letter in the name of PIN diode refers to the doped middle region which may be called as n^{-} layer, and also known as the intrinsic layer. Thickness of the layer may be altered by different manufacturing processes. Figure 2 shows the characteristic curve of a PIN diode.

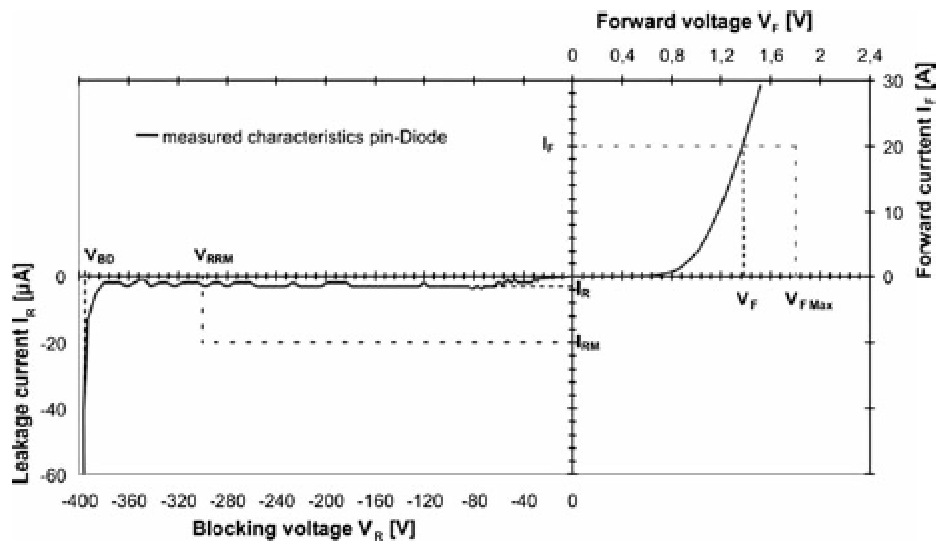

Figure 2. PIN diode characteristic I-V curve. Taken from Lutz 2011 [6]

As may be seen from the Figure 2 the blocking voltage is extremely high and the forward current may be increased to a high value with small forward voltage making the diode resistant to higher breakdown current.

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3.1.3 Diode Operating Principle

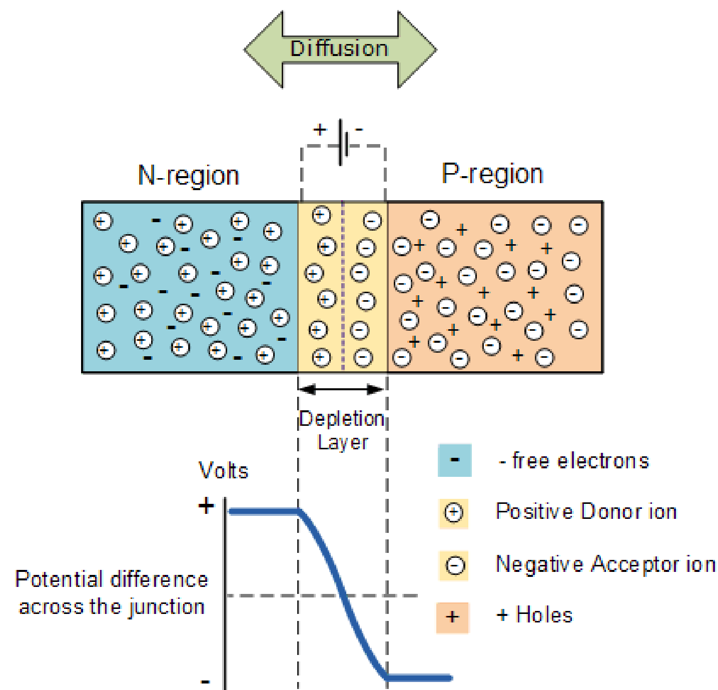

Figure 3. Presenting the pn-junction. [7]

The operation of diodes is based on the semiconducting pn-junction (Figure 3). Pn-junction is created by combining two materials with different carrier densities together. This is shown in figure 3. The potential difference between the junctions is called the threshold voltage of the diode. The threshold voltage is the potential difference that is required for the electrons to cross the depletion layer inside the semiconducting material. In practice the pn-junction is done by connecting voltage terminals to both ends of semiconducting material such as Gallium-Arsenide in the application in this thesis. Typically the threshold voltage for GaAs is 1,2V and considerably higher than with Si which is typically 0,7V. The threshold voltage and current required to drive the diode into forward conduction or reserve saturation can be found using the normalized ideal I-V characteristic curve of a pn-junction. Seen in Figure 4.

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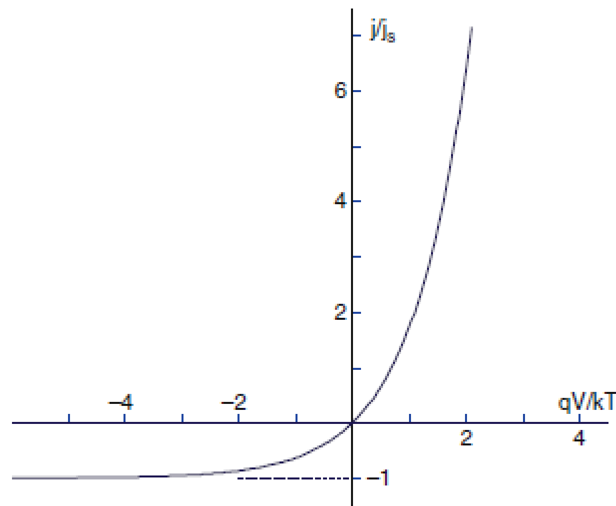

Figure 4. Normalized ideal IV-curve. Taken from Lutz 2011 [6]

To plot the curve an equation for current density is obtained by:

$$\boldsymbol{j = j_s * (e^{\frac{qV}{kT}} - 1),} \tag{3-1}$$

where j_s is the saturation current density that may be calculated by knowing the semiconductor material characteristics, k is the Boltzmann constant, T is the junction temperature, q is charge of electron, and V is the threshold voltage over the junction. For GaAs $\boldsymbol{j_s}$is typically 2.1 x $10^{-18}\frac{A}{cm^2}$. The threshold voltage of the diode may be solved by solving V from the above equation (3-1) in the point when the curve starts rising rapidly from 1 to ∞. In the Figure 4 above, this point cannot be spotted because the curve is ideal. Usually the point when the threshold voltage is crossed can be easily seen. This is the case in Figure 2 for the PIN diode.

Figure 4 may be used when explaining the forward and reverse biasing of a diode. When the diode is forward biased we apply a positive voltage to the P-region and ground the N-region. By doing this we give the free electrons energy to travel across the depletion layer and current will flow through the diode. When the diode is reverse biased a negative voltage is applied to the P-region of the diode. This will cause the electrons to be drawn away from the depletion layer blocking the current from running through the diode. When we look at the electrical diagram of the DUT in Figure 16 we can see that when a positive voltage is applied to any of the V_d's of the circuit the diode will be forward biased allowing current to pass straight to ground. If negative voltage is

applied to any of the V_d's the diode will be reverse biased and will block the current from going to the ground.

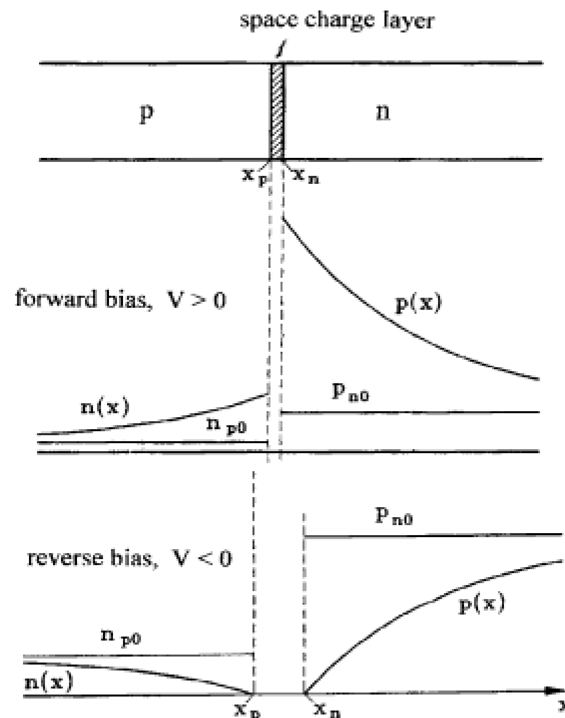

Figure 5. Carrier distribution in forward and reverse bias situation. Taken from Lutz 2011 [6]

Figure 5 presents a better picture on what happens when the pn-junction is biased with positive or negative voltage. The hole density close to the junction is described by p(x) and the electron density by n(x). It can be seen that depending on the applied bias voltage the carrier density either increases with forward bias or decreases with reverse bias.

3.1.4 RFIC Switch

The DUT in this thesis was an SP4T – Single Pole Quad Throw switch. The operation of a semiconductor switch is based on diodes ability to conduct current when forward biased and block current when the diode is reverse biased. The switch is also called a solid -state switch because it has no moving parts. The operation principle is still the same as with an electromagnetic switch. In the electromagnetic switch there is a lever that is moving so that it creates a contact with a metallic contact surface and begins to conduct electricity when a coil is powered. Powering the coil creates an electromagnetic force that pulls the lever against the contact. This state is called the ON state. When

the power is shut down from the coil, the force stops and the lever will return to its original position leaving the circuit open. This state is called the OFF state. The same principle is used with a diode but instead of powering a coil the biasing of the diode is changed by changing the voltage and current running to the diode. Forward biasing a diode to run electricity means that the positive terminal of power source is connected to the anodic p-side of the diodes pn-junction. Usually the current running through the diode is limited from the power source or using a current limiting resistor to prevent components from breaking down. Reverse biasing a diode may be done in two different ways. The first method is by connecting the positive terminal of the power source to the diodes n-side of the pn-junction, which makes the diode not to conduct electricity but block it instead. The other one that is used for the DUT in this thesis is by running a negative voltage to the diodes p-side. For doing this no moving parts are required. When the diode is reverse biased there is basically no current running through it and it may be limited from power source to zero.

3.2 LCP Substrate Material

LCP – Liquid Crystal Polymer is one of the substrate materials that became more popular in the beginning of 21st century for the high frequency applications because of a pursuit to find a cheaper material for Teflon® and ceramic materials, even though being introduced as a multilayer board material already in 1995. The good part of it is its combination of electronic, thermal and mechanical qualities. Especially its resistance to fractures and deformation caused by high temperatures are held in high value. Active and passive components can now also be integrated straight inside the LCP structure making it a good material for system-in-a-package (SIP) applications. With multilayering LCP layers on top of each other many advantages are gained. These advantages include smaller size and shorter distances between components which especially in millimetre wave applications is an important factor as soldered lines may cause interferences and errors in the signals by operating as antennas. LCP is manufactured by injecting the liquid into a mould where the hot material will freeze into its final state [8].

3.2.1 Flip-chip Bonding

After the LCP substrate specific for this application was manufactured with the conductor lines aligned with the flip chip dies of the switch it was combined with the chip by reflow soldering inside a flip chip oven. The connection was done using the Tin-Silver-Copper (SAC) lead-free solder bumps that are inserted on the switch die during manufacturing. Manufacturer's instructions were followed when the switch was bonded using a flip chip bonder and a minimum temperature of 245°C and a 3°C/second ramp rate [9].

3.2.2 Integration of Components to LCP

Because LCP may be manufactured by injecting the material into a mould, and because it has a good edge resolution, cavities may be left in the material to fit integrated components. In Figure 6 below can be seen, how integrating components into a multilayered LCP board is done.

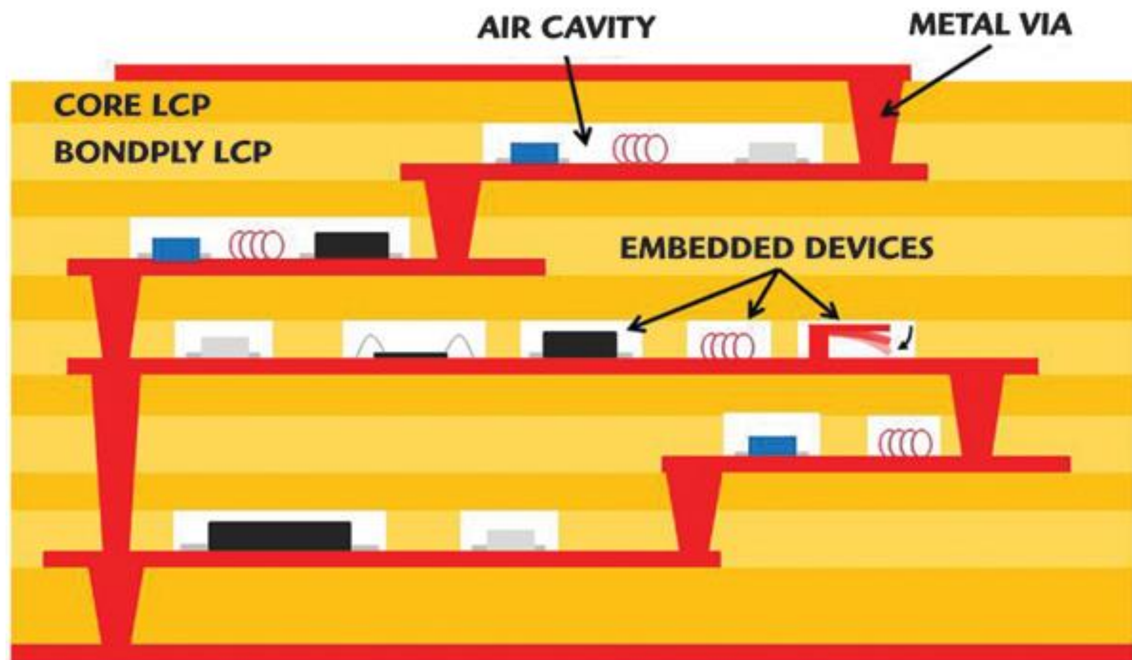

Figure 6. A schematic drawing showing how a multilayer LCP board can be made with integrated components. Taken from Kingsley 2008 [10].

Usually leaving cavities inside a multilayer board should not pose any threats or problems, but with millimetre wave frequencies the cavities may operate as resonators. Because of this they are usually filled with some material to decrease the volume of air inside the cavity. Another unique feature of LCP is, as seen in the Figure 6, that there are two separate layers which are bonded together one after the other. This is due to a melting property of the bondply material, which is made so that it melts at 290°C while

the core type of LCP melts at 315℃. When the temperature is between 295 and 315 degrees the layers melt creating a bond that cannot be separated without destroying the board. This is a benefit compared to LTCC which requires a higher manufacturing temperature of 900℃.

3.3 Concepts Used in Modelling and Testing of Millimetre Wave Circuits

3.3.1 Electromagnetic Parameters

The following characteristics are important when trying to understand the behaviour of electromagnetic waves in the LCP material. These factors hold for other radio frequency components in this thesis as well.

Dielectric constant, ε_r

A dielectric substrate has a complex value permittivity ($\varepsilon = \varepsilon' - j\varepsilon''$) and the dielectric constant (also known as relative permittivity) depends on the real part of the permittivity by equation $\varepsilon_r = \frac{\varepsilon'}{\varepsilon_0}$, where ($\varepsilon_0$ is the permittivity of vacuum), and its value in air and vacuum is 1. For millimetre wave applications a low dielectric constant reduces the capacitive effect between the elements. On the other hand if the dielectric constant is looked from the wavelength perspective with the equation below.

$$\lambda = \frac{c}{f\sqrt{\varepsilon_r}}, \tag{3-2}$$

where c is the speed of light(3 x 10^8 m/s in vacuum), λ the wavelength in meters and f the frequency in Hz. It is seen that a greater dielectric constant is suitable for smaller wavelengths allowing the circuits size to decrease. The dielectric constant of LCP is typically around 3 [10]. If the dielectric constant is increased the losses increase. This can be seen from the equation for the capacitance of a capacitor.

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}, \tag{3-3}$$

Where A is the area of the capacitor plate and d is the distance between the plates.

Conductor loss, α_c

Conductor loss on substrate material is caused mainly by the skin depth effect of electrical current. At RF and millimetre wave frequencies the roughness of the conductor surface has an effect that causes losses [11]. Surface roughness begins to have a significant effect on the conduction loss as frequency becomes higher and wavelength shorter. This can be seen from Equations (3-4) and (3-5). The skin depth (3-4) and the approximated formula for surface roughness (3-5) was first demonstrated by E. O. Hammerstad in [12].

$$\delta_s = \frac{1}{\sqrt{\sigma\pi\mu f}}, \tag{3-4}$$

where σ is the metal conductivity (S/m), μ the permeability of the metal ($\mu = \mu_r\mu_0, \mu = 4\pi\ x\ 10^{-7}$) and f is the frequency in Hz. The skin depth is a measure of how the RF current penetrates the conductor. From the formula it may be seen that the skin depth depends on the frequency, so that at lower frequencies the skin depth is larger and closer to being uniformly distributed within the conductor but at higher frequencies the skin depth becomes smaller. This means that the RF current does not go as deep into the conductor causing some of the energy to convert into heat and extensive warming of components is always a cause for insertion loss.

The surface roughness factor is defined as

$$\alpha'_c = \alpha_c\{1 + \frac{1}{90}\arctan\left[1.4\ x\ \left(\frac{\Delta}{\delta_s}\right)^2\right]\}, \tag{3-5}$$

where $\propto_c$ is the attenuation of perfectly smooth conductor, $\propto'_c$ is the corrected attenuation due to roughness, Δ is the rms surface roughness and is the skin depth δ_s from equation 3-5. The formula is close estimation to factorize and correct the conductor loss. The roughness has to be taken into account with higher frequencies when skin depth grows smaller and most of the RF current is moving on the surface. In visual inspection it is seen that the surface has irregularities that affect the movement of millimetre size current waves. From equation (3-5) it may be seen that as the skin depth becomes smaller, the actual roughness correction factor becomes bigger causing a greater effect on estimating the conduction loss of microstrip line on the LCP surface. Compared to polished semiconductor wafers, where the roughness may be only of

couple nanometers the LCP may contain roughness in size of couple of microns. Therefore it has a bigger effect on the conductor performance compared to smoother surfaces. The Figure 7 presents surface roughness of a conductor track.

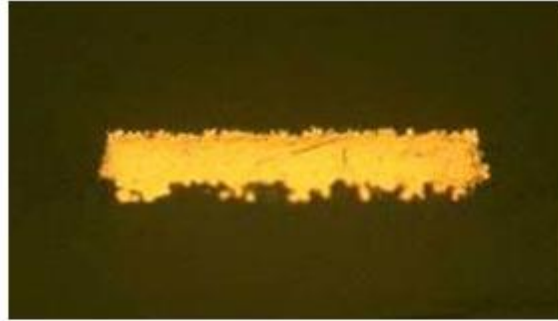

Figure 7. Thin copper track surface roughness. Taken from Hinaga [13]

Dielectric loss

Dielectric loss in high frequency transmission is caused by dielectric and conductor losses. It is generally expressed as loss tangent or dissipation factor (tan δ). It depends on the electric permittivity as

$$tan\,\delta = -\frac{\varepsilon'}{\varepsilon''}. \tag{3-6}$$

Low dissipation factor is favoured in RF applications so excessive losses are as small as possible. LCP typically has a loss tangent even less than 0.004 [10].

3.3.2 Thermo-Mechanical Parameters

Thermal conductivity

The thermal conductivity is a quality of material to explain how it conducts heat. For wireless and radio frequency applications thermal conductivity should be as stable and uniform as possible through the operating temperature range. Because LCP as a polymer is a poor thermal conductor, the heat generated inside the LCP package will not exit easily. On the other hand the package does provide a good insulation against any heat sources outside the package.

Thermal coefficient of expansion

Materials have a tendency to expand while under heat. The coefficient of thermal expansion (CTE) of LCP may be customized by alternating its chemical formula. The CTE is an important characteristic for a substrate that is being used with GaAs, for example

because of the CTE of the substrate should be close to the CTE of the parts that are attached to prevent cracks and buckling, which could break the parts or connections. Even though the CTE of LCP may be varied from 3 to 30 ppm/C, it is typically set at 17 to match the CTE of copper. A close to uniform CTE in the whole board makes it possible to use flip-chip bonding in cavities designed into the LCP substrate.

3.3.3 Noise in Electrical Circuits

The test in this thesis was made on an RF switch. To understand why low-noise and amplification with precision measurement circuits is essential the basics of noise causing effects and amplification calculations are revised in this subchapter.

Noise is troublesome always when RF and air-propagating signal transmission is used to transmit data or to receive information. The effective data that we use to control and measure environmental effects or send information as message packages has to be filtered out from a mess of radio frequencies traveling in the air. Filtering consumes the amount of data received the signal usually has to be strengthened by running it through an amplifier. While the signal is being amplified, all the excess data that was received at the antenna shall be amplified also. Most of this excess data is called noise that usually appears as a low frequency background treble. Among man-made noise sources like other radio transceivers and natural noise sources such as radiation in space (this is important especially as the frequencies become high and their wavelength approaches the wavelengths of light) the actual circuit being used will produce noise. The noise is caused because of the characteristic noise of the components in use. This noise is caused due to heating of the components and transmission lines under power, and other physical effects due to flowing electric current. The simplest way to formulate noise is if our whole impedance is completely in resistive form. The formula is N = k T B, where k is Boltzmann constant (1.38 x 10^-23), T is the operating temperature in Kelvin and B is the bandwidth of the device [13].

Even though the internal noise can be designed to be low by careful selection of components and their characteristics, the external noise causes problems for us. Another equation that characterizes our receiver-transceiver radio system is the ratio between the signal and the noise power called the signal-to-noise ratio.

$$\text{SNR} = \frac{S}{N} = \frac{signal\ power}{noise\ power} \qquad (3\text{-}7)$$

To demonstrate the noise of a complete circuit that has cascaded amplifiers, filters and modulators each one them may be given a noise factor F.

$$F = \frac{S_i/N_i}{S_o/N_o}, \quad (3\text{-}8)$$

where the SNR is compared from the input and the output. Due to matching effect between different components the noise factors may be added up. Adding up noise factors and more accurate noise calculations from different sources concerns more the area of circuit design which out of scope of this thesis and is left out because of that.

3.3.4 RF Matching and Scattering Matrices

In radio frequency applications the circuit design goal is to match each component and transmission line to 50Ω load. The effectivity of matching may be described by the voltage standing wave ratio (VSWR) and it is sufficient for this thesis to mention that VSWR follows the formula:

$$VSWR = \frac{V_{max}}{V_{min}}, \quad (3\text{-}9)$$

where V_{min} is the minimum and V_{max} maximum voltage ratio fluctuating in the transmission line. For a perfect match this value is 1, and deviations describe the mismatch caused by circuit design.

The mismatch of the circuit causes some of the signal fed into circuit to reflect back. This reflection is described by the reflection coefficient Γ and its value can be calculated from the formula

$$\Gamma = \frac{Z-Z_0}{Z+Z_0}, \quad (3\text{-}10)$$

Where Z_0 is the characteristic impedance and usually 50Ω. It should be noted that in general Z is a complex number, and hence the impedance may contain a reactance in addition to resistance. The matching of components is usually done by using a Smith chart to calculate the proper capacitor and inductor values so that the 50Ω matching

impedance is acquired. The matching is usually done by simulating the circuit with a program that assists in finding the right component values.

To generalize the use of reflection coefficient for two-port networks and higher an S matrix method can be used. It is based on Ohm's law:

$$V = ZI, \tag{3-11}$$

where Z is in matrix form and it has four terms similarly to the S matrix from now on. Figure 8 presents the idea behind equation (3-12). All the variables are now in matrix form.

Where

$$V = \binom{V_1}{V_2} \; and \; I = \binom{I_1}{I_2} \tag{3-12}$$

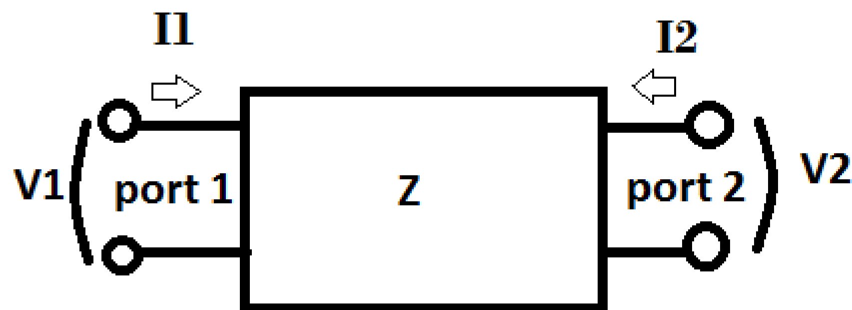

Figure 8. 2-port circuit parameter Z representation.

Appendix 1 "Deriving the S parameters" presents the derivation of the S parameters from the impedances Z and their use. The S parameters are a tool to calculate and present the matching of multi-port radio frequency systems. In the measurements performed for in this thesis one of the S parameters that is of great interest are the S11 which presents the reflection coefficient (Γ) from the device input port (usually in decibels). In a switch the reflection coefficient should be close to 1 which in decibels is 0dB dampening. Another S parameter that is monitored closely is the S21 parameter, which presents the circuit amplification. In the case of negative sign amplification it is called dampening (transmission loss) of the circuit. Amplification and dampening of the circuit occur when the signal travels from port 1 to port 2. A switch is not an amplifier, and hence the signal decreases from the switch input to the output. However, for a good switch this loss should be as small as possible. The switch mainly functions as a re-

router to feed the signal to a selectable output with as little loss in the signal power as possible.

3.3.5 S-parameters

Below the figure 9 taken from book Introduction to High frequency radio engineering presenting a directional coupler that is an electrical circuit application used in the measurement of S-parameters.

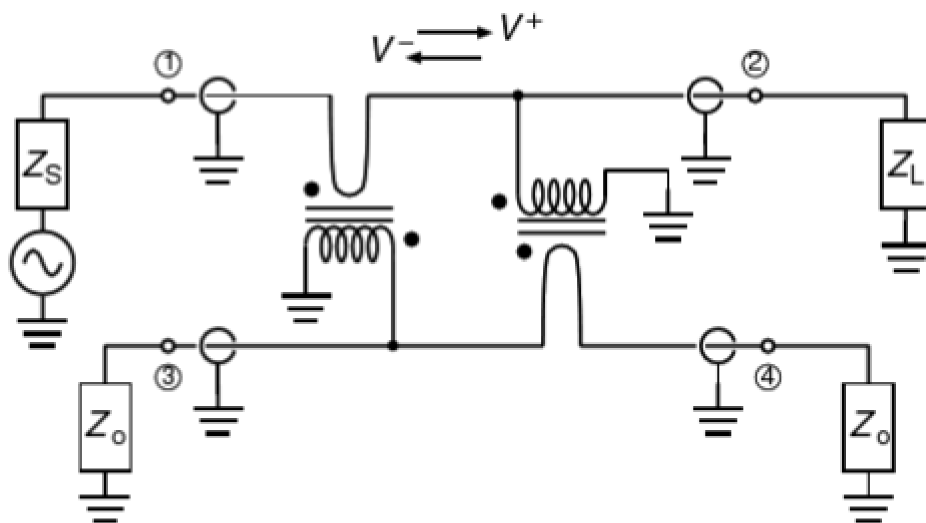

Figure 9. A circuit diagram of a directional coupler used for measuring S-parameters. Taken from Coleman 2004 [14]

The coupler is a device with four ports that each has a characteristic impedance of 50Ω. The basic operation of measuring the voltages in the coupler is given in [14].

> *Let V^+ and V^- − be the right and left travelling voltage waves in the line between ports 1 and 2. Assuming that the transformers are tightly coupled, and the self-inductance is large, they can be treated as ideal. The left-hand transformer will act as an ideal current source that forces current (1/nZ_0)*(V^+ −V^-) into the line joining ports 3 and 4. This in turn will cause a current of magnitude (1/2nZ_0)*(V^+ −V^-) to flow through the loads on ports 3 and 4. The right-hand transformer, however, will act as an ideal voltage source of magnitude (1/n)* (V^+ −V^-). This will cause a current (1/2nZ_0) (V^+ +V^-) to flow through the load on port 3 and current (−1/2nZ_0)*(V^+ +V^-) through the load on port 4. As a consequence, the voltage at ports 3 and 4 will be V^+ and V^- respectively. These voltages can be used to infer the right and left travelling voltage waves on the line joining ports 1 and 2 and hence the reflection coefficient Γ at the load Z_L . If we are only interested in measuring |Γ |, we can use simple envelope detectors at ports 3 and 4 to obtain |V^+ | and |V^- | and hence |Γ |=|V^-| / |V^+|. If we require the phase aspect of Γ, will need to find the relative phases of V + and V −* [14].

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Figure 10 shows how the directional couplers are connected to the DUT for finding S11 and S21 to find both transmission and reflection parameters of the device.

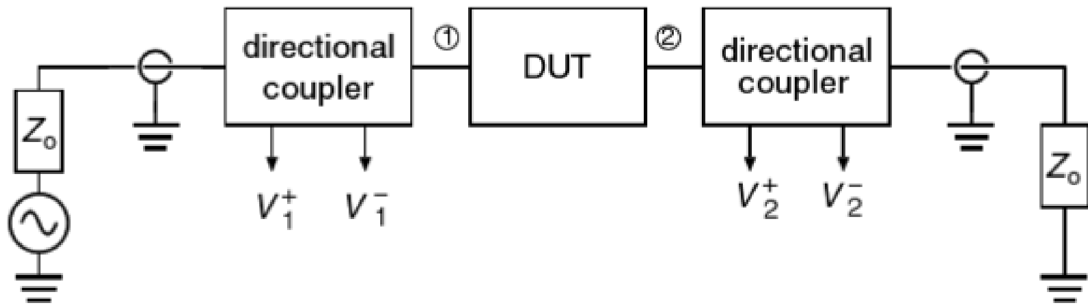

Figure 10. A diagram of a test setup for measuring the S-parameters of a device (DUT). Taken from Coleman 2004 [14]

The basic idea behind the S-parameter measurement is similar as in this work. But because of the small device size and high operating frequency more prone to errors, extremely small measurement needles were used in the radio frequency measurement of the components in this project.

3.3.6 Frequency Bands

At high frequencies the frequencies are divided into bands to make characterizing components easier for their use. Each band also has its special characteristics that set demands on product design as microstrips have to be matched carefully within the lengths of the signal wavelength.

Band Designation	Frequency Range in GHz
L-band	1-2
S-band	2-4
C-band	4-8
X-band	8-12
Ku-band	12-18
K-band	18-26.5
Ka-band	26.5-40
Q-band	30-50
U-band	40-60

V-band	50-75
E-band	60-90
W-band	75-110
F-band	90-140
D-band	110-170

Table 1. The microwave and millimetre-wave waveguide bands. Taken from Grananstein 2012 [15].

The device products used in this thesis operated at E-band which is between 60 GHz to 90 GHz as can be seen from the Table 1 above. The wavelength in this frequency band varies from 3.3 mm to 5 mm (in air).

3.3.7 Temperature Measurements and Modelling with Flip-chip Technology

There are various methods of measuring the temperature of a flip-chip component with sensors. The components used most often as sensors are thermocouples, thermistors, resistance thermometers that are also known as resistance temperature detectors (RTD). [17] Thermocouple is a measurement device consisting of two wires that are made out of two differently heat conducting metals. These wires produce voltage proportional to a temperature difference at either end of the conductors. It is not practical to be connecting the thermocouple straight into the component material surface because this may change the temperature behaviour of the component. A standard test method (STM) for testing the chip temperature variation is using a forward biased diode. This method takes advantage of the diodes forward voltage drop that changes according to temperature. This forward voltage drop of a diode is also referred to as a temperature-sensitive parameter (TSP) for because of its temperature varying effect. The advantage of using a diode is that it can be specifically designed into thermal test die to exist as a parasitic device even inside the substrate if the architecture and the substrate manufacturing process allows for it. Thus the diode would cause only extremely small alterations to the component's temperature profile.

Temperature variation models with flip chip packaging technology may be taken extremely far and the models made can be approximated with high accuracy by taking advantage of computational fluid dynamic computer (CFD) codes. However these require the right software to use and a lot of experience since simulations must be mod-

elled really carefully to get any real results out, and still they are only good approximations of how things may turn out in real life. These modelling techniques are not important in the scope of this thesis but another easier modelling method will be presented shortly. This method is called electro-thermal analog model [16]. A connection may be found with Ohm's law current flow through a resistor and heat flow through a component. As with Ohm's law the electrical current running through a resistance is caused by a voltage difference, in similar way a heat difference on the opposite sides of a component causes the heat flow $\mathbf{Q}$ through thermal resistance $\mathbf{R_{TH}}$. The principle is shown in the figure 11 below.

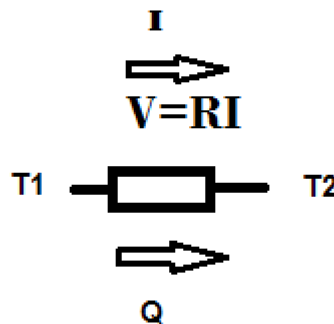

Figure 11. Illustrating the simplified idea of calculating heat flow across a "resistor"

$$\Delta \mathbf{T} = \mathbf{QR_{TH}} \tag{3-13}$$

By using this simplifying method any electrical package may be demonstrated as a big group of thermal resistors as seen in Figure 12 [16].

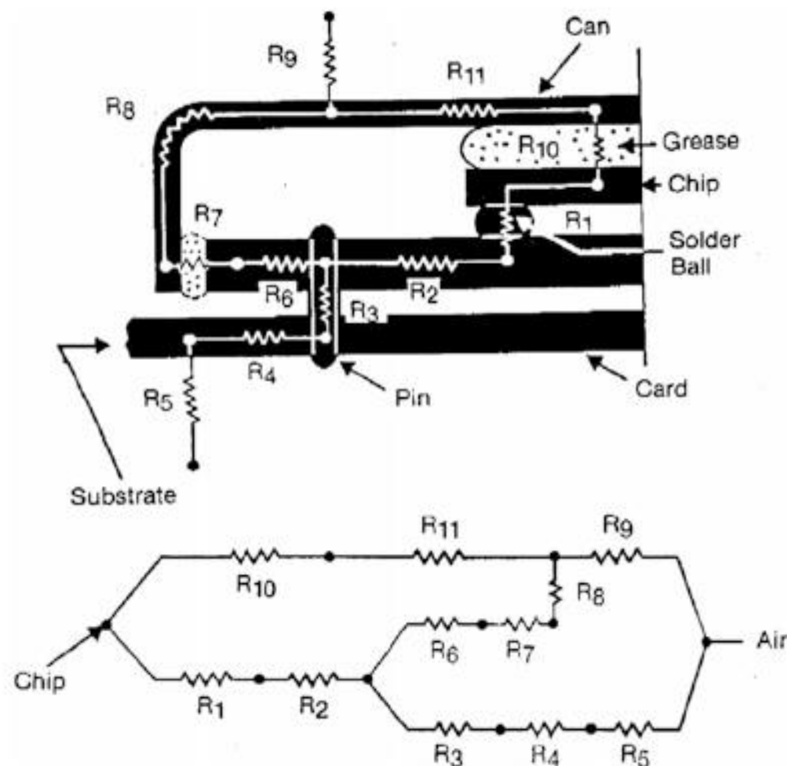

Figure 12. Showing a part of a chip with the simplified thermal resistance analogy method. Taken from Tong 2013 [16]

By using this method and knowing the geometrical structure of the flip chip device, estimated calculations of the temperature behaviour may be made based on earlier tested and common standard temperature factors.

3.3.8 Environmental stress screening

Heat in general makes components age faster because of the chemical properties of the substrates used and due to wear of semiconducting elements in higher temperature when these materials are used. Electrical current running through the components wears them out because resistance in a conductor line is bound to cause some of the electrical energy to turn to heat. The heat on the other hand causes the resistance to increase. These effects countering each other are caused by the microscopic friction of the electrons moving by forced potential inside the material. The components are usually given a lifetime of years or thousands of hours in use. To simulate the years in use heat may be used to hasten the aging process of the component. The reliability tests that use various stress sources to prematurely age a product are referred to as accel-

erated life tests. The accelerated life tests may be divided into four different categories: product development/verification tests, qualification tests (QTs), accelerated life tests (ALTs) and highly accelerated life tests (HALTs) [17].

Accelerated life testing is a reliability test method that may include various stress types. These are:

- low temperature storage
- thermal cycling
- power cycling
- thermal shock
- thermal gradients
- fatigue
- mechanical shock
- drop shock
- sinusoidal vibration tests
- random vibration tests
- creep/stress-relaxation tests
- voltage extremes
- high humidity
- radiation.

These physical stresses may be applied as step tests or as continuous conditions, and to achieve greater pre-maturing effect different stress tests may be combined. First the failure modes causing the device to fail are evaluated then the stresses causing these failures are quantified and estimated. Then the stress levels are increased and an evaluation is made based on how much the increased stress, increases the failure and aging rate of the product. The products should be tested with sufficient parameters to stress the design strength but not at too high values that would bring it to its hard failure where the part or the enclosure materials begin to fail by melting or fracturing. The reliability may be improved by either enhancing the design to create greater design strength, by lowering the design stress or by setting limitations for the product if it is not able to withstand stresses for example because of the limitations in the technology in use. It is known that smartphone touch screens start malfunctioning at low temperatures and this is caused by the electrical qualities in the technology being used. The risk with designed life tests outside the field is that the assumed physical conditions

where the failure is calculated to appear may not accelerate the expected failure but cause another failure which cannot take place in field conditions.

Because the component tested in this thesis was from a commercial provider (TriQuint) the need for an accelerated life test to see where the first faults occur was disregarded as the manufacturer has ran their own tests for the components already. Instead a temperature step stress with a burn-in test at each heat step was designed for the test circuit that has already been used to find out if failures would occur when the chip is connected to a substrate.

A burn-in test is a MIL standard test given specifications in MIL-STD-883H Method 1015.10. The purpose of a temperature step stress test is to find devices with manufacturing defects that would cause early stress and time dependent failure. The burn in test is made close to the maximum operating conditions for the device. Electrical measurements are conducted at regular intervals as seen in the tests in this work, where each step could be seen as a burn-in stress on its own. The test instructions specify the minimum temperature levels and times for burn-in. In this thesis the burn-in temperature and times were modified because a burn-in had never been done for the DUT and to see how different temperatures act with the test board substrate material.

3.4 Measurement setups and device under test

3.4.1 S-parameter and climate chamber test setups

The used test chamber was an ESPEC PTZ-175 climate chamber. It has 500 x 280 x 300 mm chamber with a temperature range from -70℃ to +180℃ and a temperature change rate of 5℃/minute heat-up and 5℃ cool-down. It will easily reach the required temperature values needed in the test. The chamber can be controlled either through an embedded control interface in the front panel or using a PC and software which connects to the chamber through an RS-232 port. The device is built to follow IEC-60068-1 standard for environmental testing. [18]

Figure 13 shows the test setup and equipment with type numbers for the E-band S-parameter tests.

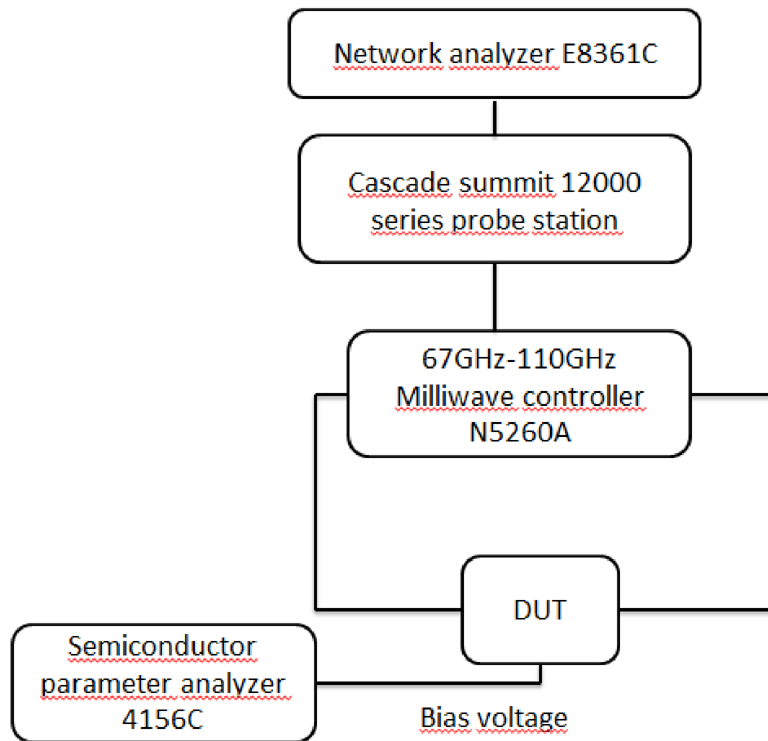

Figure 13. The S-parameter test setup at MilliLab-VTT microwave laboratory.

Test was done on the Agilent PNA microwave network analyser that has a bandwidth from 10 MHz to 67 GHz. Since frequencies higher than 67 GHz were needed in the tests the network analyser's bandwidth had to be increased using a millimeter-wave controller N5260A from Keysight (previously Agilent). The semiconductor parameter analyzer 4156C was used to produce the bias voltages and currents for the test because of its capability to produce extremely clean and transient free power. Figure 14 below shows the probes that were used for measuring the radio frequency characteristics of the DUT. The characteristics of the probes are specified by their frequency range for which they are designed for, and by the distance of the ground and signal needles in the probe. Figure 14 shows a 150 micron probe head. The distance between the middle and the outer needles is 150 micrometres. A 200-micron probe would be preferred for this particular circuit as may be seen from the figure. The outer needles just barely touch the ground contacts creating a good connection for the measurement. The probe type is referred to as GSG-probe for its structure having three needles; ground-signal-ground. The probe has a signal needle in the middle. This needle is the centre conductor that runs inside a coaxial cable. The grounds are then connected to the coax ground, and there are two of them to ensure proper grounding at

higher frequencies. A typical GS-probe with ground-signal needles is considered to be reliable only up to 10GHz.

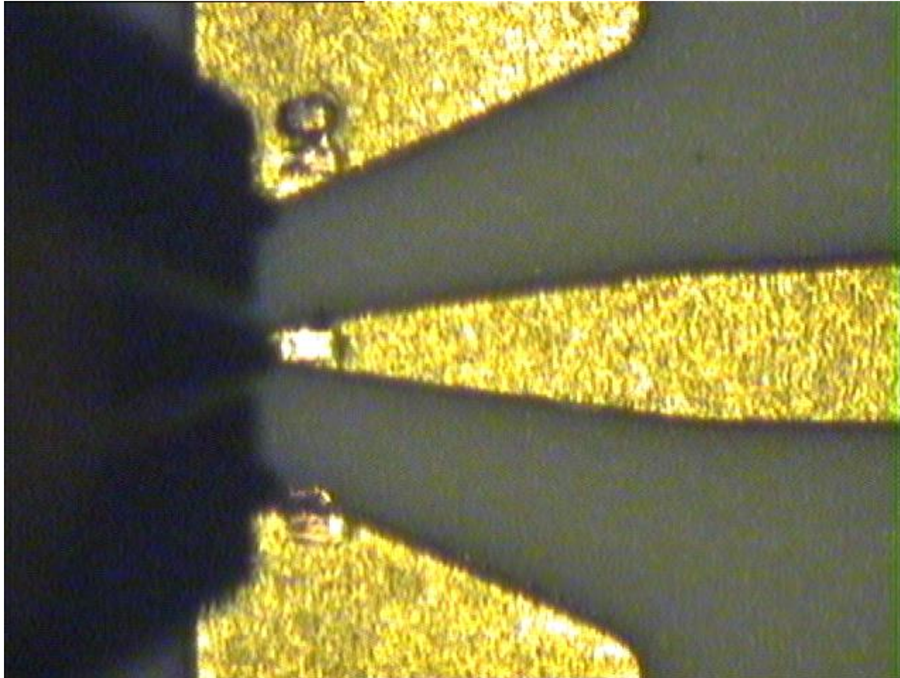

Figure 14. A photograph of the probe tip on the device contact

The vector network analyzer was calibrated with Short-Open-Load-Thru (SOLT) on-wafer calibration standards. The tested switch was powered during the test using the semiconductor analyser and while in the chamber, power was fed through a 50 mm port on the side of the chamber. The test setup and biasing may be seen from the Figure 15.

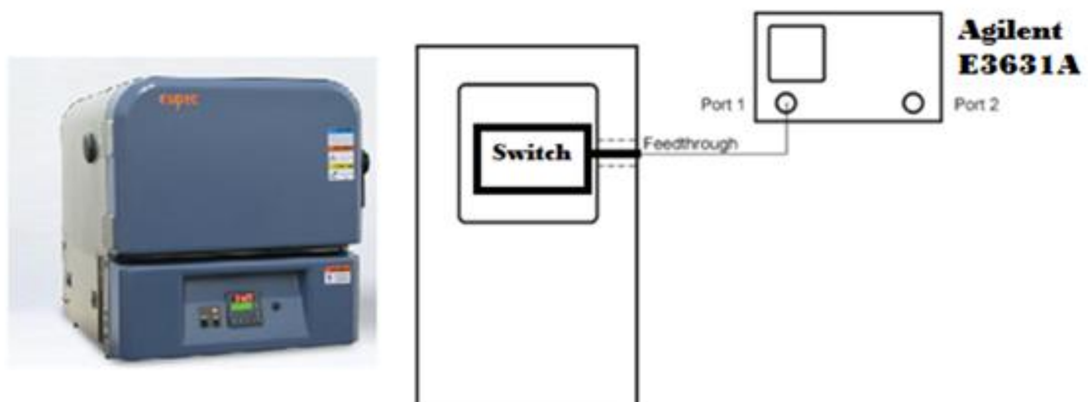

Figure 15. The biasing arrangement method of DUT in the climate chamber.

The bias was used to activate the component inside the climate chamber so that it is active while the heat stress was used to age the device, similarly as if the device would be used in an application. The voltage source during the test was Agilent E3631A triple output DC power supply. The power supply was controlled using Labview software and a program that was made using the GPIB libraries from National Instruments (see Appendix 2 for a screenshot of the program).

3.5 The device

3.5.1 Device under test

The switch that was used in the test was made by TriQuint semiconductor and is referred to with part number TGS4306-FC, an RF switch flip chip MMIC. The switch has one RF input port and four RF output ports. The diodes are produced using PIN MMIC technology to make the four Gallium Arsenide (GaAs) diodes in the switch. The operating frequency range of the switch is from 70 GHz to 90 GHz. Main characteristics of the component are a 3.0 dB insertion loss 20 dB isolation between the four outputs, a typical 8 dB thru state return loss and less than 5 nanosecond switching speed. As may be seen from the electrical diagram of the circuit in Figure 16, the DC blocking capacitors are already integrated inside so no external DC blocks are required.

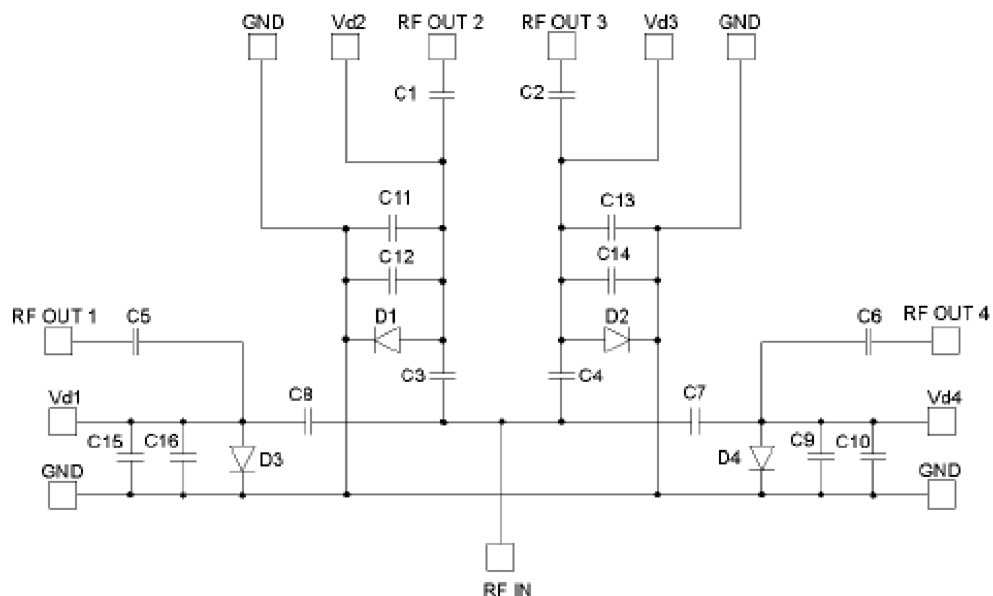

Figure 16. The circuit diagram of the switch.

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The DC blocks are the capacitors, C1, C2, C3, C4, C5, C6, C7 and C8 positioned at the RF input and output. The circuit is designed so that a separate connector is used to contact the dies under the flip chip. In the Figure 12 below the switch is seen mounted on the LCP substrate. The flip-chip connections are under the switch and cannot be seen in Figure 17.

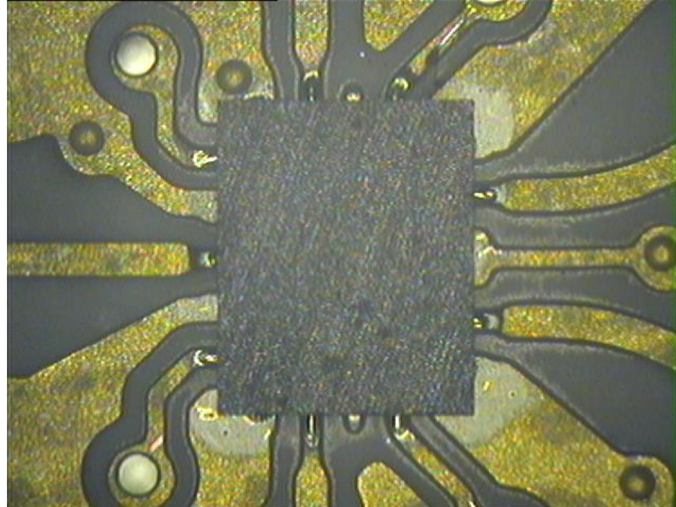

Figure 17. A photograph of the SP4T switch on the LCP substrate

The input conductor is coming from the left in the middle. The basic operation of the switch is based on forward and reverses biasing the diodes D1, D2, D3 and D4. To forward bias a diode, a positive voltage of 1,35V with 10mA current is applied to the V_d of desired RF output. To reverse bias the diode a negative voltage of -5V with 0mA current is applied to the V_d of the desired RF output. The output port is selected by reverse biasing the selected RF output. With one input port and four outputs, selection of the output is referred to as states. Only one output may be used at a time for normal operation. The states follow in numerical order with State 1 being RF 1 output selected. In state 1, a voltage of -5V is applied to the V_{d1} and 1,35V with 10mA current to the rest. In state 2, a voltage of -5V is applied to V_{d2} and 1,35V with 10mA current to the rest. The only exception is in state 5 when 1,35V with 10mA current is applied to all V_d's. This state isolates the RF input from all the outputs. The test report in chapters 4 and 5 the voltage -5V with 0mA is referred to as the ON-voltage and the 1,35V and 10mA current as the OFF-voltage.

4 Reliability Test

4.1 Organizing the Test

The chip was run through a temperature step stress test designed specifically for this thesis. Step stress generally means that the DUT is held at steady temperature for a set time. After each step the temperature is increased by a predetermined amount. In between each step the DUT was RF-tested to verify its operation after each step. In case of active devices the device can be biased to activate the active components inside to simulate field operation. In this thesis after the RF test was passed the DUT was taken back to the climate chamber and the steady temperature will be increased by 25 degree Celsius for the next 48 hours steady test state. The test method is referred from the ESCC Evaluation test program for discrete semiconductors document [19]. The Espec BTZ-175 chamber easily reached the required temperatures.

The chamber required a rise time to heat the chamber up to required temperature. Test clock was started when the set temperature had been reached and stopped after 48 hours. The bias was checked with a digital multi meter (DMM) after the devices had been put in to the climate chamber, and before the test clock was started. The bias was also checked using DMM after the test clock stopped, and before the DUT was removed from the chamber. Electrical tests were performed within 48 hours of the ending of the test as the MIL-STD-883-5010 for burn-in requires.

The temperature steps were created using an ESPEC BTZ-175E climate chamber. The climate chambers are fairly accurate temperature wise but when the temperature is taken from room level to test level the chamber requires a steadying time so that the whole chamber is uniformly at the same temperature. It was assumed that when the whole chamber had reached a steady temperature level, the DUT was also at the same temperature and the test clock may be started. The steadying time for this ESPEC chamber was tested before the actual testing began. It was found to be approximately 5 minutes. After ramping up the temperature it first rose at least 2 degrees Celsius above the stated temperature after which the chamber turned off and cooled down to test temperature. The Figure 18 shows how the temperature was first ramped up. In this test it was decided sufficient to monitor the ambient temperature of the chamber

relying on the chambers own thermal couple sensor. The decision was based on the fact that this thesis concentrates more on demonstrating the test feasibility rather than finding accurate and statistically comparable results from a single component. But because of this the component temperature could have been slightly different than the temperature indicated by the chamber readout.

The graphical representation of the step stress is shown on Figure 18 below. This figure presents the thermal stress levels where the component was held for 48 hours per each level. The radio frequency test after the stress was performed when the temperature was lowered back to room temperature approximately around 24 degrees. The test laboratory had an artificial clean room inside that had been installed after building the room. The higher room temperature can be explained by the way the ventilation has been construction that makes all the fresh air spread to the room through the clean room making the ventilation poor. The chamber has small leakage that increases the room temperature.

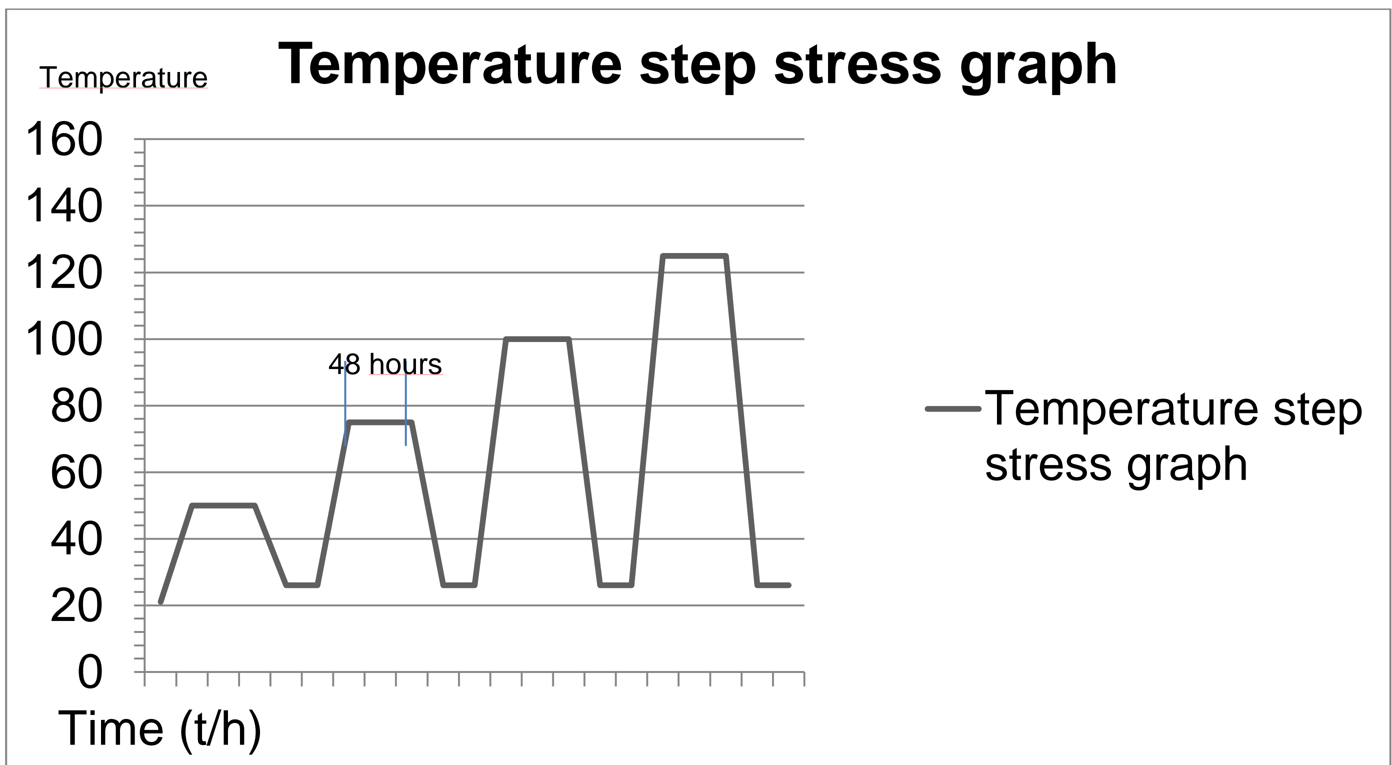

Figure 18. Temperature step stress graph

The temperature per each stress level are presented in the table 2 below, where the actual degrees in Celsius are on the left and the soak time is on the right.

Table 2 Temperature levels

Temperature (℃)	Test time (h)
25	48
50	48
75	48
100	48
125	48

Figure 19 and Figure 20 present photos showing the microscopic RF testing probes in contact on the LCP chip with the chip installed.

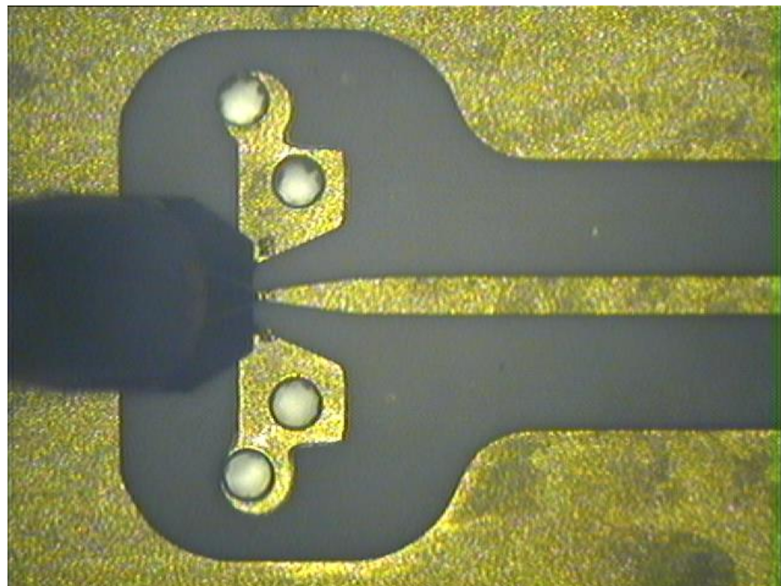

Figure 19. RF probe on chip input

As may be seen from the photos, the ground needles of the probes just barely make a contact with the gold contact pads. Ideally the needle would make a contact in the middle of the ground pad. Results were found accurate enough to state that the connection was good.

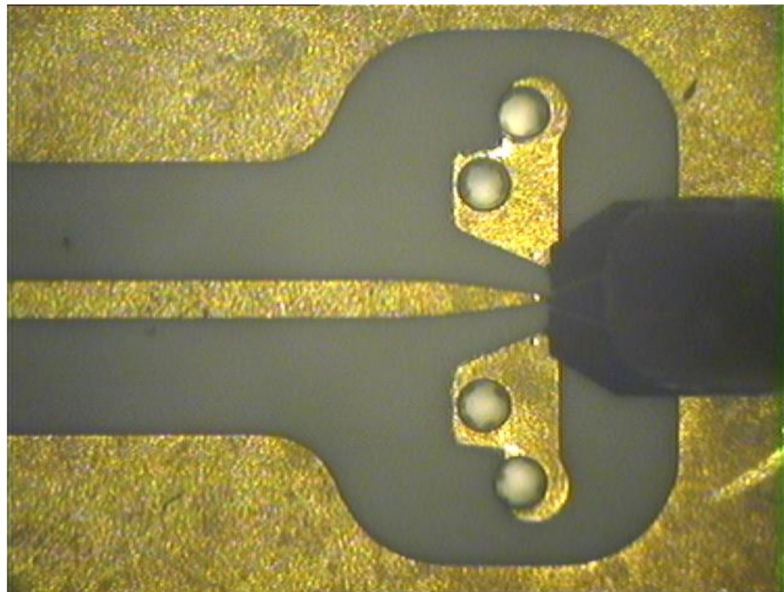

Figure 20. RF probe on chip output

The radio frequency tests were repeated always after the 48 hour soak period to see if degradation had occurred already at lower temperatures. The RF tests were performed in a 100 000-class clean room. The complete flow chart of the test may be seen below in Figure 21.

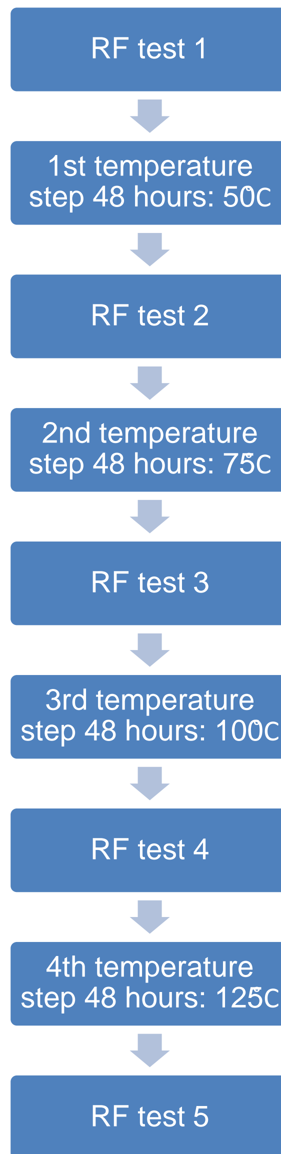

Figure 21. The test measurement flow chart.

The test was completed without breaking the DUT. So all the 5 RF test were made.

4.2 Test Report

The first radio frequency test was made on Wednesday 31.10.2014 at 12:00. The measurement equipment was calibrated as reported in chapter 3.4.1. The input power to the chip was set to be -17dBm. The intermediate frequency that was used for sampling was 150Hz and the test resolution was selected to be 801 points. The resolution selection was kept at average to make the test faster. The knowledge was used deter-

mining the resolution that the DUT should only acts as a conduction line allowing the signal to pass through without great changes expected, therefore greater resolution which is usually used to find accurate resonance spikes in high frequencies was not needed. The radio frequency test was mainly meant to check that the DUT was still functional and to monitor if the insertion losses grew or isolation decreased after being exposed to thermal stress while being biased and in operational mode. This first radio frequency test was the 0-level test to which the rest of the tests were compared. The voltage source has three output channels out of which two were used. These will be referred as channel 1 and channel 2 in the text.

The voltage had to be fine-tuned during the tests to find accurate output voltage. This was not done on all the steps as it was not needed. When fine-tuning was done it is explained in the report. First temperature step was initiated on 31.10.2014 at 12:15 o'clock. The temperature inside the chamber was set to 50℃. In the first temperature step the voltage for the channel 1 of the voltage source was set to be 1,440 V even though the specification sheet shows 1,35V for the OFF-state RF-outputs, but with 1,44 V input the actual voltage level was measured to be 1,268 V. The voltage was slightly less (1,35-1,268=0,082) than what was expected to go into the output terminals, this loss was not thought to be significant. The loss of voltage may be explained with various reasons as losses in the cable, inaccuracy of the display on the voltage source to name two. This voltage will be adjusted again during the ramp up of the next heat step to go near the required 1,35V. The current for the OFF voltage channels was limited to 16mA and the actual current level was monitored to be 11mA so slightly more than the 10mA given in the specification. The maximum current that may go in to any of the V_d inputs is 40mA so it should not cause any trouble with the device as the current is mainly used to drive the diode into compression. For channel 2 of voltage source, the terminal controlling the ON-state RF-output, the voltage was set to -5,00V and the actual measured voltage was -5,004 V close to the expected value. The current was limited to 0A, and the actual current level was measured to be 5,529$\times 10^{-5}$A close to 0 when the minimum current that would drive the diode into conduction is 10mA. This value was 200-times smaller so the RF output 4 should be functioning normally. The first heat step was finished on 2.11.2014 at 12:20.

The DUT was inspected visually after the first temperature step and no changes were found. The second radio frequency test used the same specifications as the first one to keep them comparable. The second radio frequency test was made on 3.11.2014 at 10:00. The second temperature step test was initiated on 3.11.2014 at 10:15 and the test clock was started at 10:35. The temperature inside the chamber was ramped up to 75°C. The second test ended on 5.11.2014 at 11:00.

The DUT was inspected visually after the second temperature step, and again no changes were found. The third RF test was produced on 5.11.2014 at 11:05. The third heat step was started on 5.11.2014 at 11:20 and the test clock was started at 11:40. The temperature inside the chamber was ramped up to 100°C. In the beginning of the test the voltage was set to be 1.4 V, but the measured value stayed at 1.2 V so the set voltage was increased to 1.6 V producing a voltage of 1,2 V, the voltage was not adjusted more since no change could be observed. The control voltage for the output was -5 V producing a measured voltage of -5 V and 0 A current (reading from the voltage source). Increasing the voltage for the OFF output terminals did not affect the measured voltage. The third thermal step ended on 7.11.2014 at 12:10.

The DUT was inspected visually after the third heat step and no changes were found. The fourth RF test was produced on 7.11.2014 at 12:20. The fourth heat step was started on 7.11.2014 at 12:30 and the test clock was started at 12:50. The temperature inside the chamber was ramped up to 125°C. The fourth thermal step ended on 9.11.2014 at 13:10.

The DUT was inspected after the fourth heat step, and still no changes were found. The fifth RF test was produced on 10.11.2014 at 8:30.

5 Results and Analysis

During the S-parameter measurements (RF-tests) between each thermal stress step the parameters did not show significant alterations. The peaks did not shift in frequency either so it can be said that the chip tolerated the burn-in thermal steps extremely well without any degradation.

Reflection parameters:

The graph in Figure 22 shows the S11 parameters (SP4T input port) from the five RF measurements when the device was biased to isolation. The device is in isolation when switch state 5 is selected by applying 1.35 volt and below 15mA current to each of the five RF outputs.

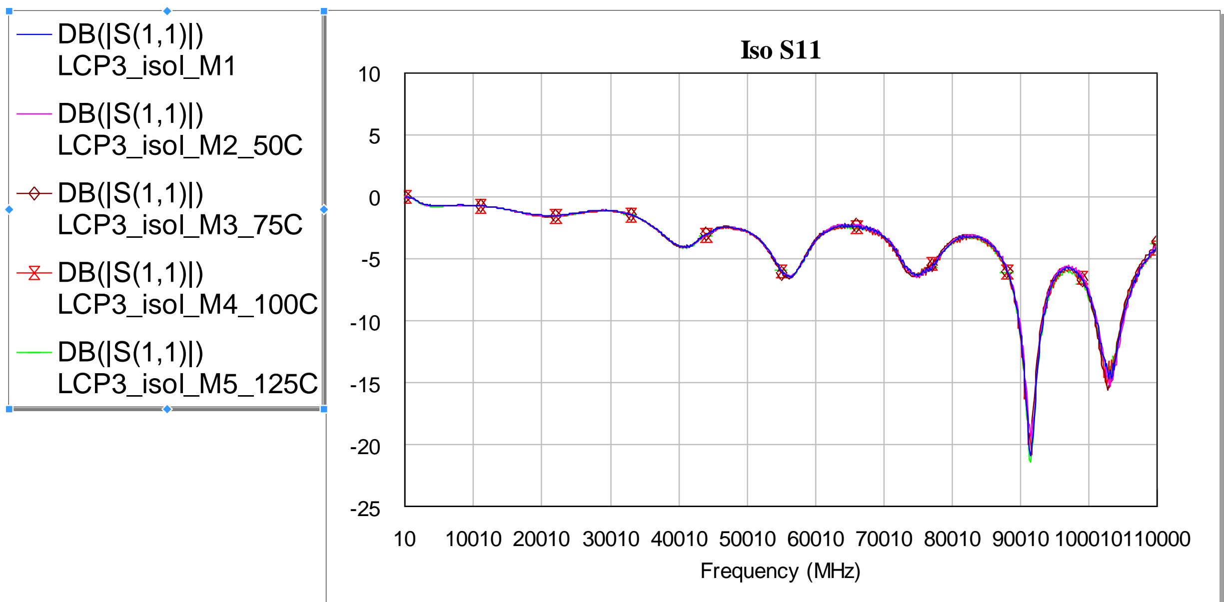

Figure 22. S11 parameters switch in state 5.

The graph in Figure 23 shows the S11 parameters when the device was biased to open RF output 3. Switch state 3 is enabled by biasing the RF output 3 with 1.35 volts and 15mA and applying -5 volt and 0A to other RF outputs.

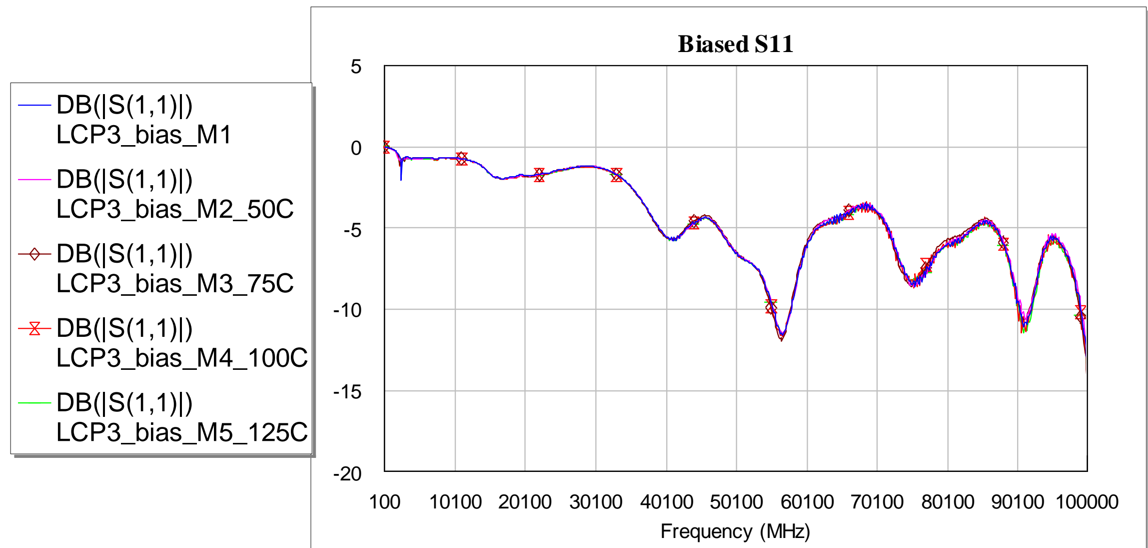

Figure 23. S11 parameters in switch state 3

Transmission parameters:

The graph in Figure 24 shows the S21 parameters from the five RF measurements, when the device is biased to isolation. The device is in isolation when switch state 5 is selected by applying 1.35 volt and below 15mA current to each RF output. The isolation was found to be approximately -25dB in the frequency band.

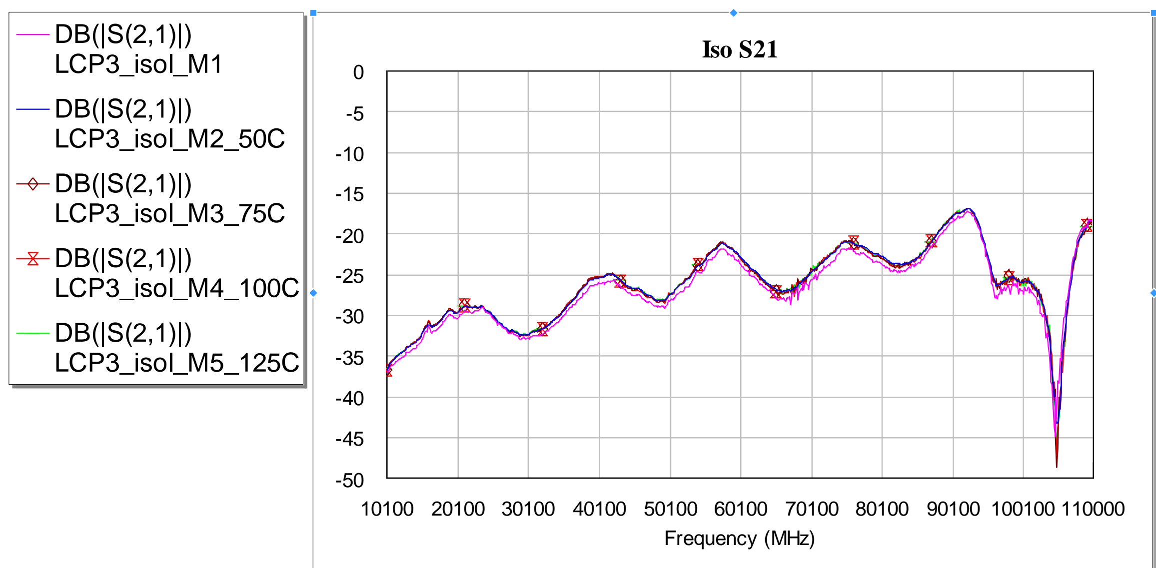

Figure 24. S21 parameter in switch state 5

The graph in Figure 25 presents S21 parameters when the device is biased to open RF output 3 for signal transmission. Switch state 3 is enabled by biasing the RF output 3 with 1.35 volts and 15mA and applying -5 volt and 0A to other RF outputs. The graph presents an insertion (transmission) loss of approximately -7dB in the frequency band. It is clear from all the S-parameter results (Figures 22 to 25), that the stress testing has not degraded the RF performance of the SP4T switch in any significant way. Any small deviations between the five sets of measurements are within the VNA calibration accuracy.

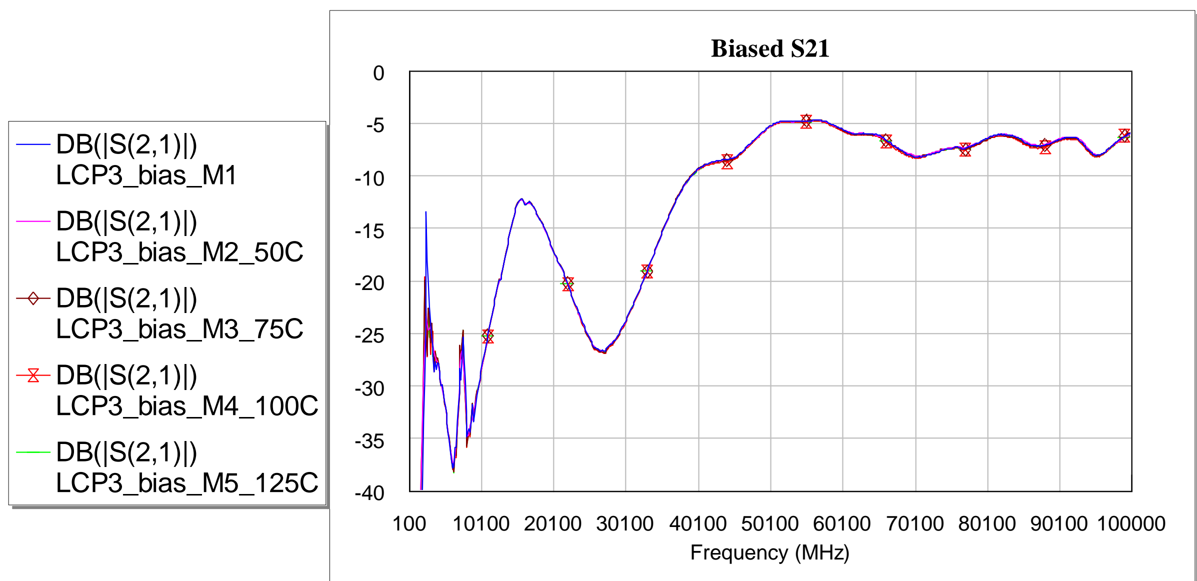

Figure 25. S21 parameter in switch state 5

Operational voltages:

The voltages were recorded for the OFF bias 1.35 voltages for it showed variation during the stress steps. The ON bias -5 stayed at fairly steady state with only 0,00X variations in the voltage. The current for channel 3 with -5 V output stayed also approximately close to zero with only micro amps measured and reported. The variations for the 1.35 OFF bias were explained due to limiting the current level to 10mA. The program used to drive the voltage source made it work as a steady-current source because of setting the current to a certain level. The voltage source then kept the current at a steady level but alternated the output voltage as a function of this current. The millivolt size fluctuation in the voltages was considered to be due to semiconductors impedance characteristics changing in a raised temperature, which caused the voltage source to adjust the voltage to maintain the current at the set level.

The voltage was recorded every 5 minutes. The resulting graph is seen on Figure 26. The number of record can be read from the x-axis and the y-axis presents the value of the voltage in volts. Graph of the first stress step voltage:

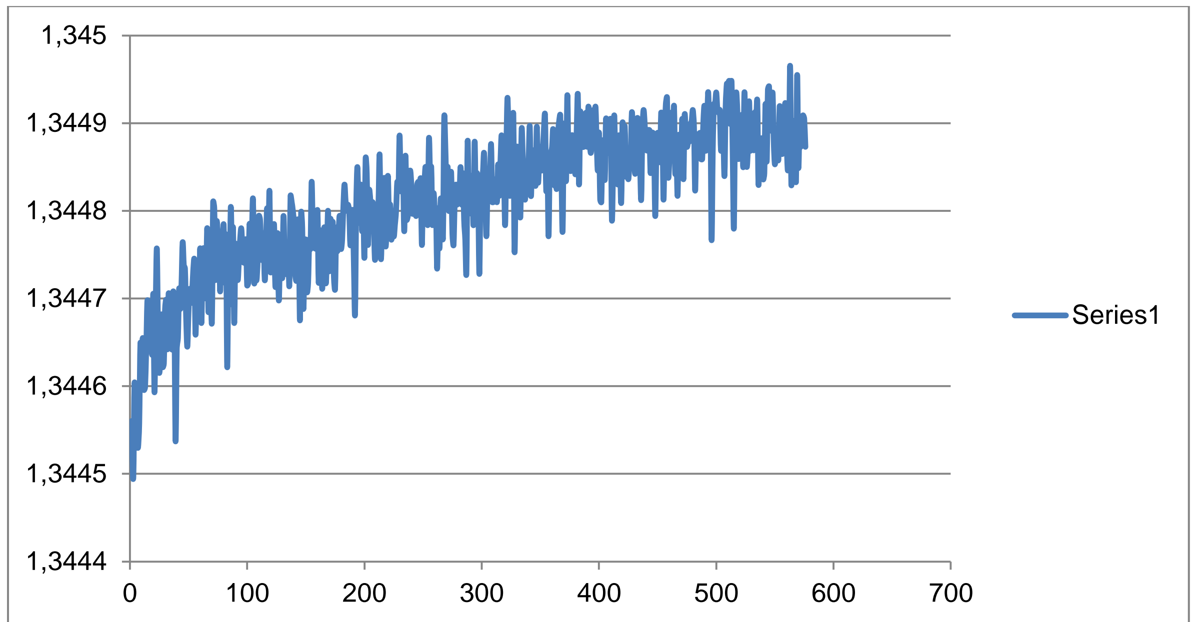

Figure 26. Output voltage to drive RF-inputs 1,2,3,5.

6 Conclusion

A reliability assessment project was conducted on a single MMIC SP4T chip, with the project purpose in testing whether the facilities at MilliLab – VTT were sufficient for temperature step stress tests to be carried out. This thesis explained the technologies that were involved, the test processes and gave background information on reliability engineering.

The test was designed by the standards generally in use when considering sending a device to space. Designing a special test structure gave a good presentation of the flexibility of making various reliability assessments at MilliLab – VTT. Tests were carried out as planned and it can be said that it gave valuable information and confidence to VTT to take on more demanding reliability tests in the future.

From the Figure 22 to Figure 25 it can be seen that the device endured the temperature stress test without experiencing degradation in the performance. The Figure 24 shows a small alteration after the first measurement but the next RF tests were consistent. This small change can be explained that the burn-in temperature in the first step had a small effect on the devices performance. The test was successful even though only one device was tested.

This thesis gives a good start for anyone interested in the testing of millimetre wave components. To upgrade this thesis a bigger batch of devices would be needed so that the results could be used to make statistical deductions on the reliability and the breaking conditions of the device. Some statistical mathematics would also be required to handle greater sample sizes for products and to analyse and approximate different failure conditions.

Improvement suggestions include recording the voltages of the DUT during the heat steps. The program could monitor the output voltage and make adjustments accordingly automatically. The voltages that are set from the program should then also be recorded to see how the actual voltage responds to the set voltage.

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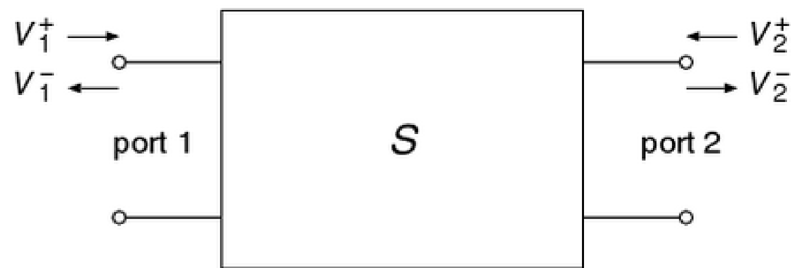
Appendix 1 Deriving the S parameters



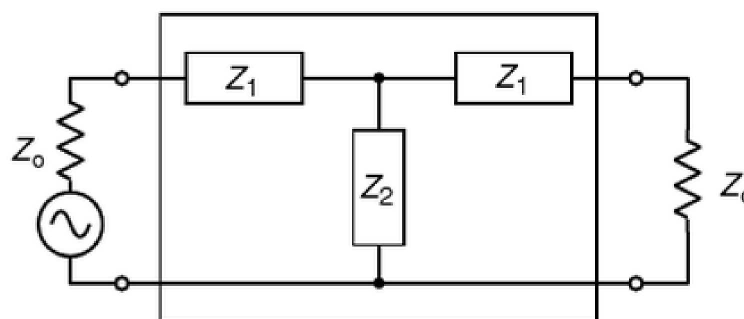
Instead of the traditional Z matrix description seen in the chapter, a two-port system may be pictured as above. The in- and out-going waves $V_1^+, V_2^+ \; and \; V_1^-, V_2^-$ may be found using the S matrix relation $V^- = SV^+$ where $V^{+/-} = \begin{pmatrix} V_1^{+/-} \\ V_2^{+/-} \end{pmatrix}$.

Then the 2x2 S-matrix can be found using the equations:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+$$

The network is considered to be symmetric from both directions. A 50 Ω matched load is connected to port 1 and port 2. Now because of the matched load at port 2 the in-going voltage at port 2 is $V_2^+ = 0.$ And so from the above equation pair S_{11} may be found. This shall be called the reflection coefficient at port 1. Now another picture is needed which shows the impedances between the port 1 and port 2.



Next look into port 1 to see the input impedance from this direction to calculate S_{11}. $Z_{in} = Z_1 + Z_2||Z_1 + Z_0$ is the input impedance seen from port 1 and deriving the equation further a complete form is found to be.

$$Z_{in} = Z_1 + \frac{Z_2(Z_1+Z_0)}{Z_0+Z_1+Z_2} = \frac{Z_1^2+Z_0Z_1+2Z_1Z_2+Z_0Z_2}{Z_0+Z_1+Z_2}.$$

Now then $S_{11} = S_{22} = \Gamma_{in} = \frac{Z_{in}-Z_0}{Z_{in}+Z_0}$ so the equations combined reveals the complete equation for the reflection coefficient,

$$\frac{Z_1^2+2Z_1Z_2-Z_0^2}{Z_1^2+2Z_0Z_1+2Z_1Z_2+2Z_0Z_2+Z_0^2}.$$

Next we may find the solution for S_{21} since the output voltage is $V_2 = V_2^-$.

$$V_2^- = V_2 = V_1\frac{Z_{in}-Z_1}{Z_{in}}\frac{Z_0}{Z_1+Z_0}.$$

Now V_1 is needed. It is found to be $V_1 = V_1^+ + V_1^- = V_1^+ + S_{11}V_1^+$ and ly $V_1^+ = V_1/(1+S_{11})$.

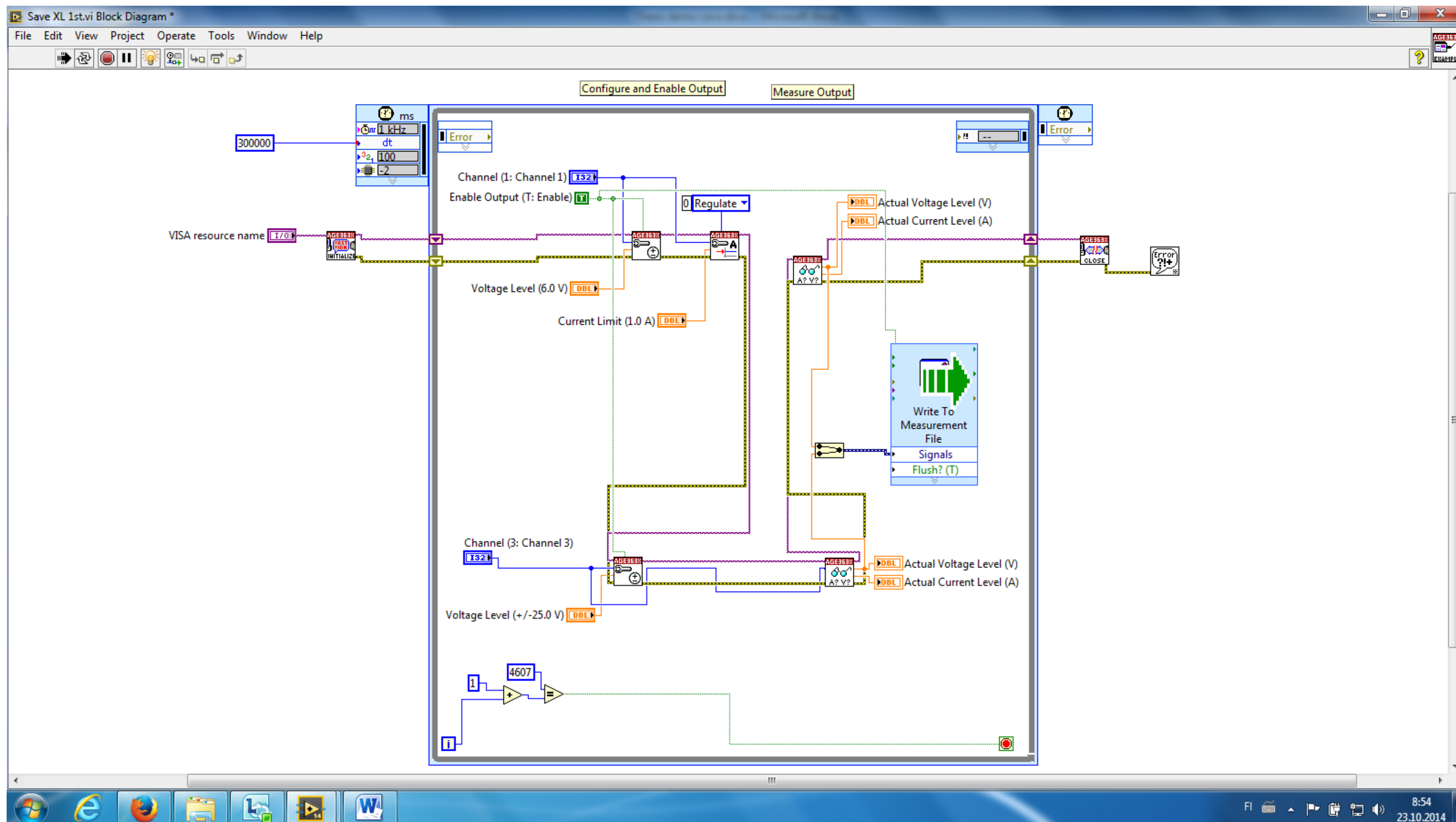
Now the final S parameter can be solved and it is called the amplification of the circuit, it may also be negative.

$$S_{21} = \frac{V_2^-}{V_1^+} = V_1\frac{Z_{in}-Z_1}{Z_{in}}\frac{Z_0}{Z_1+Z_0}\frac{1+S_{11}}{V_1}$$ And after completing the equation

$$S_{12} = S_{21} = \frac{2Z_2Z_0}{Z_1^2+2Z_0Z_1+2Z_1Z_2+2Z_0Z_2+Z_0^2}.$$

These four are the essential parameters that are usually measured during the radio frequency test.

Appendix 2 Screenshots from GPIB voltage control program with Labview



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VISA resource name

GPIB0::5::INSTR

Output Settings

Channel (1: Channel 1)

Channel 1 | 1

Voltage Level (6.0 V)

1,440

Current Limit (1.0 A)

0,016

Channel (3: Channel 3)

Channel 3 | 3

Voltage Level (+/-25.0 V)

-5,000

Measurements

Actual Voltage Level (V)

1,282

Actual Current Level (A)

0,011

Actual Voltage Level (V)

-5,005

Actual Current Level (A)

2,991E-5

The program is used to reach the instrument using GPIB serial communication with VISA. Then the voltages for channel 1 and channel 3 are chosen, and the output of the device is read and printed on the program every 5 minutes. The current in channel 1 was also limited to prevent the diodes inside the device to burn. The output voltages are also recorded to an Excel file to monitor that the device is still functioning. The counter on the bottom is used to calculate that sufficient amount of readings is reached.

Appendix 3 Photos of the test setup