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VCO for PLL Frequency Synthesizer

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<p>Phase Locked loops have become very vital in most communication systems today. They are used in radio receivers, mobile telephones, GPS systems. They are also used to generate frequencies comparable to the accuracy of a crystal oscillator. Considering the scope of this single circuit, this thesis is focused in the design of a Voltage Controlled Oscillator (VCO) that can be use in the system.</p> <p>The design of the VCO was done with NI Multisim software and simulated with a voltage range of 0V to 2V, also the results were compared with that of real components in same voltage range and finally was milled on a printed circuit board.</p> <p>The simulation and measurements were successful, the phase noise, tuning sensitivity and oscillation frequency range (tuning gain) were measured successfully and the results were compared as required.</p> <p>The results are a clear analysis of the comparison between theory and practice. Phase locked loop on itself is a very important research topic as it covers many disciplines of electrical and electronic engineering such as Communication theory, Control theory, Signal analysis, Noise Characterisation, Digital circuit design to name but a few. With further studies the prototype of the VCO circuit could be attain with a better result.</p>	
Keywords	VCO, PLL Frequency Synthesizer

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Acronyms

PLL	Phase Locked Loop
VCO	Voltage Controlled Oscillator
PFD	Phase Frequency Detector
XOR	Exclusive OR gate
DPLL	Digital Phase Locked Loop
APLL	Analogue Phase Locked Loop
CP	Charge-Pump
K_{VCO}	Voltage Controlled Oscillator Tuning Sensitivity
FM	Frequency Modulation
PM	Pulse Modulation
Nano (n)	10^{-9}
Mega (M)	10^6
Farad (F)	Capacitor unit
Henry (H)	Inductor unit
DC	Direct Current
AC	Alternating Current
NI	National Instruments
PCB	Printed Circuit Board

1 Introduction

Phase Locked Loops (PLL) Frequency synthesizer is an electronic system that can properly generate any range of frequencies from a single fixed time-base or oscillator. It can combine frequency multiplication, frequency division, and frequency mixing (Frequency mixing process generates sum and difference frequencies) operations to produce the desired output signal. It is a new class of circuit that is used primarily in communication system applications. It is suitable for a wide variety of applications, such as AM radio receivers, frequency demodulators, multipliers, dividers, and other items of frequency electronics.

This study will cover the ways in which frequency synthesizers can be made from phase locked loops (PLL), the various components that make-up the PLL frequency synthesizer with a focus on the design of a voltage controlled oscillator, which is a very vital part of a PLL system and certain considerations needs to be taken in order to design a good oscillator.

VCO turns to be one of the most important parts in Electronics and Communication today, it is able to produce an oscillating frequency from an input voltage. Apart from it being a very import component in a PLL system, it is also use in Frequency Modulator (FM) and Pulse Modulators (PM).

This study is carried out on simulation software called NI Multisim. Multisim is a software use to design and simulate electrical and electronic circuits. The VCO is designed using this software; measurements are taken from this software and compared with measurements taken from real components placed on a circuit board.

2 Theory of Phase Locked Loop (PLL) Frequency Synthesizer

2.1 Digital PLL Synthesizer

Digital PLL (DPLL) synthesizer is at the origin of most single loop synthesizers. It requires placing a digital divider in the loop between the VCO and the phase detector, thereby making it able to run at a higher frequency than that of the phase detector. This

will in turn make the VCO frequency to be divided by the division ratio of the divider, for instance n , and the VCO will run at n times the phase comparison frequency. Changing the division ratio of the divider, will also change the output frequency of the oscillator. This makes the frequency synthesizer programmable, as shown in figure 1 schematic of the digital frequency synthesizer below.

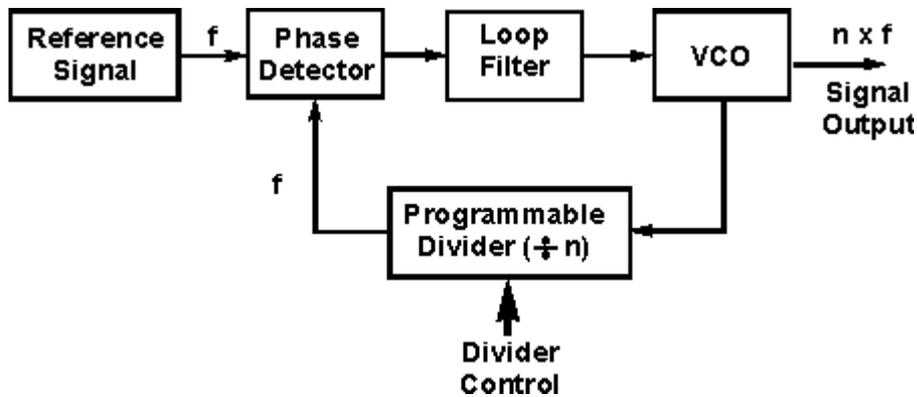


Figure 1 Basic digital frequency synthesizer, Adapted from Fmuser [1].

2.2 Analogue PLL Synthesizer

Frequency synthesizer of this type involves putting a mixer into the PLL between the VCO and the phase detector. Introducing an external signal at the other terminal of the mixer, a fixed offset equal to that of the external frequency is introduced into the loop, as indicated in figure 2 below.

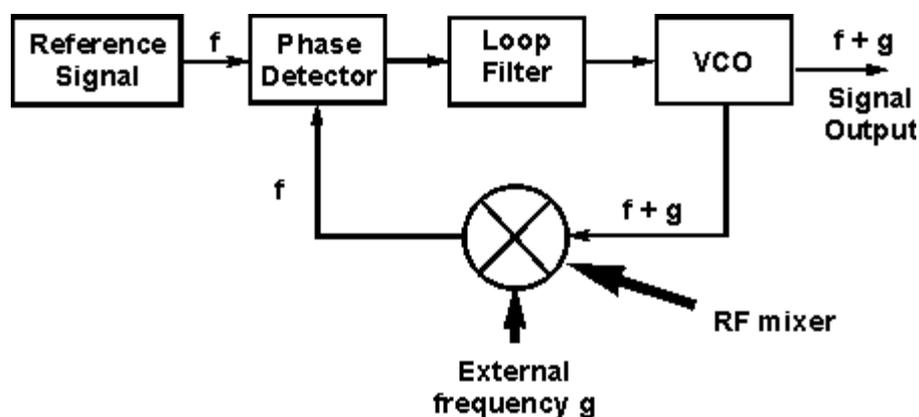


Figure 2 Basic analogue frequency synthesizer, Adapted from Fmuser [1]

When the loop is in lock the signals entering the phase detector are at exactly the same frequencies. The mixer adds an offset equal to the frequency of the signal enter-

ing the other port of the mixer. If the reference oscillator is operating at a frequency of 10 MHz and the external signal is at 15 MHz then the VCO must operate at either 5 MHz or 25 MHz for instance. Normally the loop is set up so that mixer changes the frequency down and if this is the case then the oscillator will be operating at 25 MHz. To be able to produce high quality frequency synthesizers with very cost effective and with high levels of performance, most synthesizers uses both digital and analog frequency synthesizer techniques.

2.3 Phase Locked Loop Operation

Most frequency synthesizers are based around a phase locked loop (PLL). PLL is a feedback control system that generates an output signal whose phase is related to the phase of an input reference signal. As the name suggests, it operates by trying to lock to the phase of a very accurate input signal via the use of its negative feedback path. PLL consist of three building block; Phase Detector, Loop Filter and Voltage Controlled Oscillator (VCO), as shown in figure 3 below. A reference oscillator is sometimes included in the block diagram, even though is not compulsorily part of the loop, but a reference signal is required for its operation.

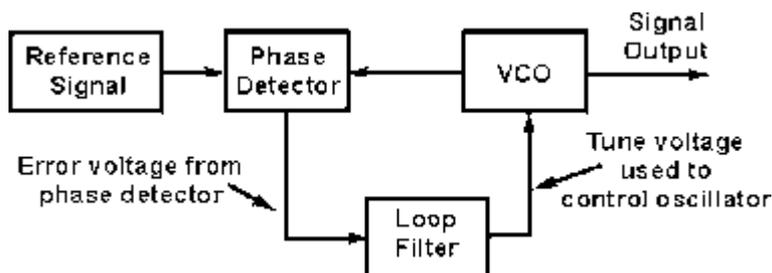


Figure 3: Phase Locked loop basic diagram, Modified from Fmuser [1].

In figure 3 above, the VCO produces a signal which is send through the phase detector where the phase is been compared with the reference signal, hence a difference or error voltage is produced, resulting to the phase difference between the two signals. The error voltage that is coming from the phase detector goes through the loop filter, which filters any impurities and high frequency segments from the signal. Later, this error voltage is sent to the control terminal of the VCO which uses it as its tuning voltage. This voltage helps to reduce the phase difference and the frequency between the two signals. At the beginning, this loop will be out of lock, where the error voltage will

drag the frequency of the VCO towards the direction of the reference, till the error can no longer be minimize any further and the loop is locked.

At locked state, a steady state error voltage is build. An amplifier is used between the phase detector and the VCO, to minimize the error between the signals to smaller levels. Nevertheless, small patches of voltage will remain at the control terminal of the VCO as this is what leads to a correct frequency. The phase difference between reference signal and VCO remain constant as shown in figure 4 below, because of the presents of the steady error voltage. Since the phases between these two signals are constant, it therefore means the two signals are on same frequency.

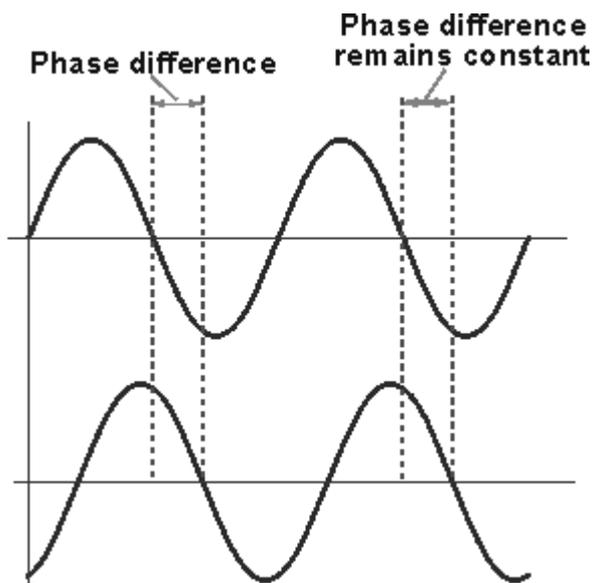


Figure 4: Phase difference between signals, Modified from Ian Poole [2].

2.4 Phase Detector

Phase detector is a frequency mixer, analog multiplier or logic circuit that compares two input signals and produces an error signal which is proportional to their phase difference. It is the key component of a phase locked loop. There are two categories of phase detectors:

- ❖ Phase only sensitive detectors
- ❖ Phase-frequency detectors

2.4.1 Phase Only Sensitive Detectors.

This is the most uncomplicated form of Phase detectors. They only produce an output that corresponds to the phase difference between the two signals. They produce a constant voltage just as the phase differences between the two incoming signals are stable. In the other sense, a frequency difference between the two signals will cause them to produce a varying voltage. One example of a phase detector that can be used is an Exclusive OR circuit.

The exclusive OR, XOR phase detector circuit can produce a highly functional simple phase detector for some applications. Figure 5 illustrates the schematic of an Exclusive OR phase detector.

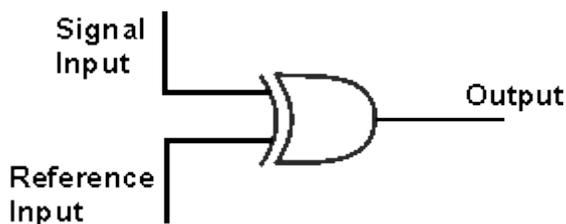


Figure 5 Exclusive OR phase detector, Modified from Ian Poole [2].

The operations of the exclusive OR phase detector is illustrated in figure 6 below:

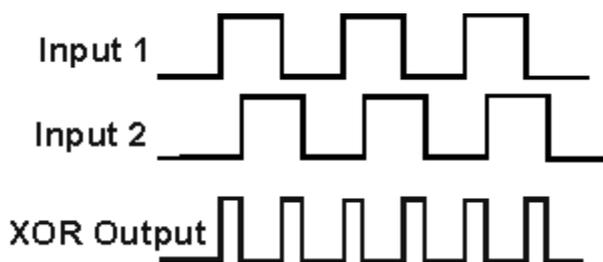


Figure 6 XOR phase detector waveforms, Modified from Ian Poole [2].

As shown in the waveforms above, the XOR gate is seen to be used as a straightforward but productive phase detector.

One of its drawbacks is that, they are sensitive to the clock duty cycle. This implies that a steady duty cycle of 1:1 should be used. This will lock with a phase error if the input duty cycles are not 50%.

2.4.2 Phase-Frequency Detectors

One advantage of this form of detector is that when the phase difference is in the middle of $\pm 180^\circ$, a voltage corresponding to the phase difference is produced. Above this the circuit will limit at one of the opposites. Hence no AC component is going to be built when the loop is out of lock; therefore, the output from the phase detector is going to pass via the filter to bring the PLL into lock. Some examples of this type of phase-frequency detector are the Dual D type phase comparator and the Edge triggered JK flip flop phase frequency detector.

2.5 Loop Filter

The loop filter is responsible for the filtering operation of the error voltage that comes from the phase detector. The phase detector output is made up of a dc component placed above the ac component. The low pass filter helps to filter out the unwanted ac component, since it cannot be used as an input to the VCO. The performance of the loop is also determined by the loop filter as it is one of the key components in the PLL. The poles introduced by the loop filter to the transfer function of the PLL are in turn used in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancellation, a loop filter of order 2 or more are used in most of the critical application PLL circuits. [3]

2.5.1 Loop Stability

When designing any system, one of the main things that needs to come to your mind is the stability of that system particularly when it comes to designing an oscillator be it for frequency synthesis or phase lock loop or any electronic device. Phase locked loop in this case needs to be stable in every condition under test. In order to attain this goal, the loop gain and filter components have to be well calculated so that the loop stability can be attained at all operating conditions.

2.5.2 Loop Filter Bandwidth

Loop filter bandwidth also affects the stability of the loop and reduces the lock time of a PLL system if it is increased beyond its limit. As mentioned in Analog Devices [4], loop filter normally is 1/10 of the phase frequency detector (PFD) frequency (channel spacing), which implies that the bandwidth should not be over PFD/5. Figure 7 below shows

one of the most common types of filter (third order integrator). The R2C3 pole provides extra attenuation for spurious products.

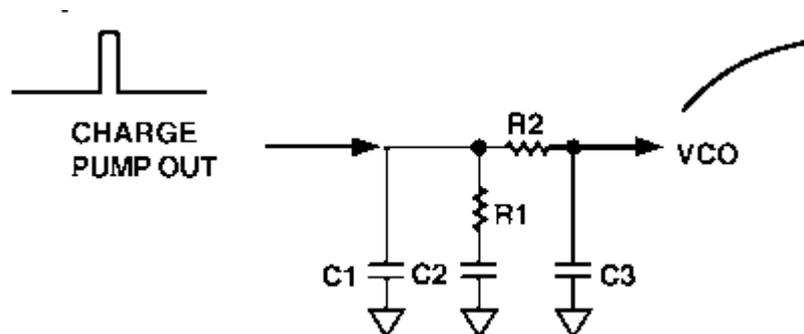


Figure 7 A third-order loop filter, Adapted from Analog Devices; PLL Synthesizer [4].

A loop filter's can be doubled, to do this we need to double either the PFD frequency or the charge-pump (CP) current. If the actual K_1 (tuning gain) of the VCO is greatly higher than the nominal K_1 used in designing a loop filter, the loop filter will be significantly be wider than expected. There is a great challenge in designing a wideband PLL because of the variation of the loop bandwidth with the presents of K_1 . The easiest way to solve this situation of the loop bandwidth caused by the K_1 variation is by increasing or decreasing the programmable charge-pump current. [4]

3 Voltage Controlled Oscillator (VCO)

3.1 Introduction

One of the fundamental parts of electronics and communication today is an oscillator, whose oscillation frequency is controlled by a voltage input [5]. They are used for clock generation in microprocessors to frequency translation in mobile applications, it is also an important element in frequency synthesizers. Due to the demands in electronics and communication for a good performance PLL with voltage controlled oscillation being the key components, researchers have been focusing on designing a good performance VCO, which has become extremely important.

3.2 VCO for Phase Locked Loops

VCO is a key building block for phase locked loops (PLLs). They can be use in micro-processor to generate clocks, in optical transmission systems they can be use in clock and data recovery, while in wireless systems such as radio, they are used for frequency synthesising. For the PLL frequency range to be covered entirely, the important factor for the VCO will be its wide tuning range. The phase noise of the VCO will also be taken into considerations due to the fact that when the loop is locked, the noise generated by the VCO at the centre of the oscillation frequency will be filtered out by the loop bandwidth. Within the PLL or frequency synthesizer, the performance of VCO is of greatest importance, because the performance determines many of the overall performance characteristics of the overall synthesizer. [2]

3.3 VCO Design Requirements

The key requirements for a VCO consist of; tuning range, oscillation frequency, phase noise, tuning gain, and power consumption. The VCO must be able to tune based on the requirements of the application to be use in and its oscillation frequency, the frequency of oscillation is determined by the application in which the VCO is to be use, in this case a PLL system. The tuning gain is also important, and is measured in terms of volts per hertz (or V/MHz). It is the tuning shift for a given change in voltage.

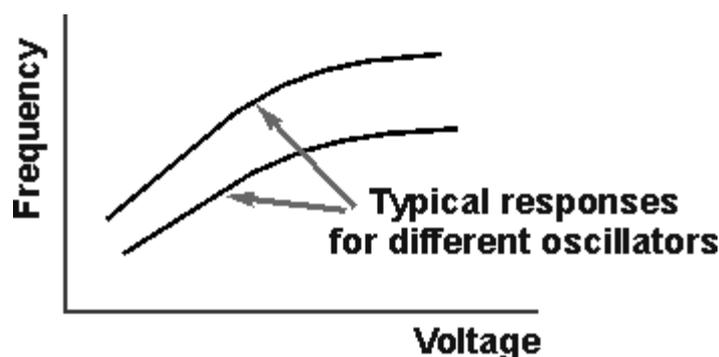


Figure 8 VCO V/F curves, Modified from Ian Poole [2].

The VCO response curves as shown in figure 8 above can be seen to be relatively straight at lower frequencies. However they normally flatten out at higher voltages where the changes in capacitance from the varactor diodes reduce.

The phase noise is of importance when use in frequency synthesizer, the phase noise performance of the VCO determines many of the overall phase noise performance characteristics of the overall loop and overall synthesizer if use in one. Power consumption is always an important factor when designing any device for most applica-

tions, for instance in applications that uses battery for power supply will have the life span of the battery increase with a low power design. [2]

3.4 Oscillator Fundamentals

A simple oscillator produces a periodic output, usually sinusoidal waveforms, but for this to happen, some considerations and analysis are to be made for it to oscillate. We can start by considering a feedback system as shown in figure 9 below, the combination of an amplifier with gain $A(j\omega)$ and frequency dependent feedback loop;

$$H(j\omega) = \beta A \quad (1)$$

This leads to the expression,

$$\frac{V_o}{V_i} = \frac{A}{1-\beta A} \quad (2)$$

Hence the oscillator will oscillate when,

$$\beta A = 1 \quad (3)$$

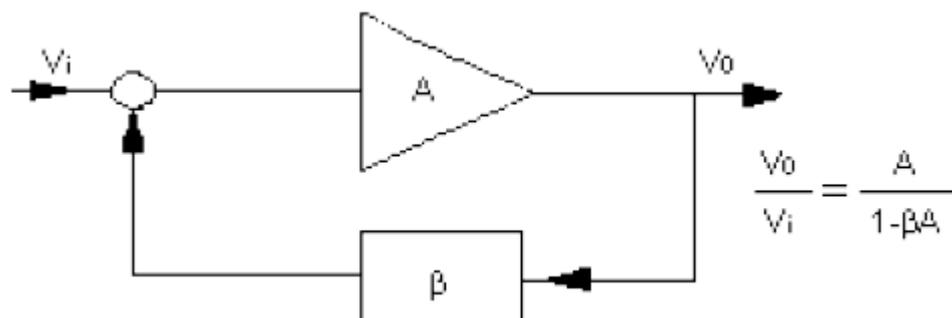


Figure 9 oscillator modelled as a combination of an amplifier and a Feedback, Reprinted from Mini-Circuits [6].

The phase shift around the loop must be 360 degrees at the frequency of oscillation with a unity open loop gain. The common emitter circuit provides 180 degree phase shift. If the circuit is used with feedback from collector to base, the feedback circuit must provide additional 180 degree phase shift. If a common base is used, there is no

phase shift between the emitter and collector signals, the feedback circuit must provide either 0 degree or full 360 degree phase shift [6].

3.4.1 Oscillator Design Examples

To generate a negative resistance, capacitances are placed at the base and emitter of a bipolar transistor and at the emitter and ground of the transistor; this can be shown on the figure below,

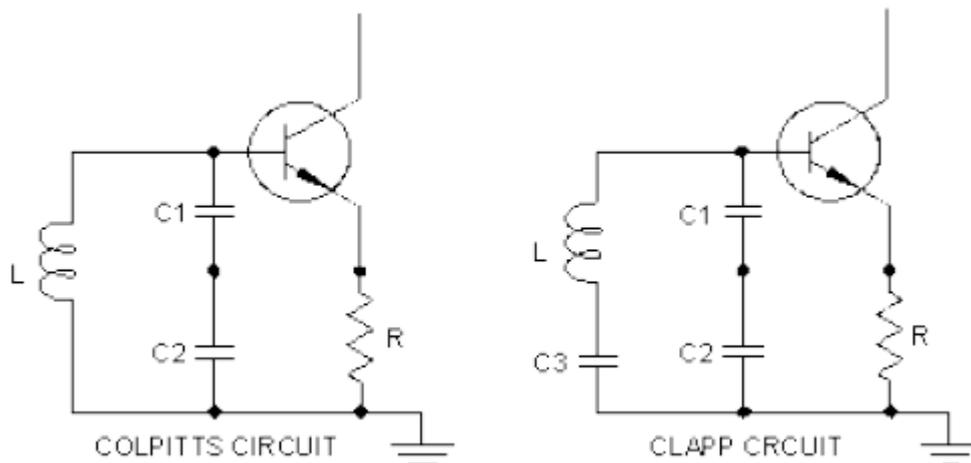


Figure 10 Colpitts and Clapp oscillator circuits, Reprinted from Mini-Circuits [6].

The system includes a resonant circuit to ensure that the oscillation occurs on a given frequency. The resonant circuit can be one of a number of configurations from an LC resonant circuit in either series or parallel resonance dependent upon the circuit [2]. The circuits in figure 10 above is preferred for high stability oscillator circuits, because of the ease with which the resonator may be isolated from the load [6]

3.4.2 CLAPP VCO Equivalent Circuit

Clapp is one of the commonly used VCO circuit, it operate as an oscillator, because it is made up of an active device such as a bipolar transistors, and can generates a negative resistance as mentioned in section 3.4.1 above. The resonant circuit of clapp is made up of an inductor and capacitor in series as shown in figure 12 (a) and (b) below.

Condition for resonance is;

$$f^2 = \frac{1}{4\pi^2 LC_3} \quad (4)$$

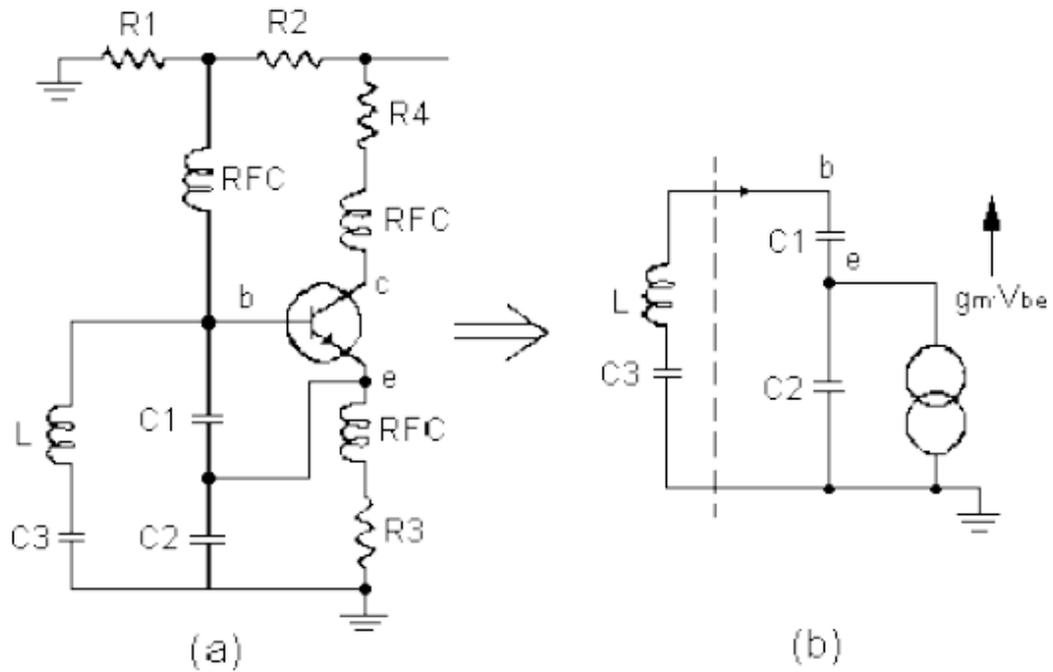


Figure 11 Oscillator design evaluation for CLAPP circuit, Reprinted from Mini-Circuits [6].

The figure above comprises of the Clapp circuit (a) and its small signal equivalent circuit (b). The design equations are derived below based on the equivalent circuit (b). The input impedance seen to the right of the dotted line in figure 11b above is given by

$$V = \frac{i}{j\omega C_1} + \frac{i + g_m V_{be}}{j\omega C_2} \quad (5)$$

Where

$$V_{be} = \frac{i}{j\omega C_1} \quad (6)$$

$$\frac{V}{i} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2} \quad (7)$$

The quantity $\left(\frac{g_m}{\omega^2 C_1 C_2}\right)$ is negative indicating a negative resistance component, hence to maintain oscillations [6],

$$r < \frac{g_m}{\omega^2 C_1 C_2} \quad (8)$$

Where r , is the series resistance of the resonator.

Frequency of oscillation is given by;

$$(\omega^2)L = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \quad (9)$$

For oscillation to take place, the ratio C_1/C_2 is selected to be greater than 1. A VCO is obtained by replacing a fixed capacitor such as C_3 with a varactor diode.

3.5 VCO Varactor

Varactor diode is a very important component in a VCO, so some measures need to be considered when dealing with it, so that it should not be forward bias, in turn reducing the quality factor (Q) and hence spurious signals will be increased. Two types can be use within the VCO namely the Abrupt and Hyper-abrupt.

3.5.1 Abrupt Varactor Diode

This abrupt diode offer higher quality factor and lower phase noise within the VCO, but in terms of the tuning range, is relatively low and require a high tuning voltage to yield the required tuning range.

3.5.2 Hyper-abrupt Varactor Diode

Their voltage is linear, hence a linear tuning characteristic can be realised. They have a relatively wide tuning range with lower tuning voltage, but the quality factor offered by them is low. Therefore, their phase noise is not the best.

3.6 VCO Tuning Sensitivity

Following up from section 3.5 about varactors above, their capacitance is related to the bias voltage by the following equation as gathered from mini circuit website [6];

$$C = \frac{A}{(V_R + \phi)^n} \quad (10)$$

A = constant, V_R = applied reverse bias voltage, ϕ is the built-in potential which is 0.7 for silicon diodes.

$$C = \frac{A}{V^n} \quad (11)$$

A is the capacitance of the diode when V is 1volt and n is a number between 0.3 and 0.6, can be up to 2 for abrupt junction. The tank circuit of a VCO has a parallel tuned circuit consisting of an inductance L, fixed capacitance C_f , and varactor diode C. Frequency of oscillation may be as follow,

$$\frac{1}{\omega^2} = L(C_f + AV^{-n}) \quad (12)$$

Let ω_o be the angular frequency of the unmodulated carrier and V_o and C_o be the corresponding values of V and C. So from equation (12) we have

$$L = \frac{1}{\omega_o^2(C_f + C_o)} \quad (13)$$

If V_o is modulated by a small voltage V, the carrier will be deviated by a small frequency $\partial\omega$.

$$(\omega_o + \partial\omega)^{-2} = L[C_f + A(V_o + \partial V)^{-n}] \quad (14)$$

Substituting (13) into (14), we have

$$\left(1 + \frac{\partial\omega}{\omega_o}\right)^{-2} = \frac{C_f + C_o \left(1 + \frac{\partial V}{V_o}\right)^{-n}}{C_f + C_o} \quad (15)$$

The oscillator tuning sensitivity K (K_{VCO}) can therefore be;

$$K_1 = \frac{d\omega}{dv} = \frac{n\omega_o}{2V_o} \left(\frac{C_o}{C_f + C_o} \right) \quad (16)$$

The units of K_1 is rad/sec/volt [9]

3.7 VCO Circuit

VCO comprised of a tuneable voltage that is applied to a varactor diode. The varactor is made from a variable capacitor (as described in section 3.5 above). A bipolar transistor is used as the active device instead of field effect transistor (FET) because of its low input impedance and is current driven, as compared to the high input impedance and voltage driven of a FET. Bipolar transistors have low level of flicker noise and are suitable for phase noise performance. Figure 12 below illustrates the schematic of a VCO,

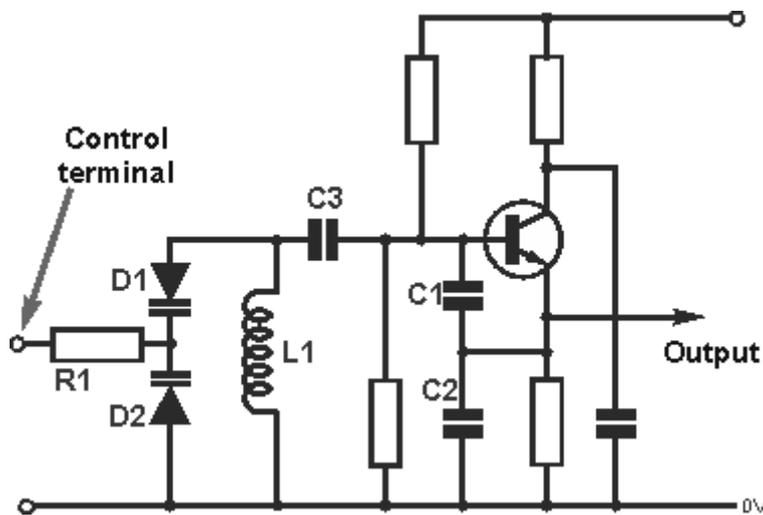


Figure 12 Voltage Controlled Oscillator Circuit, Modified from Ian Poole [2].

In other to block the dc from the inductor, a series capacitor C3 is used, if not it will short to ground and the bias arrangement will be upset. For wideband, series back-to-back varactors are connected instead of a single one. This helps to reduce distortion and the effect of fringing and mounting capacitances [8].

3.8 VCO Phase Noise

Phase noise can be defined as the short-term random frequency fluctuations of a signal. Frequency stability is of great importance in any oscillator design. The focus of the frequency stability will base on the short-term and long-term stability. Long-term is how the output signal varies over a long period of time, specified as a ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in dB. On the other hand short-term stability is the variations that occur over a period of seconds or less. Figure 13 below shows the short-term stability of a signal examined with a spectrum analyser. [12]

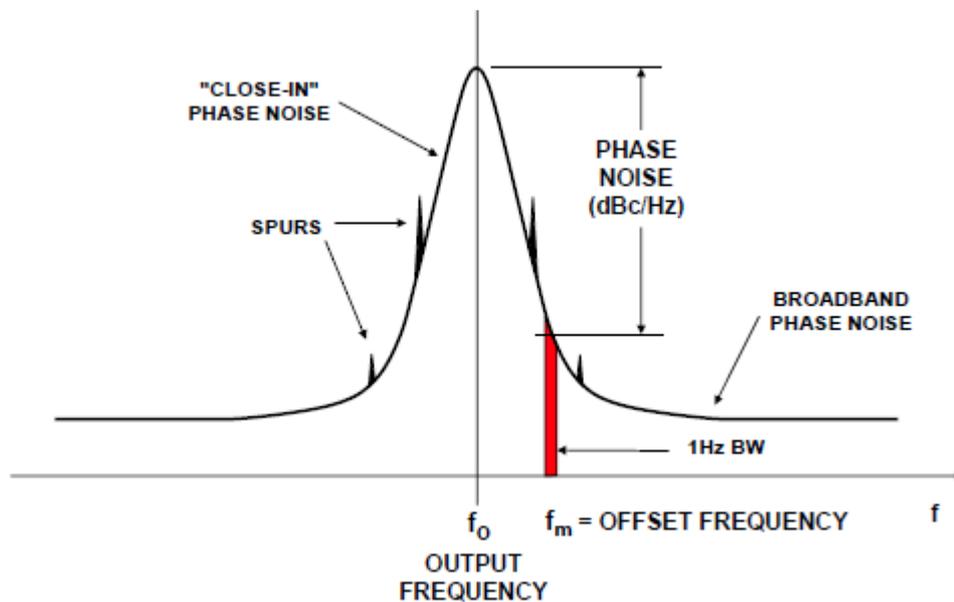


Figure 13 Oscillator Phase Noise and Spurs, Reprinted from Analog Devices; Fundamentals of PLL [12].

The source of phase noise in an oscillator is due to thermal and flicker or $1/f$ noise. This is also characterised by its single-sideband phase noise as shown in figure 14 below.

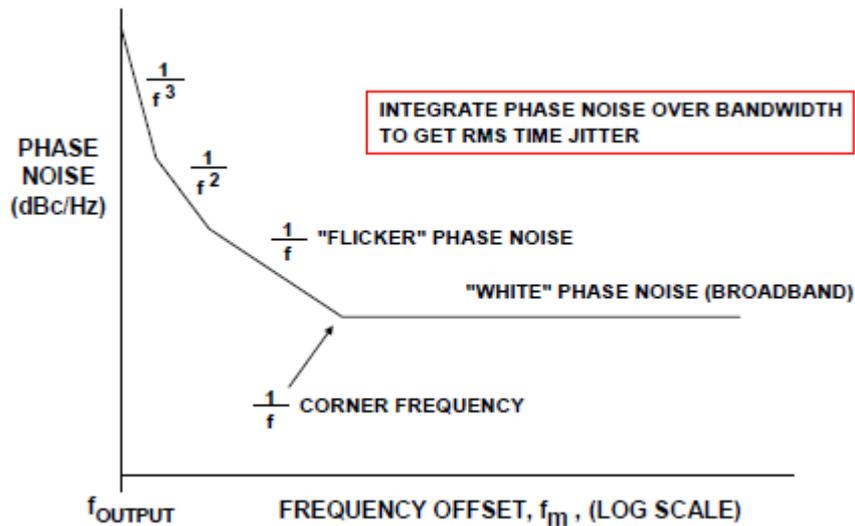


Figure 14 Phase Noise in dBc/Hz versus Frequency Offset from Output Frequency, Reprinted from Analog Devices; Fundamental of PLL [12].

As can be seen in the above figure, the phase noise curve is somewhat analogous to the input voltage noise spectral density of an amplifier. Like amplifier voltage noise, low $1/f$ corner frequencies are highly desirable in an oscillator. [12]

4 Designs and Simulations

The design of the VCO was done with an NI Multisim version 13. First a calculation was done in order to select the components that will be needed for the design. From the theory gathered from section 3.4.2, the selection of the capacitor was based on that theory that for the oscillator to oscillate, the ratio of $C1/C2$ must be greater than one was applied and in section 3.5 it was mentioned that in order to block the dc from the inductor, a series capacitor $C3$ is used, if not it will short to ground and the bias arrangement will be upset, this is better achieved if we set the value of $C3$ to be greater than those of $C1$ and $C2$. Also an inductor value was chosen to have a better oscillation and also form part of the resonant circuit. Figure 15 illustrates the design schematics.

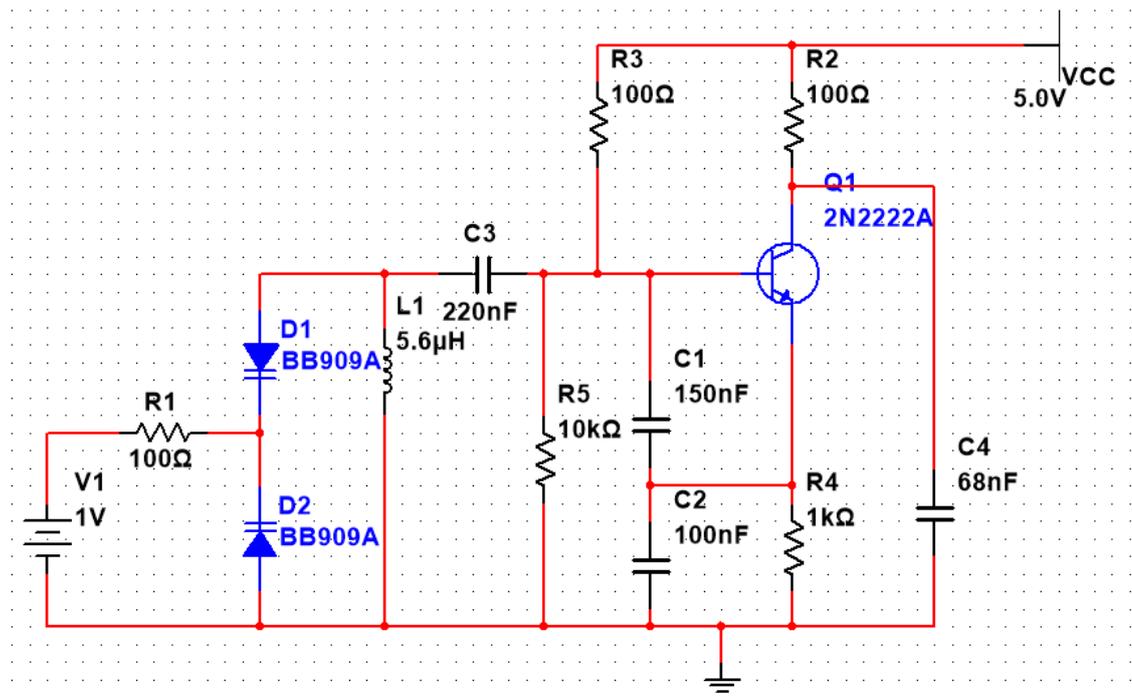


Figure 15 VCO design Schematic.

The values of the resistors are chosen for better biasing, a BB909A varactor diodes were for back-to-back connect to produce wideband oscillation, and a bipolar transistor of type 2N2222A was used because of its low impedance and current driven characteristics its possess. This circuit is powered with a Vcc of 5.0V, and is tune with different values of voltages at the input.

The varactor diode is separated from the control line from the phase detector by R1. The resistor R2 at the collector terminal affects the oscillator loop gain. As in a common collector amplifier, the lower the impedance in the collector circuit the more loop gain the circuit will have. The R2 resistor at the emitter terminal is used for current feedback hence provides a stable DC bias point that will be independent of the beta of the transistor. [8]

4.1 Design Calculations

Using equation 4 and equation 9, we can calculate the exact values of the resonance frequency and the VCO frequency respectively, including the varactor diodes values. In the design the following values where assign to the components; C1 = 150nF, C2 =

100nF, $C_3 = 220\text{nF}$, $D_1=31\text{pF}$, $D_2=31\text{pF}$ and $L = L_1 = 5.6\mu\text{H}$, as can be seen in figure 15 above.

From equation 4, the Resonant Frequency is calculated as follows;

$$F = \sqrt{\frac{1}{4\pi^2 L(C_3 + D_T)}} \quad (17)$$

Where $D_T = D_1 + D_2 = 62\text{pF}$

This implies,

$$F = \sqrt{\frac{1}{4(3.14^2)(5.6\mu\text{H})(220\text{nF}+62\text{pF})}} \quad (18)$$

Hence $F = 143.44 \text{ KHz}$

From equation 9, we calculate the VCO Frequency as follows;

$$(\omega^2)L = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{(C_3 + D_T)} \quad (19)$$

$$F_{vco} = \sqrt{\frac{C_2(C_3 + D_T) + C_1(C_3 + D_T) + C_1 C_2}{4\pi^2 L C_1 C_2 (C_3 + D_T)}} \quad (20)$$

This implies,

$$F_{vco} = \sqrt{\frac{(100\text{nF}*(220\text{nF}+62\text{pF}))+(150\text{nF}*(220\text{nF}+62\text{pF}))+ (150\text{nF}*100\text{nF})}{4*3.14^2*5.6\mu\text{H}*150\text{nF}*100\text{nF}*(220\text{nF}+62\text{pF})}} \quad (21)$$

Hence $F_{vco} = 309.9 \text{ KHz}$

4.2 Simulation setup

The simulation is done with NI Multisim Agilent 54622D Mixed Signal Oscilloscope. The output of the circuit is taken from emitter section of the transistor and ground, and it is connected to the input port of the oscilloscope as shown in figure 16 below. The simulation is carried out at a tuning voltage of 0-2V as specified for the study requirements.

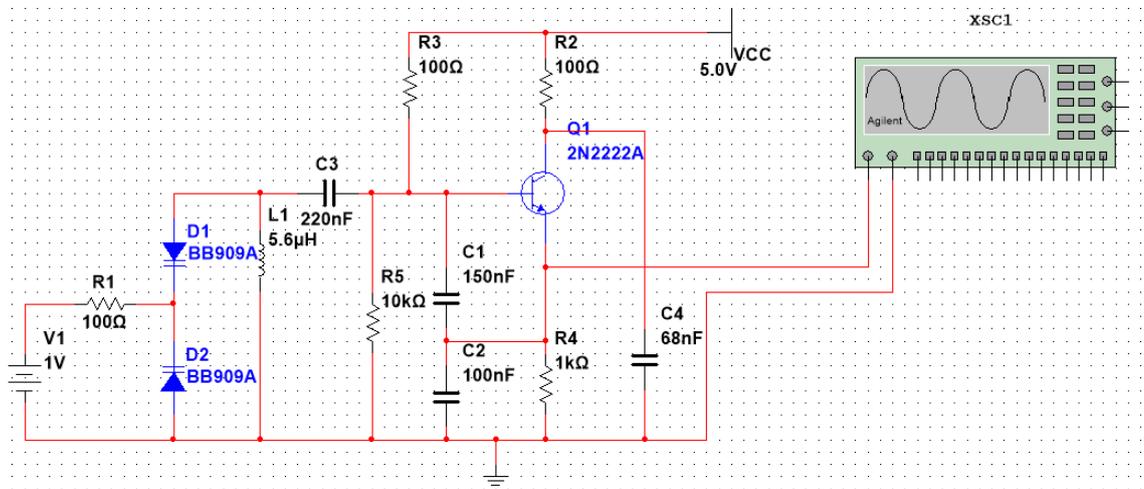


Figure 16 simulation setup schematic.

Figure 17 below illustrates the output waveform of the VCO frequency on the Agilent Oscilloscope, with an output frequency of 295.89 KHz at a tuning voltage of 1V, running at a time division of $0.2\mu\text{s}$ and a voltage division of 69.29mV.

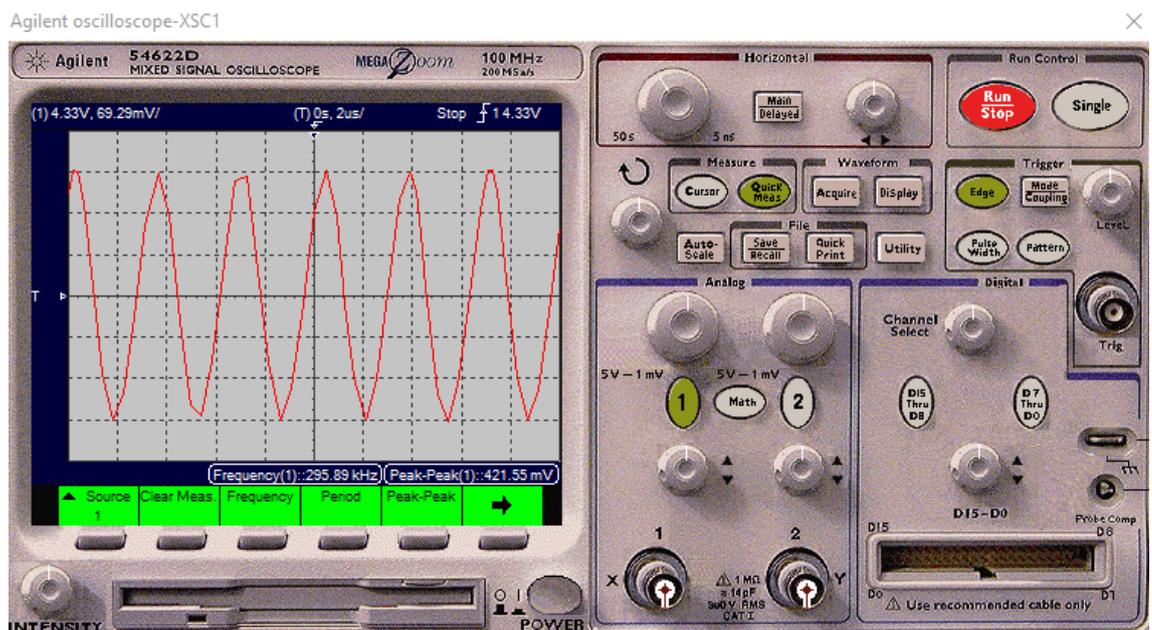


Figure 17 Simulation result on Agilent Oscilloscope.

It can be seen that the simulated value differs from the calculated value by 14.01 KHz. This difference can be due to the fact that the simulation takes into account all the components in the system that causes the frequency to be smaller than that of the calculated value.

5 Measurements and Results

The measurements for this study was carried out in three parts and graphs plotted to display the results, which is later compared with other results. From the VCO simulation carried out at tuning range of 0-2V, data were captured to plot graphs of output frequency to control voltage and tuning sensitivity (K1) to control voltage, and finally Measurement of the VCO phase noise is done.

5.1 Control Voltage to VCO Frequency Measure (V/F) Curve

Data are capture from the simulation as shown in table 1 below. These data are then plotted as shown in figure 18 below. This is called VCO tuning gain and is measured in V/KHz, it is the tuning shift for a given change in voltage, details of how these values are generated can be found at Appendix 1A below.

Table 1 V/F captured data.

Control Voltage (V)	VCO Frequency (KHz)
0	292.56
0.5	294.26
1	295.89
1.5	297.48
2	298.54

The above data are plotted on the graph below.

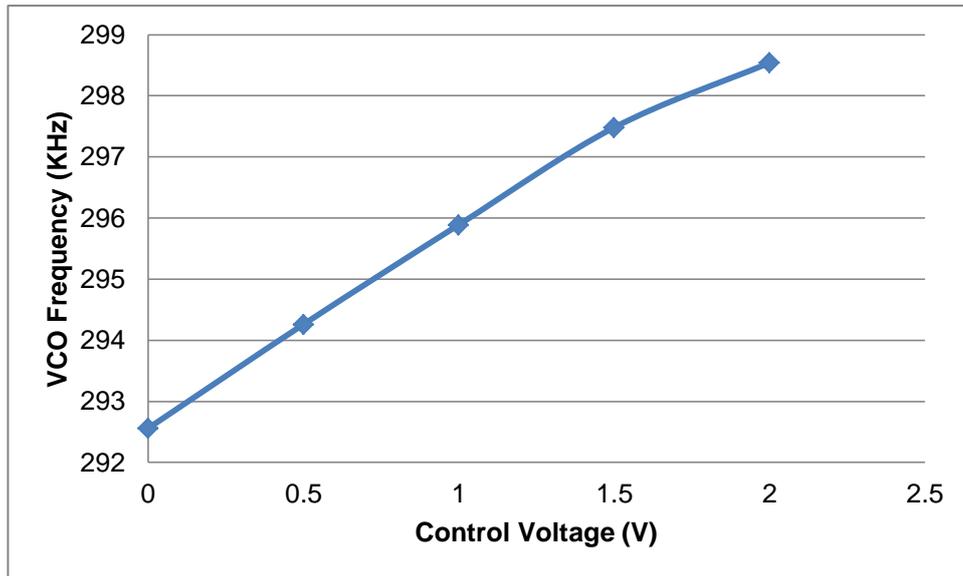


Figure 18 Graph of VCO V/F

It can be seen from the curve above that at lower frequencies the VCO response curve is relatively straight and as the voltage increases the curve looks to be getting flat which indicates the changes in capacitance from the varactor diodes is reducing. Normally this curve supposed to be relatively straight all through, but the bent from this curve indicates there are some spurious resonances which can cause the loop to be unstable.

5.2 Kvco Measurement

The measurement of the VCO tuning sensitivity is carried out from the simulation setup as shown in figure 16 and 17 above. Since the tuning sensitivity is defined as the frequency change per unit volt of tuning voltage, these measurements is done from different tune voltages and frequencies output as plotted in figure 18 above. The slope of the curve is the tuning sensitivity and is calculated from different tune voltage.

This relationship can be develop from equation 16 above, which is the change of output frequency to change in tune or control voltage, as shown in equation 22 below,

$$K_{vco} = \frac{\Delta F}{\Delta V} \quad (22)$$

From the above equation 22, different values of Kvco can be calculated at different tune voltage, and a graph is plotted to see the relationships they have.

By approximation from Figure 18,

$$\text{At } 0\text{V, } K_{vco1} = \frac{293-292}{0.2-0.2} = 2.5 \text{ KHz/V} \quad (23)$$

$$\text{At } 0.5\text{V, } K_{vco2} = \frac{297-295}{0.7-0.4} = 6.7 \text{ KHz/V} \quad (24)$$

$$\text{At } 1\text{V, } K_{vco3} = \frac{297-295}{1.3-0.7} = 3.3 \text{ KHz/V} \quad (25)$$

$$\text{At } 1.5\text{V, } K_{vco4} = \frac{297.9-297.1}{1.6-1.4} = 4.0 \text{ KHz/V} \quad (26)$$

$$\text{At } 2\text{V, } K_{vco5} = \frac{299-298}{2.3-1.8} = 2.0 \text{ KHz/V} \quad (27)$$

From equation 23 to 27 a tuning sensitivity table can be drawn and a graph plotted.

Table 2 Tuning sensitivity data

Control Voltage(V)	Kvco(KHz/V)
0	2.5
0.5	6.7
1	3.3
1.5	4.0
2	2.0

The above table is represented with the curve below.

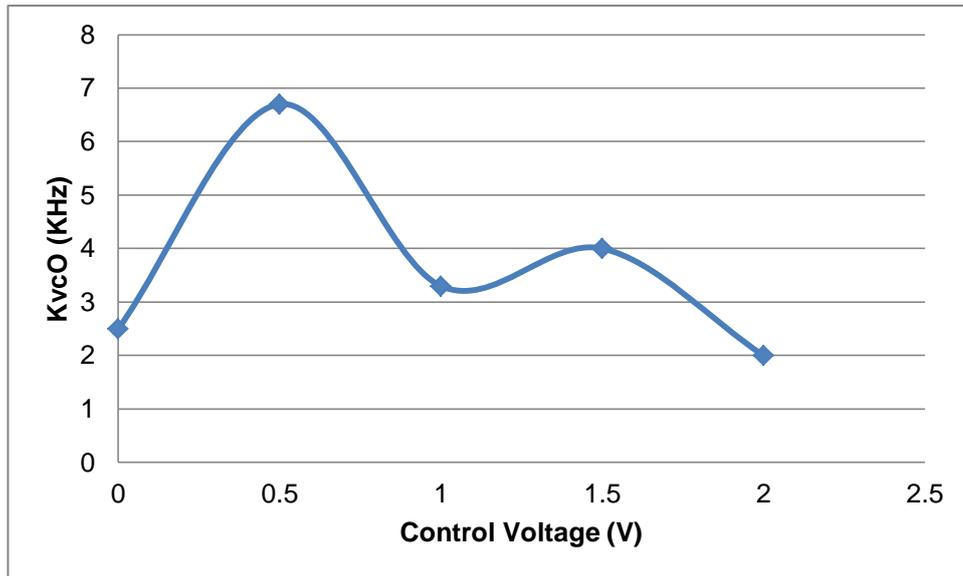


Figure 19 VCO Tuning Sensitivity curve.

As shown in the figure 19 above, the tuning sensitivity grows with the tune voltage but a sharp fall is noticed as the tune voltage gets higher and at some point a small rise is seen then a fall, this can cause the phase locked loop to become unstable if this is implemented into one.

5.3 Real Components Measurement

The measure was carried in the laboratory with the lab equipment like Oscilloscope and Spectrum Analyzer. The components were placed on a circuit board as show in figure 20 below. The result was analysed with the Oscilloscope and the Spectrum Analyzer and the Spectrum Analyzer the Phase Noise is measured.

Connecting both the Oscillator and the Analyzer at same time was not possible because the load was too much for the circuit to carry since it has very low voltage, so a buffer was implemented at the output of the oscillator, as can be seen in figure 20 below.

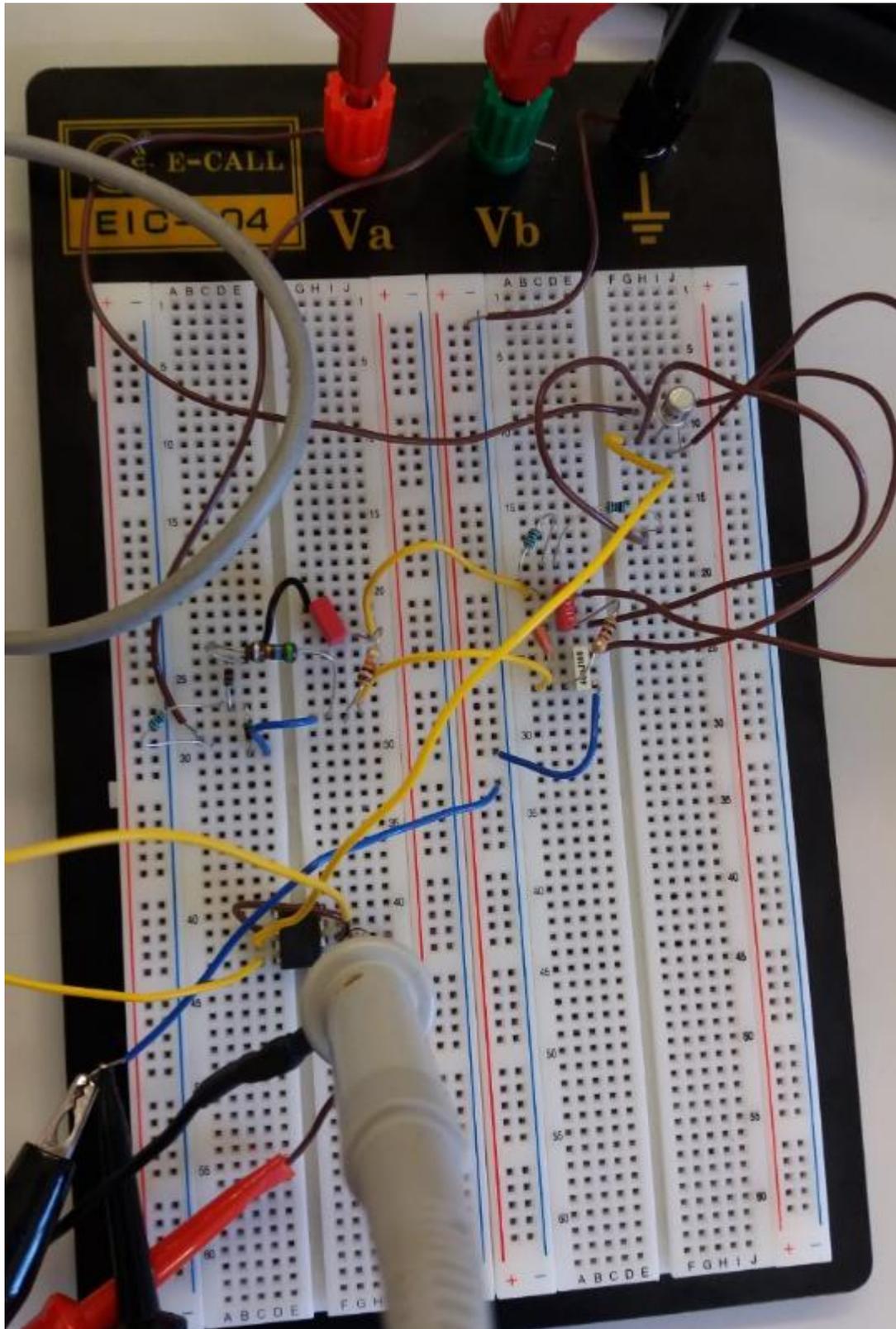


Figure 20 Real Component Measurement Setup

The waveform of the above circuit were captured in different forms, before placing the buffer and after placing the buffer (oscilloscope and spectrum analyser waveforms) and the results were both different as shown in figures below.

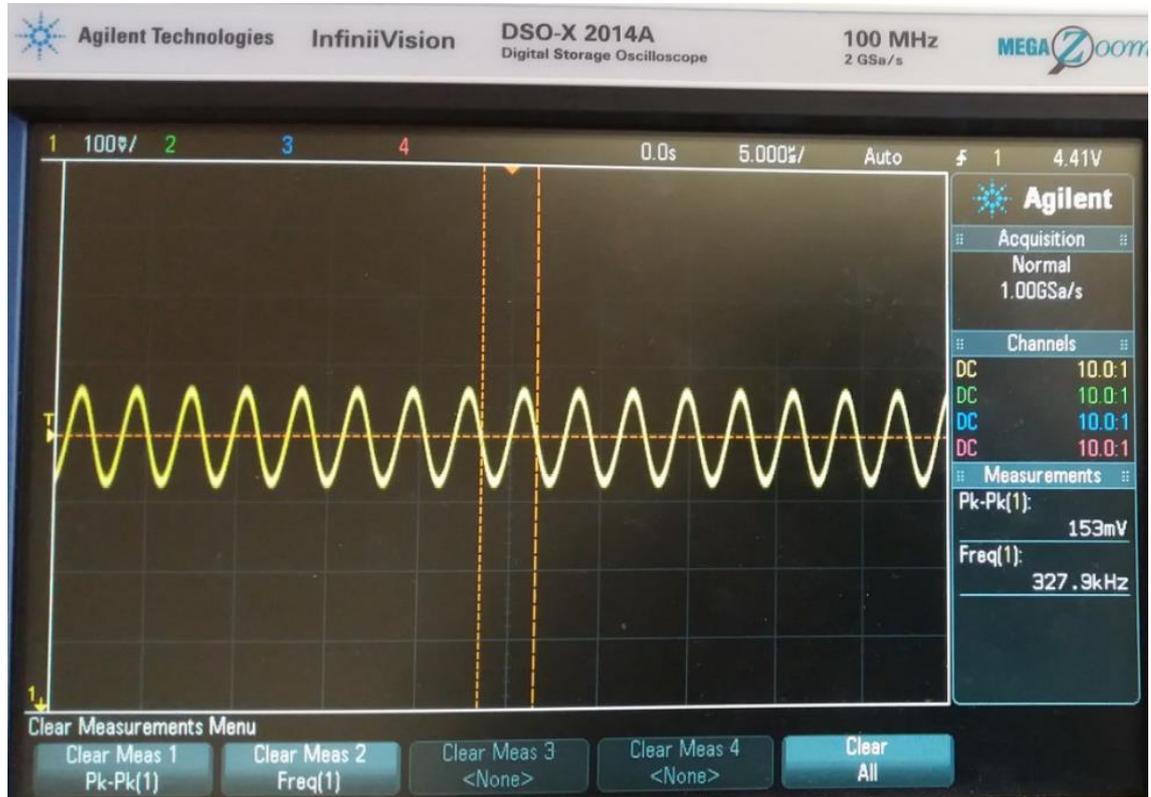


Figure 21 Measurement Waveform before placing the Buffer at 1V

Here the circuit is oscillating at a frequency of 327.9 KHz at 1V.



Figure 22 Oscilloscope Measurement Waveform after placing the Buffer at 1V

Here the oscilloscope is oscillating at a frequency of 376.7 KHz at 1V, which is different from that in figure 21 above because of the buffer placed at the output of the oscillator. Appendix 1B below illustrates the various waveforms at different input voltages.

Comparing this result with that of the simulated and calculated values, we can see that while the calculated value is at 309.9 KHz, the simulated value is at 295.85 KHz and the component value is at 376.7 KHz, there is a small difference in the results, and this is to show that theory and practice are very close together.

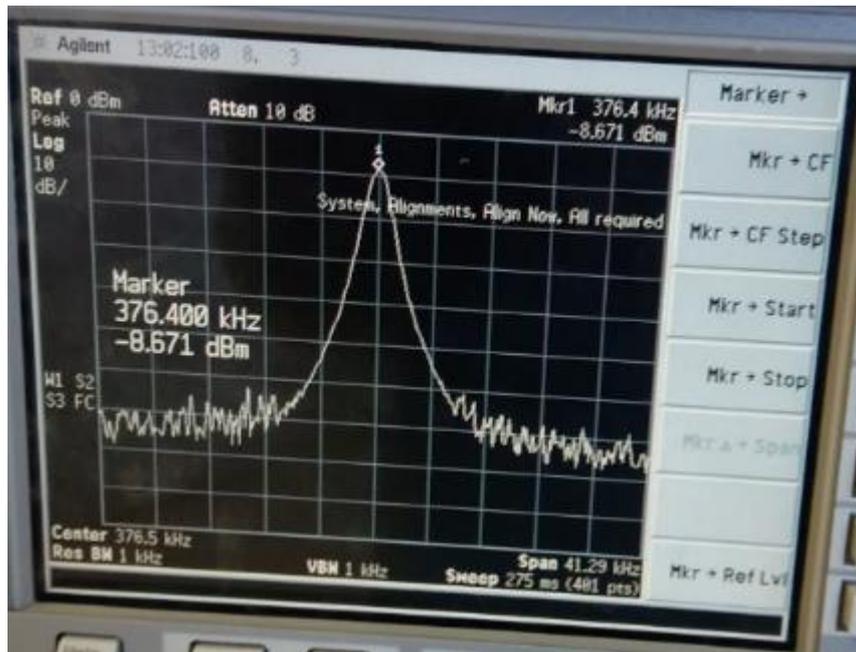


Figure 23 Spectrum Analyzer output signal at 1V

As seen in figure 22 and 23, there is a slight difference in the output frequency, this is because of the equipment type and their accuracy. Spectrum analyzer is used for observing signals and it looks at signals in frequency domain while oscilloscope looks at signals in the time domain. The results obtained from the Oscilloscope after placing the buffer will be used to calculate the tuning sensitivity (gain) and the VCO tuning gain. In appendix 2A below details of the spectrum analyzer captured signals are demonstrated.

5.3.1 VCO Tuning Gain

The table below shows the relationship between the control voltage and the output frequency obtained from the real component measurement, detailed waveforms can be found in appendix 1B below.

Table 3 V/F captured data

Control Voltage (V)	VCO Frequency (KHz)
0	375.8
0.5	376.2

1	376.7
1.5	376.9
2	377.9

The above Captured data are plotted on the graph below.

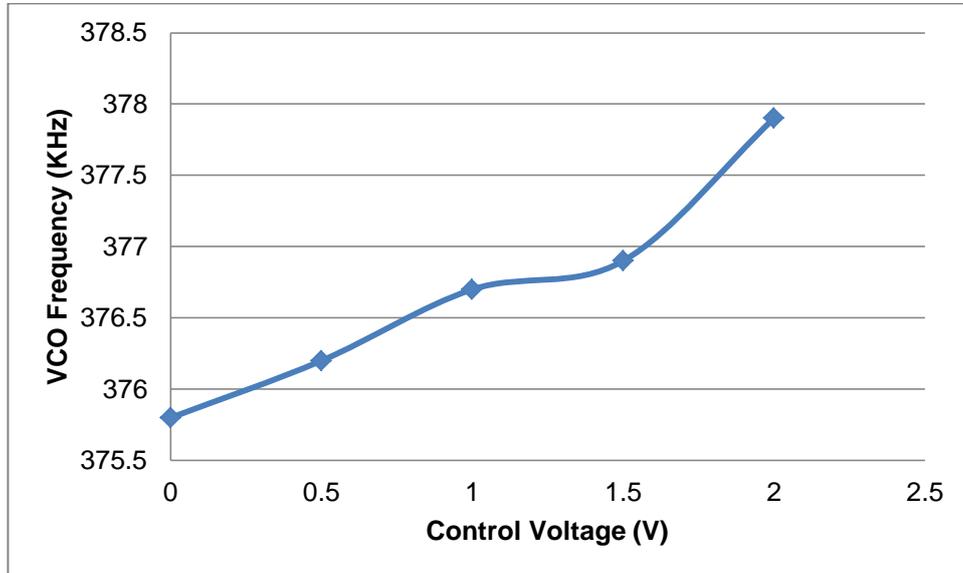


Figure 24 Graph of VCO V/F

At lower voltage we weakness a linear curve and after some point there is this dip in the curve, this is because of spurious signals in the circuit. Comparing this result with that of the simulated result above, the dip in that of the real component is too visible and dipper than that of the simulated curve, one reason can be of the external noise and delay that causes the signal to be unstable than the simulated signal.

5.3.2 VCO Tuning Sensitivity (Kvco)

The tuning sensitivity is calculated based on the relationship we saw in equation 22 above. The slope at various input voltages is estimated from figure 24 above, and the results are as follows;

$$\text{At } 0\text{V, } K_{vco1} = \frac{375.9-375.5}{0.2--0.2} = 1.0 \text{ KHz/V} \quad (28)$$

$$\text{At } 0.5\text{V, } K_{vco2} = \frac{376.4-376}{0.6-0.3} = 1.33 \text{ KHz/V} \quad (29)$$

$$\text{At 1V, } K_{vco3} = \frac{376.8-376.5}{1.2-0.8} = 0.75 \text{ KHz/V} \quad (30)$$

$$\text{At 1.5V, } K_{vco4} = \frac{377.1-376.8}{1.7-1.4} = 1.0 \text{ KHz/V} \quad (31)$$

$$\text{At 2V, } K_{vco5} = \frac{378.2-377.7}{2.2-1.8} = 1.25 \text{ KHz/V} \quad (32)$$

From equation 28 to 32 a tuning sensitivity table can be drawn and a graph plotted as shown in figure 25 below.

Table 4 Tuning sensitivity data

Control Voltage(V)	Kvco(KHzV)
0	1
0.5	1.33
1	0.75
1.5	1
2	1.25

The above results are plotted on the graph below.

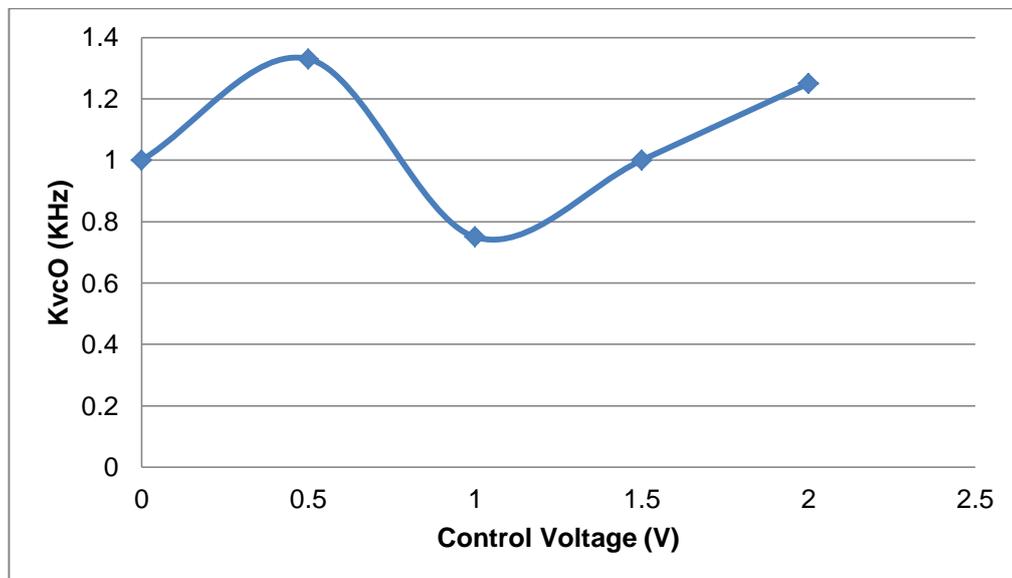


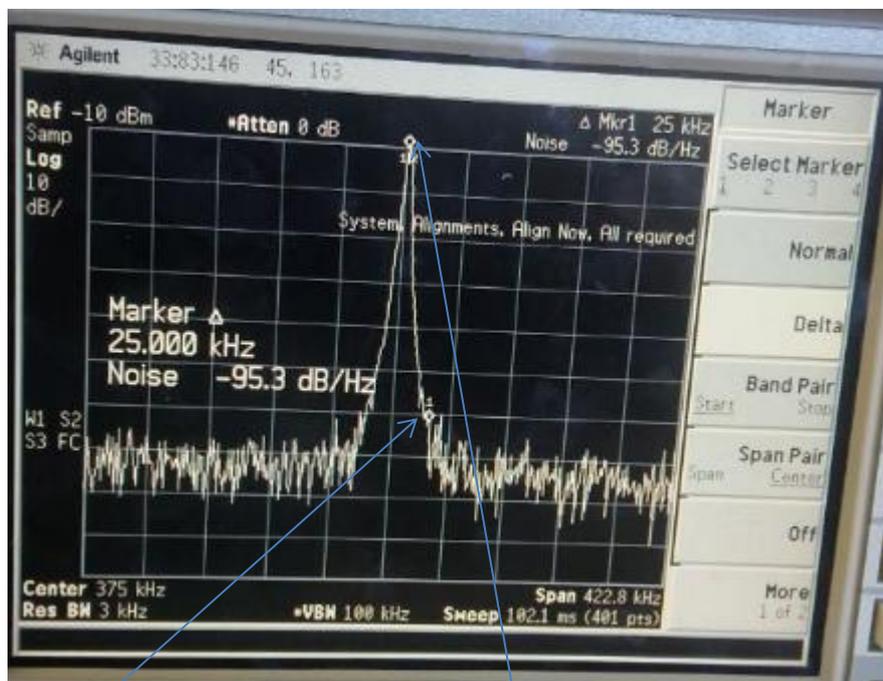
Figure 25 VCO Tuning Sensitivity curve.

The relationship of this curve can be seen in the curve, as it rise and falls and rise again, which is almost the same as that of the simulation, this is consider more accurate, because the dip in it demonstrates there are some spurious signals in the system.

5.3.3 VCO Phase Noise Measurement

One of the easiest methods to measure phase noise is by the use of a Spectrum Analyser. Since phase noise is of great importance for many systems, it is important to measure it with care and accuracy. Figure 13 in section 3.8 above demonstrate at what level phase noise and broadband phase noise are measured.

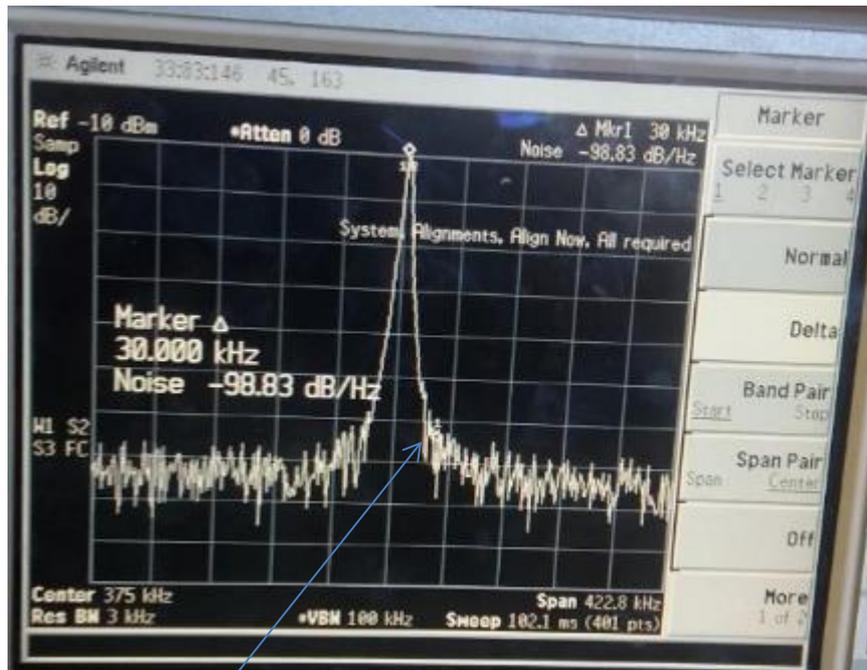
The short-term stability of this VCO was examined with a spectrum analyzer, and data were captured from a frequency offset of 0Hz to 25 KHz, and the broadband phase noise started at 30 KHz. Figure 26 and 27 below illustrates the phase noise at 25 KHz offset and broadband noise at 30 KHz offset respectively.



Phase Noise level in dB/Hz

Figure 26 Phase Noise at 25 KHz Frequency Offset displaying a value of -95.3dB/Hz

The arrows shows the levels at which the phase noise is measured. I can be seen that at the frequency offset of 25 KHz the noise is -95.3 dB/Hz.



Broadband Phase Noise

Figure 27 Broadband Phase Noise at 30 KHz Frequency Offset with -98.83dB/Hz

Figure 27 above shows the broadband phase noise of -98.83 dB/Hz at a frequency offset of 30 KHz. The arrows on the diagram indicates the level at which the broadband phase noise begins.

Table 5 below shows the results of the VCO Phase Noise measurement, details of this captured data can be seen in appendix 2B below.

Table 5 Phase Noise in dB/Hz versus Frequency Offset in KHz

Frequency Offset (KHz)	Phase Noise (dB/Hz)
0	-53.86
5	-55.49
10	-66.87
15	-78.46
20	-89.07
25	-95.3

These measured values are plotted on the graph below.

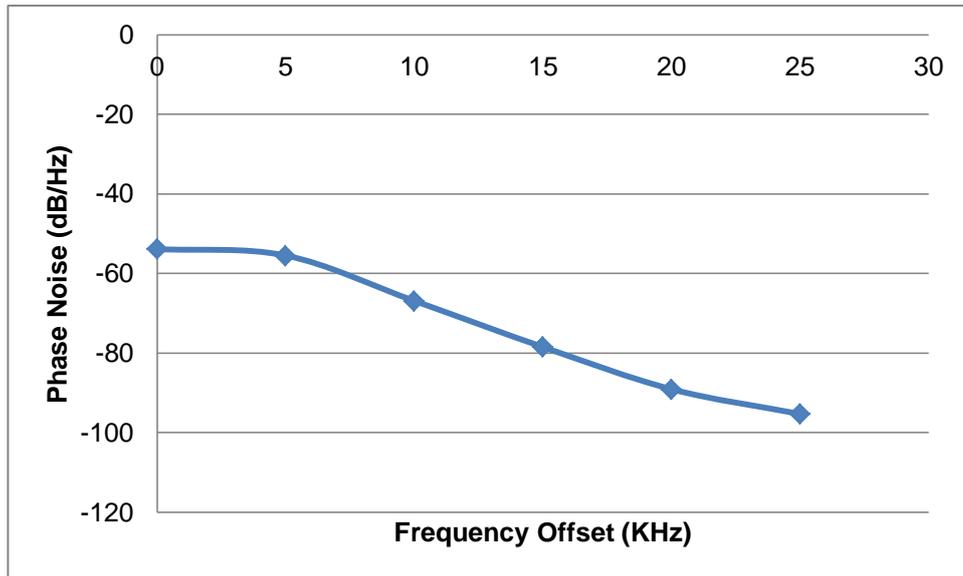


Figure 28 Phase Noise in dB/Hz versus Frequency Offset in KHz

The above graph show the relationship between the phase noise and the frequency offset.

6 Conclusions and Discussions

6.1 Conclusions

This thesis was to design a voltage controlled oscillator that can be use in a Phase Locked Loop system, this design was to be analyse with real components and milled on a printed circuit board as shown in appendix 2C. PLL system was discussed and some characteristics of it were also analysed.

The design of the oscillation was done with NI Multisim Software and the results were compared with that of real components, which was successful. Results were taken from both an Oscilloscope and a Spectrum Analyzer. Graphs of the tuning gain and tuning sensitivity of the oscillator were plotted and were similar to those in the theory. The design was made on a printed circuit board but a reliable result could not be attained.

One of the key aspects of the design which is the phase noise was analysed using a Spectrum Analyzer and the result was similar to the one in the theory. Also the rela-

tionship between the phase noise and the frequency offset was analysed and a graph plotted.

Hence, the goal of the Thesis which was to design a VCO, compared the simulated result with that of a real components, measure the Phase noise, tuning gain, tuning sensitivity and making a prototype was partially attained, since a reliable result could not be attain from the PCB prototype.

6.2 Discussions

The goal of this thesis was partially attained due to some drawbacks. First, because the calculation was done and simulated using BB112 Varactor diode which was the key component in the design and the oscillator was oscillating at 4.86MHz as can be seen in appendix 2D. This was not achieved on real components because the BB112 Varactor was not found in most of the close shops around the country, and could only be ordered abroad and due to the time for the completion of the thesis, it was not possible, so a new calculation was done for the BB909A varactor diode which could be found in the shop.

Also, some other difficulties were encountered that took more time to complete the work in other to catch up with time, this leads to minimal attempts to make the prototype work properly after several boards were milled and tested.

The discrepancy in the above results may be due to the noise contributed from the power sources in the laboratory, also to ensure good results care must be taken when making the measurements, since these results were taken by snapshots which is not very accurate.

Another point to note is the unit of the phase noise. Normally phase noise unit is dBc/Hz, but for some reason the spectrum analyzer used displays it as dB/Hz.

The measurement of this design may be improved by using other measurement techniques instead of the direct measurement carried out with snapshots. Also the prototype of the design could be achieved.

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<http://www.analog.com/media/en/training-seminars/tutorials/MT-086.pdf>. Accessed 21 March 2016

(A) VCO Simulation Results

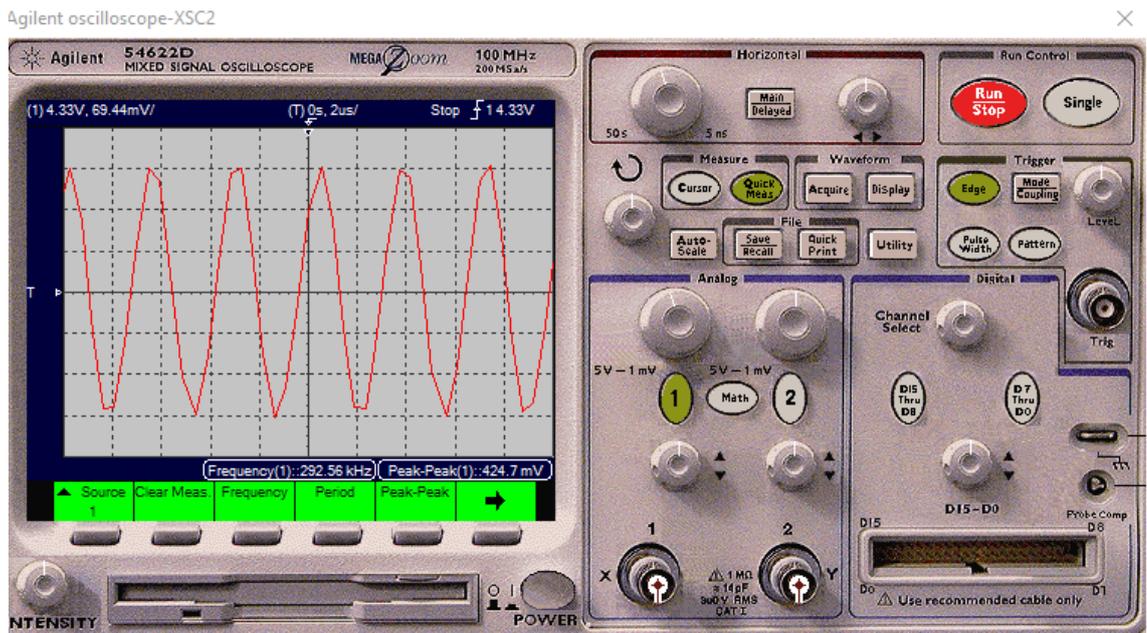


Figure 29 Simulation result on Agilent Oscilloscope at 0V

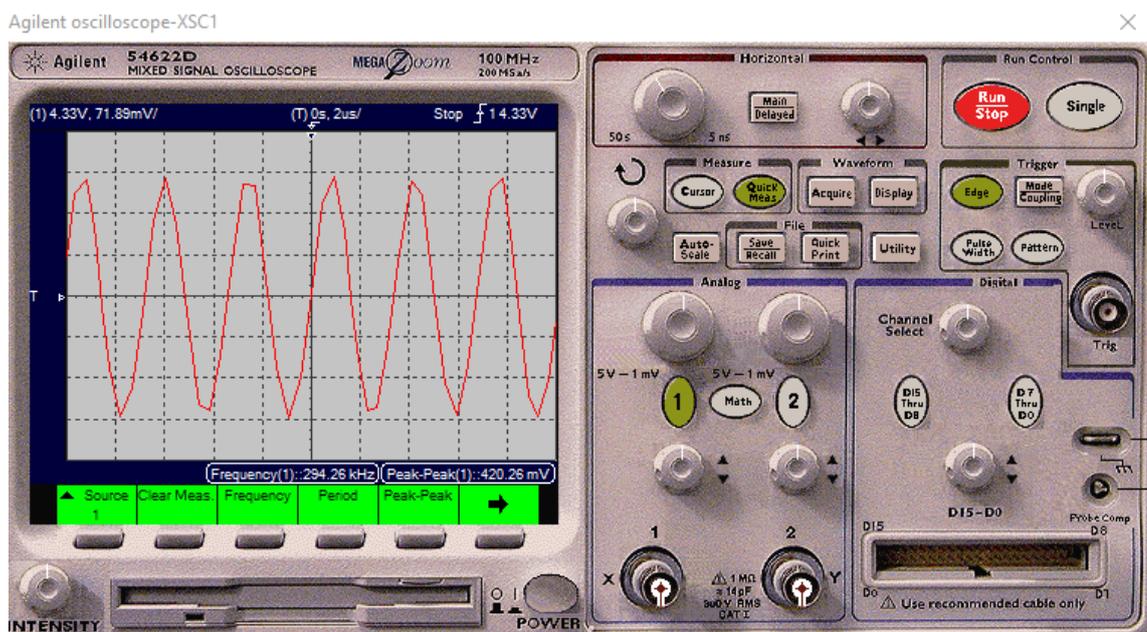


Figure 30 Simulation result on Agilent Oscilloscope at 0.5V

Agilent oscilloscope-XSC1

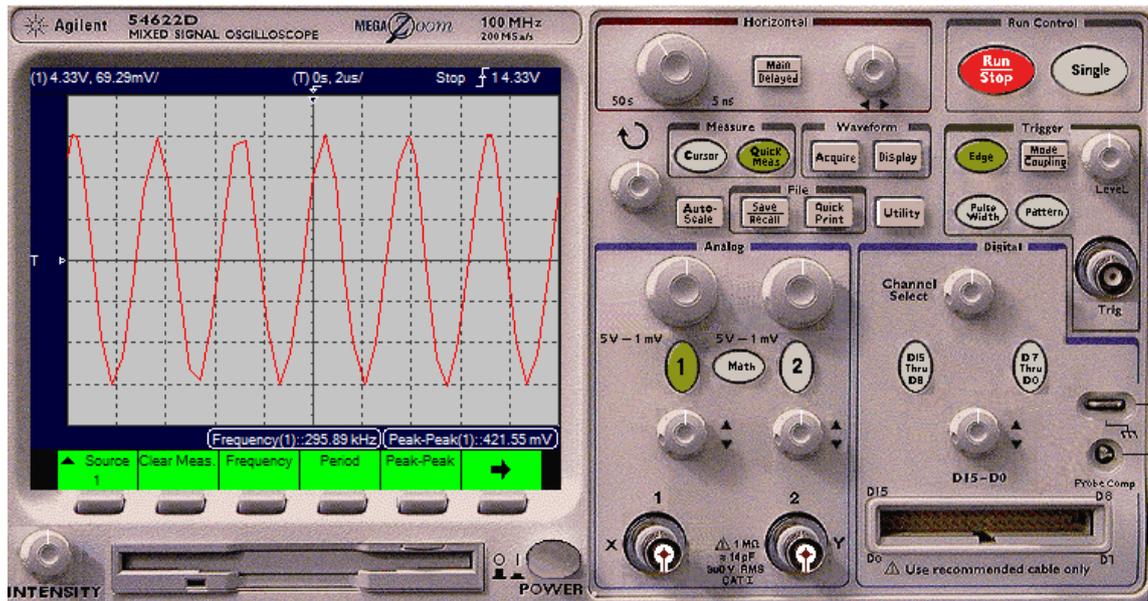


Figure 31 Simulation result on Agilent Oscilloscope at 1V

Agilent oscilloscope-XSC1

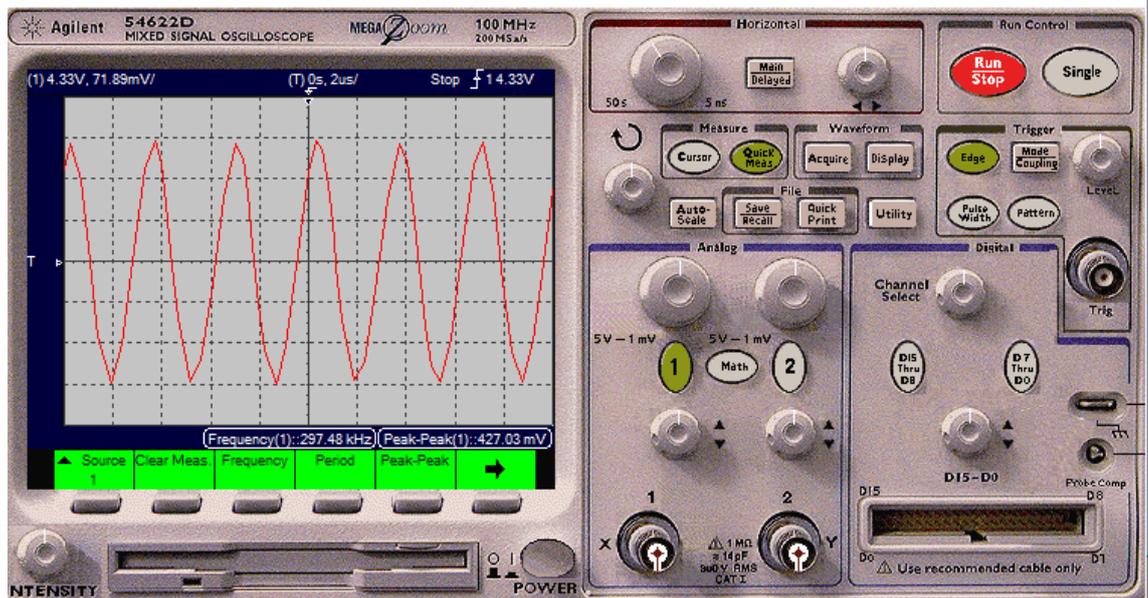


Figure 32 Simulation result on Agilent Oscilloscope at 1.5V

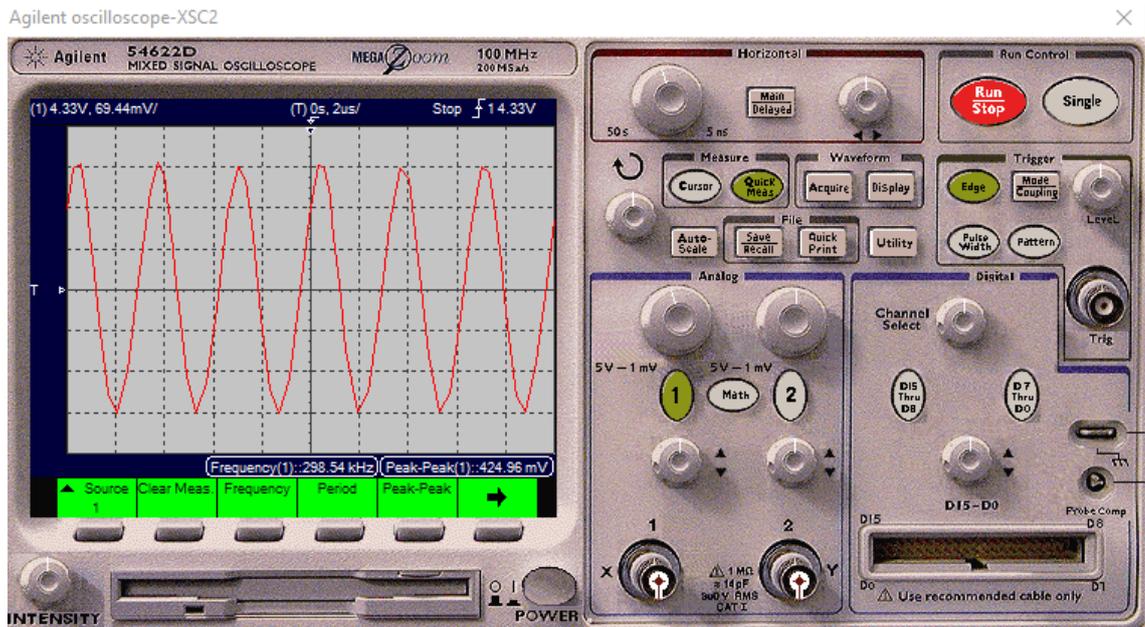


Figure 33 Simulation result on Agilent Oscilloscope at 2V

(B) Real Component Results (Oscilloscope Waveforms)



Figure 34 Oscilloscope Measurement Waveform after placing the Buffer at 0V



Figure 35 Oscilloscope Measurement Waveform after placing the Buffer at 0.5V

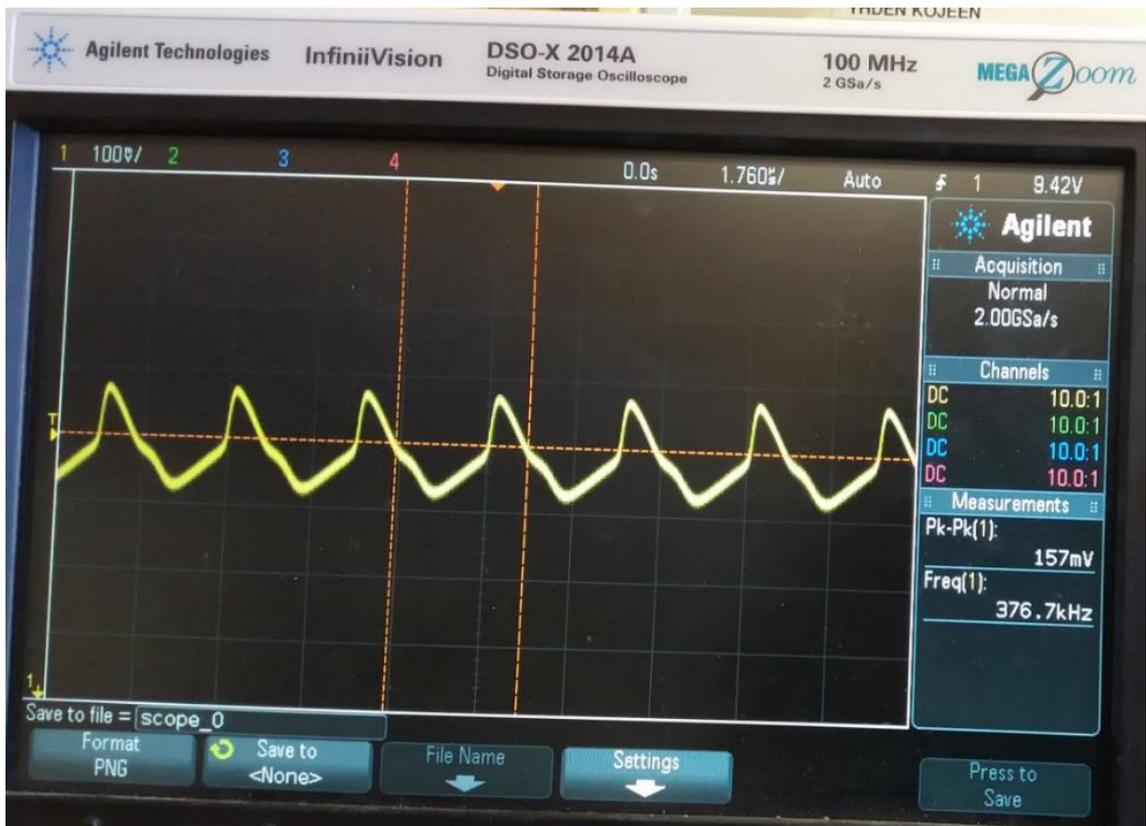


Figure 36 Oscilloscope Measurement Waveform after placing the Buffer at 1V



Figure 37 Oscilloscope Measurement Waveform after placing the Buffer at 1.5V

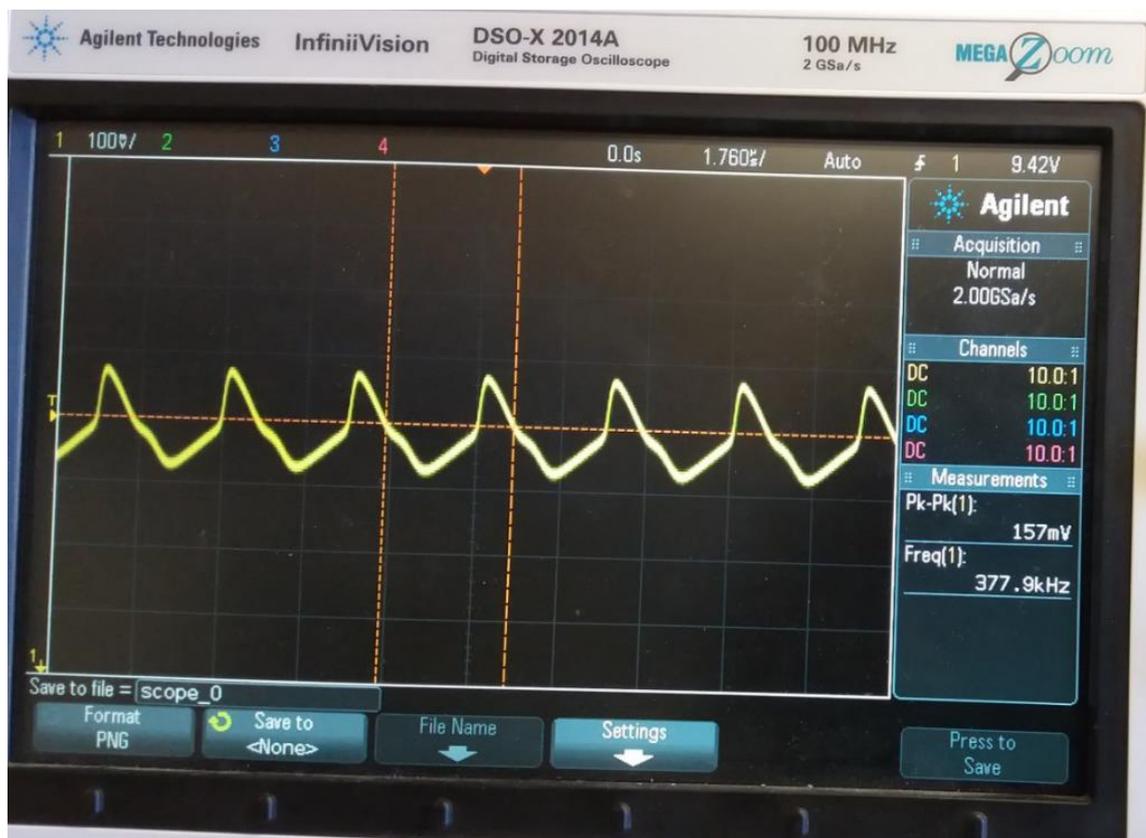


Figure 38 Oscilloscope Measurement Waveform after placing the Buffer at 2V

(A) Real Component Signal Display by Spectrum Analyzer

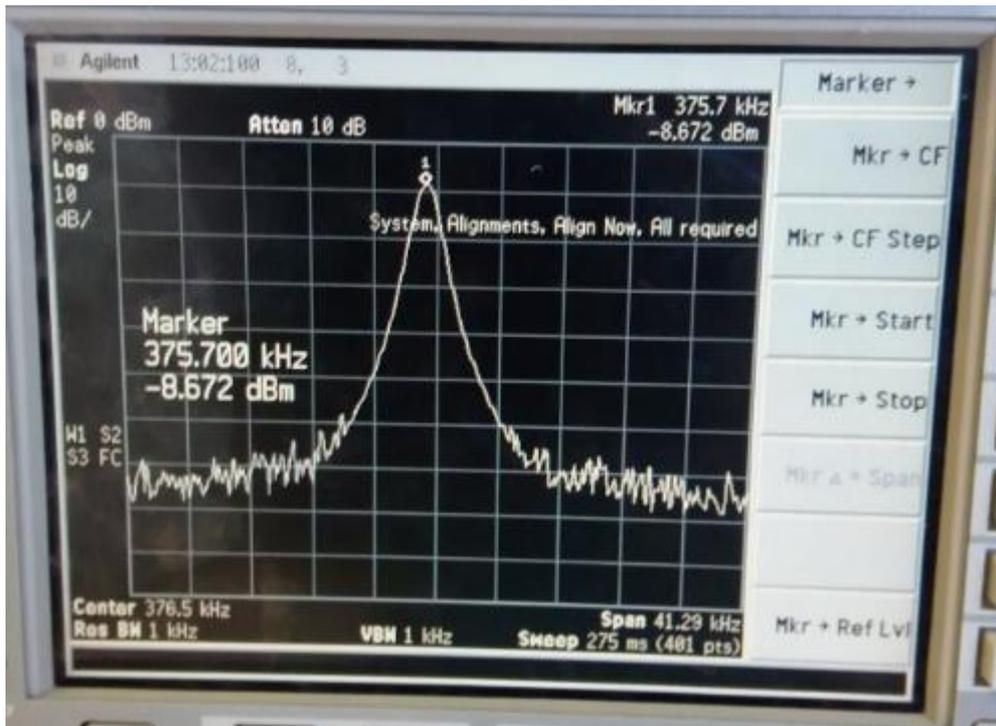


Figure 39 Spectrum Analyzer Signal Display at 0V

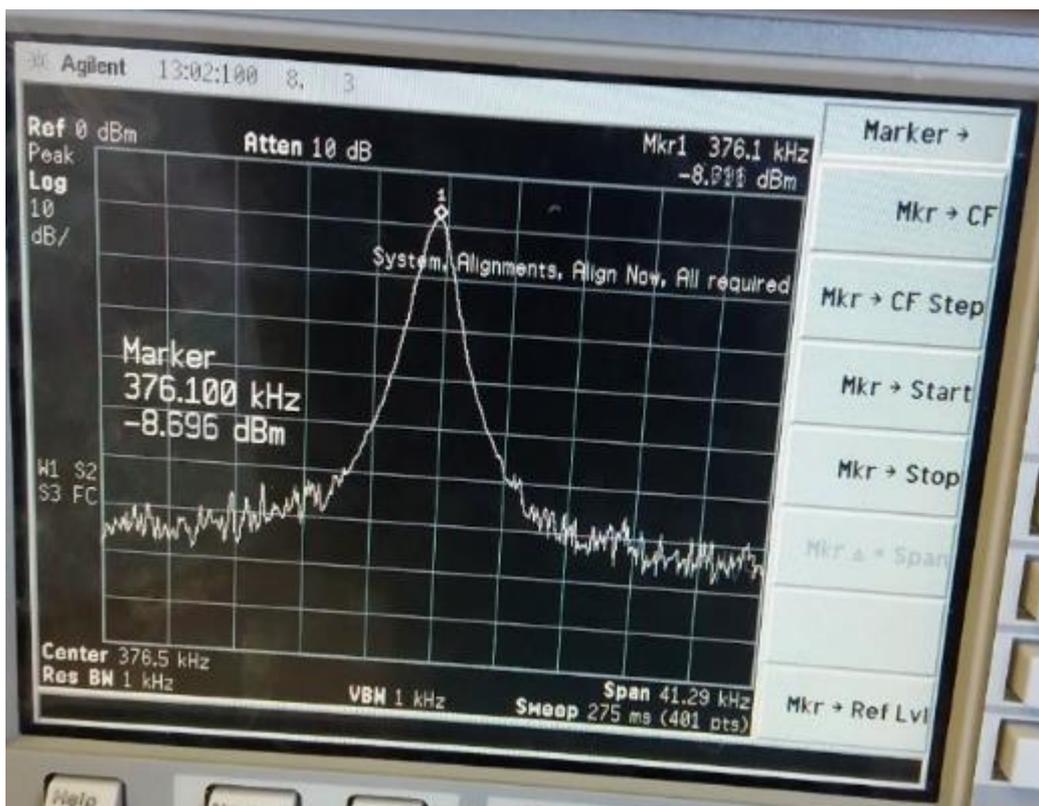


Figure 40 Spectrum Analyzer Signal Display at 0.5V

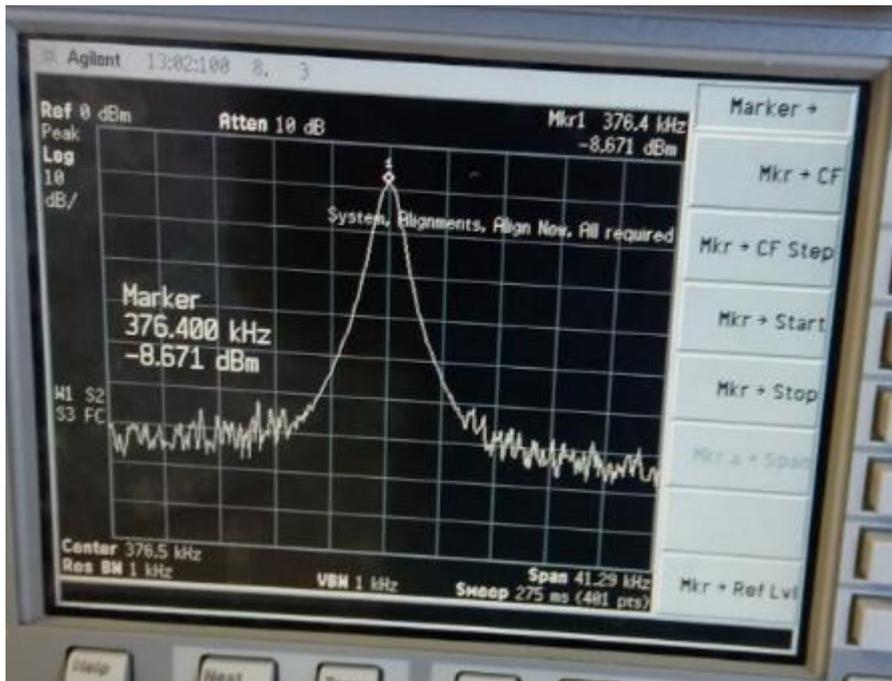


Figure 41 Spectrum Analyzer Signal Display at 1V

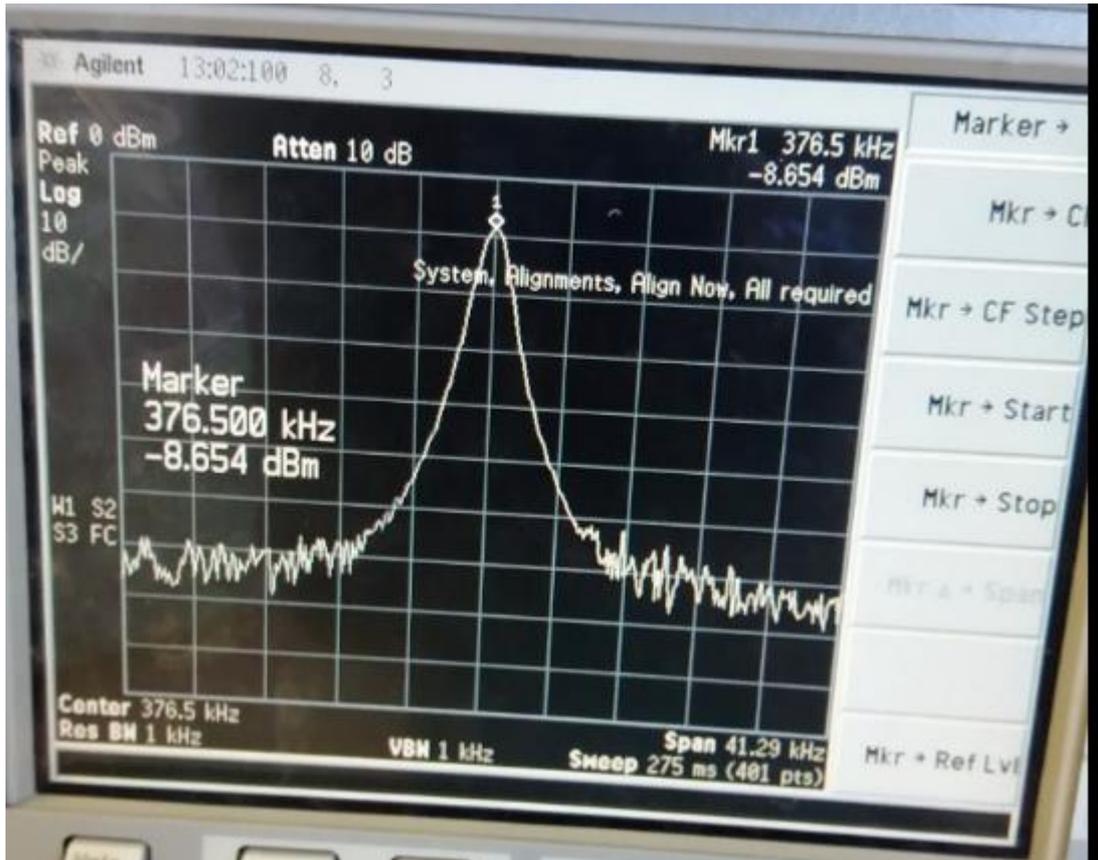


Figure 42 Spectrum Analyzer Signal Display at 1.5V

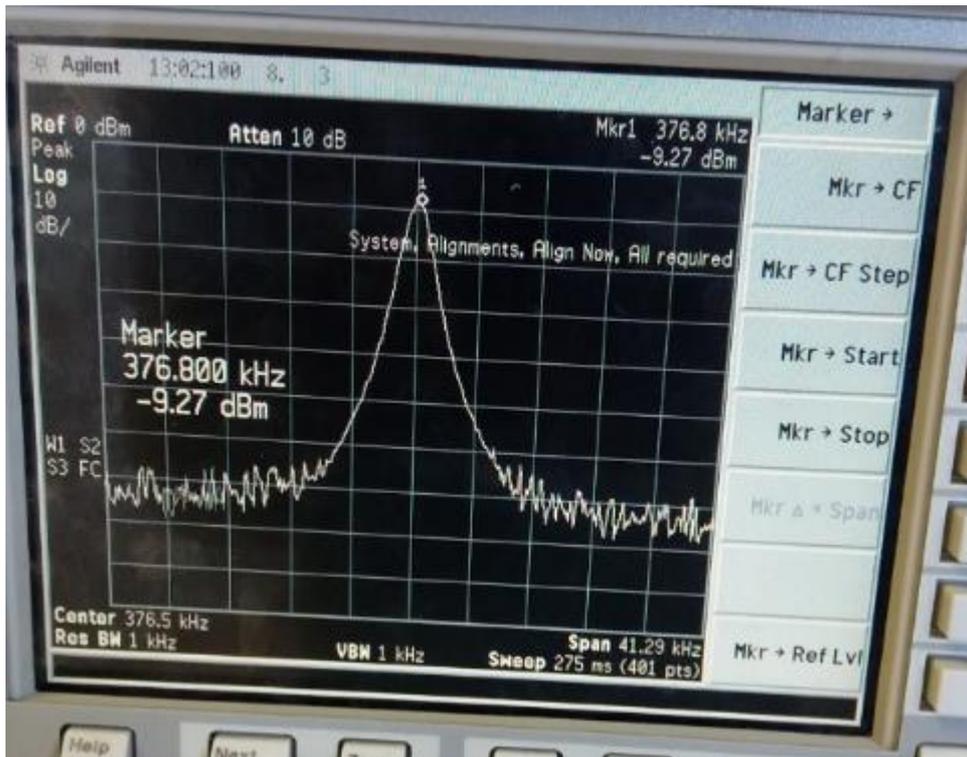


Figure 43 Spectrum Analyzer Signal Display at 2V

(B) Phase Noise Measurement Signals

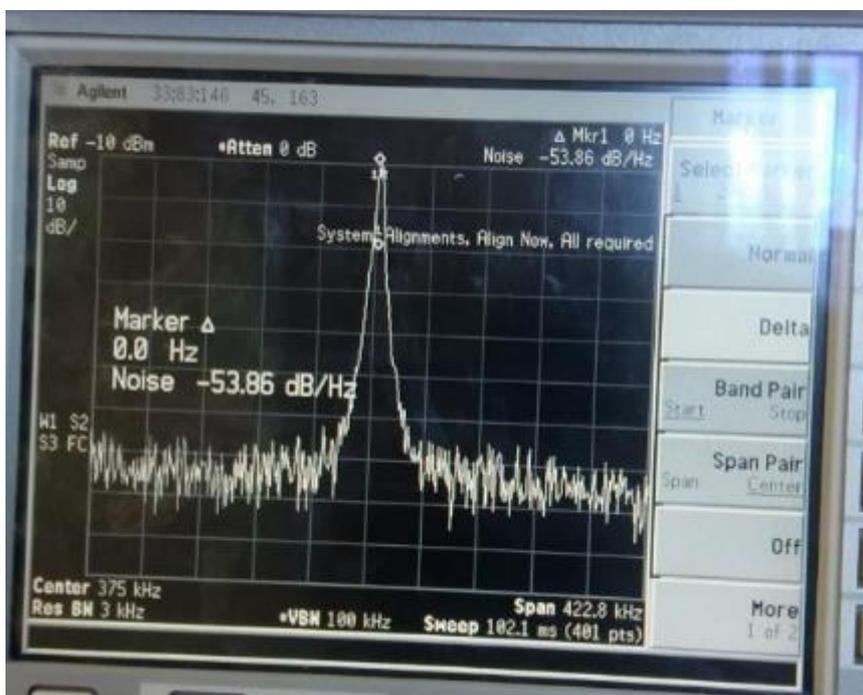


Figure 44 Phase Noise at 0 Hz Frequency Offset displaying a value of -53.86 dB/Hz

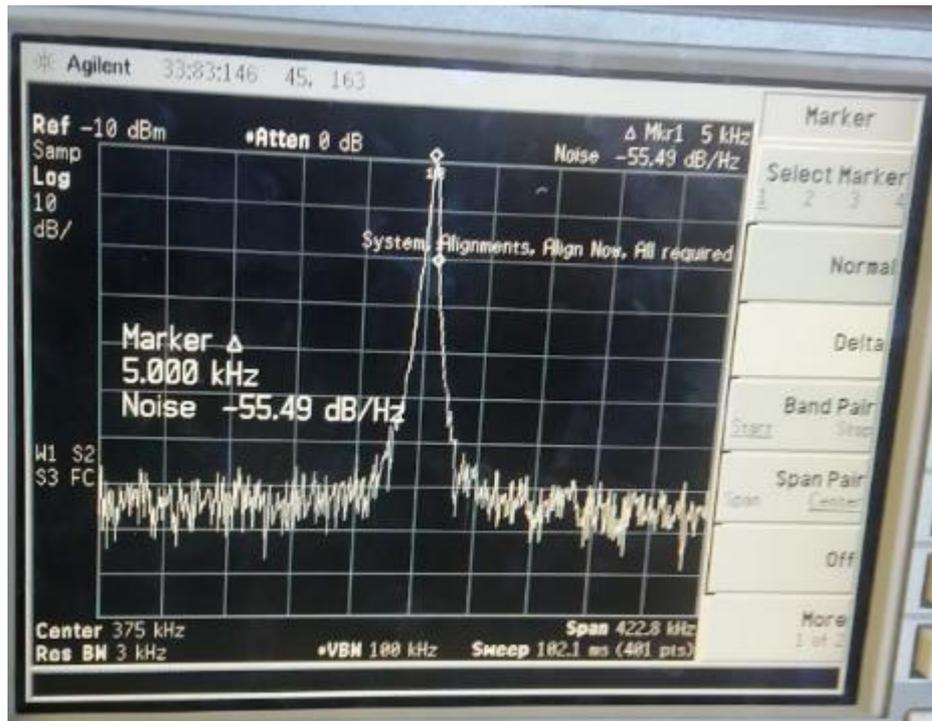


Figure 45 Phase Noise at 5 KHz Frequency Offset displaying a value of -55.49 dB/Hz

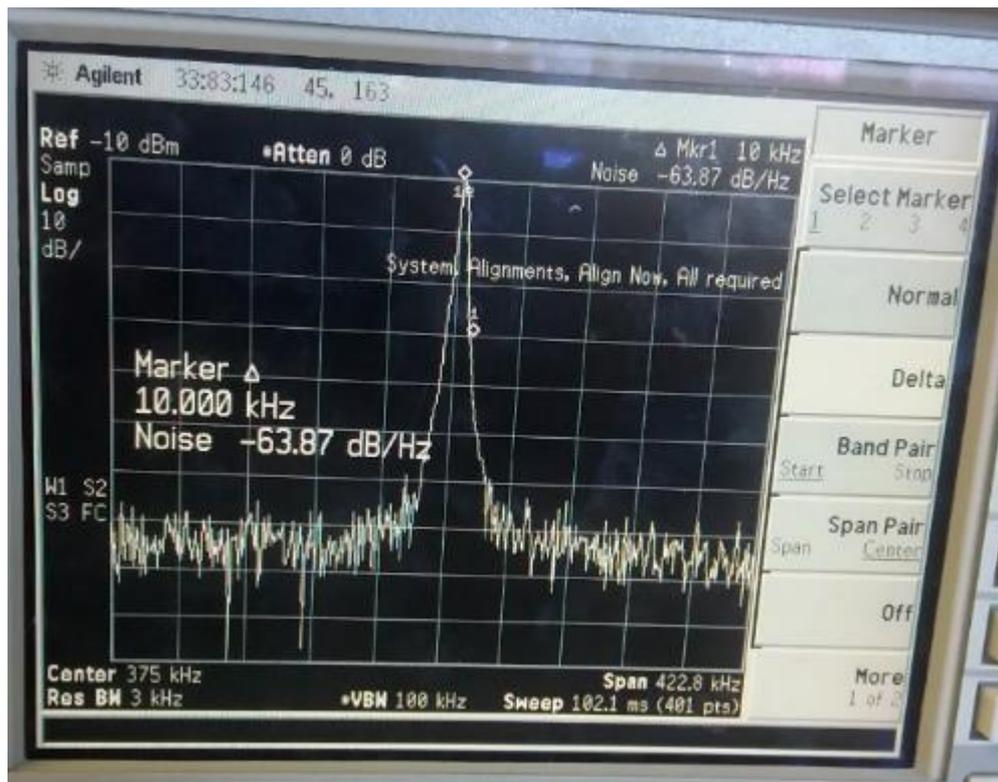


Figure 46 Phase Noise at 10 KHz Frequency Offset displaying a value of -63.87 dB/Hz

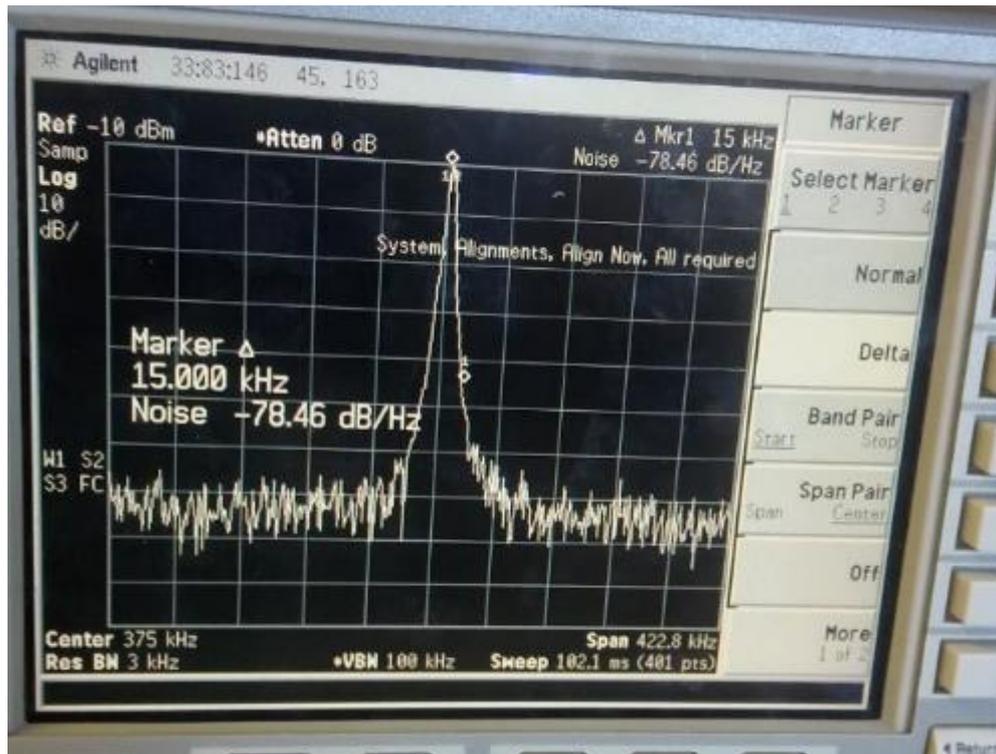


Figure 47 Phase Noise at 15 KHz Frequency Offset displaying a value of -78.46 dB/Hz

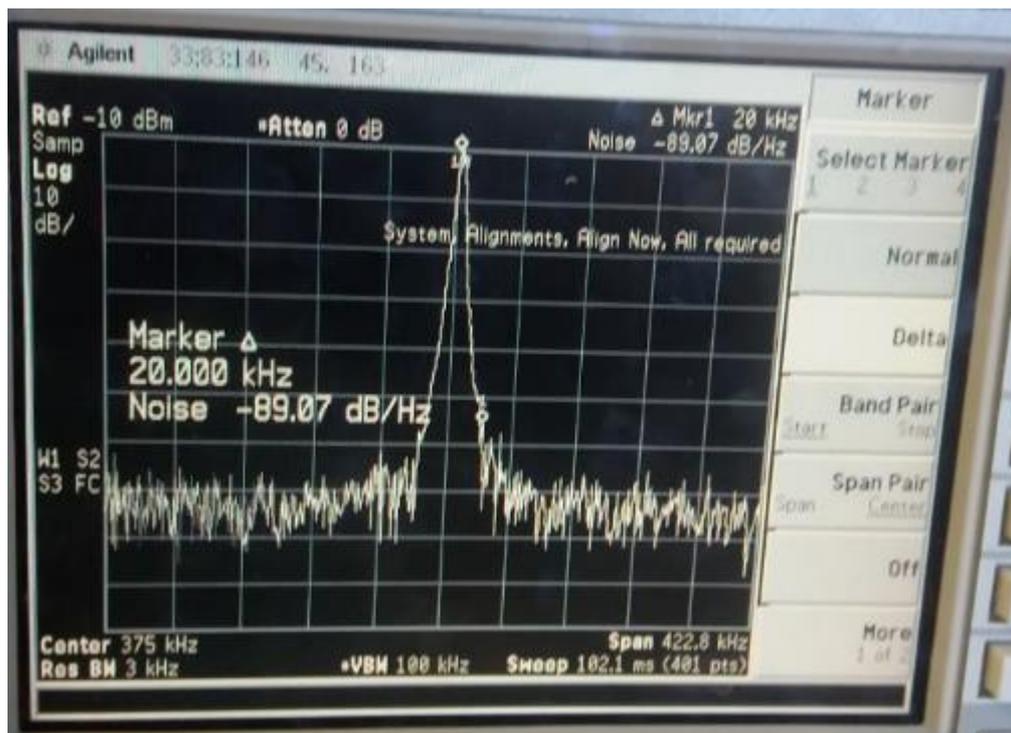


Figure 48 Phase Noise at 20 KHz Frequency Offset displaying a value of -89.07 dB/Hz

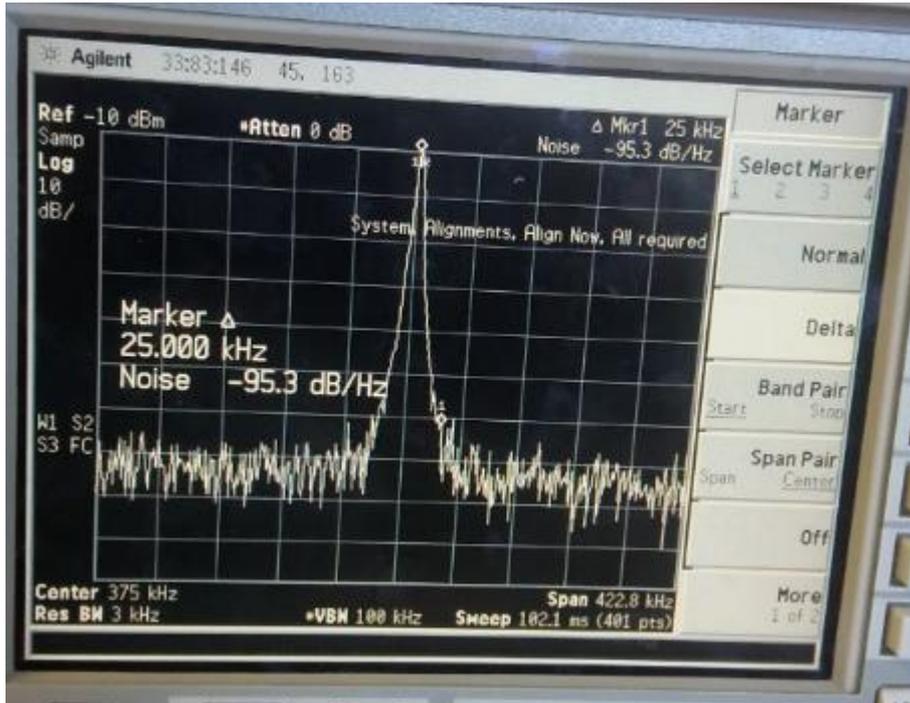


Figure 49 Phase Noise at 25 KHz Frequency Offset displaying a value of -95.3 dB/Hz

(C) Printed Circuit Board Designs

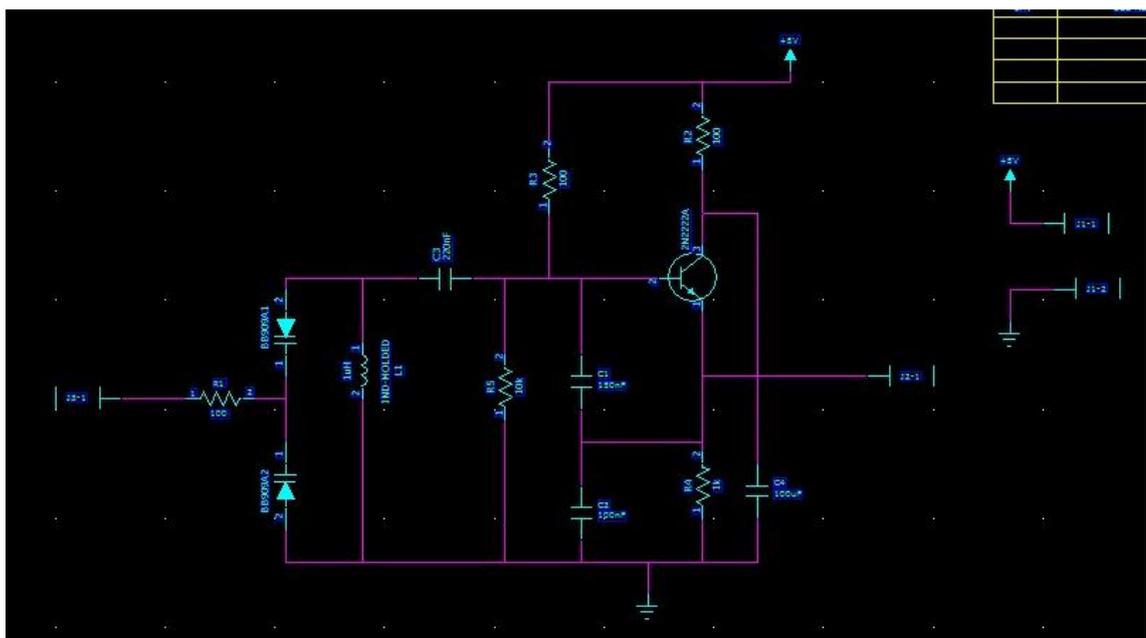


Figure 50 PCB Logic Diagram

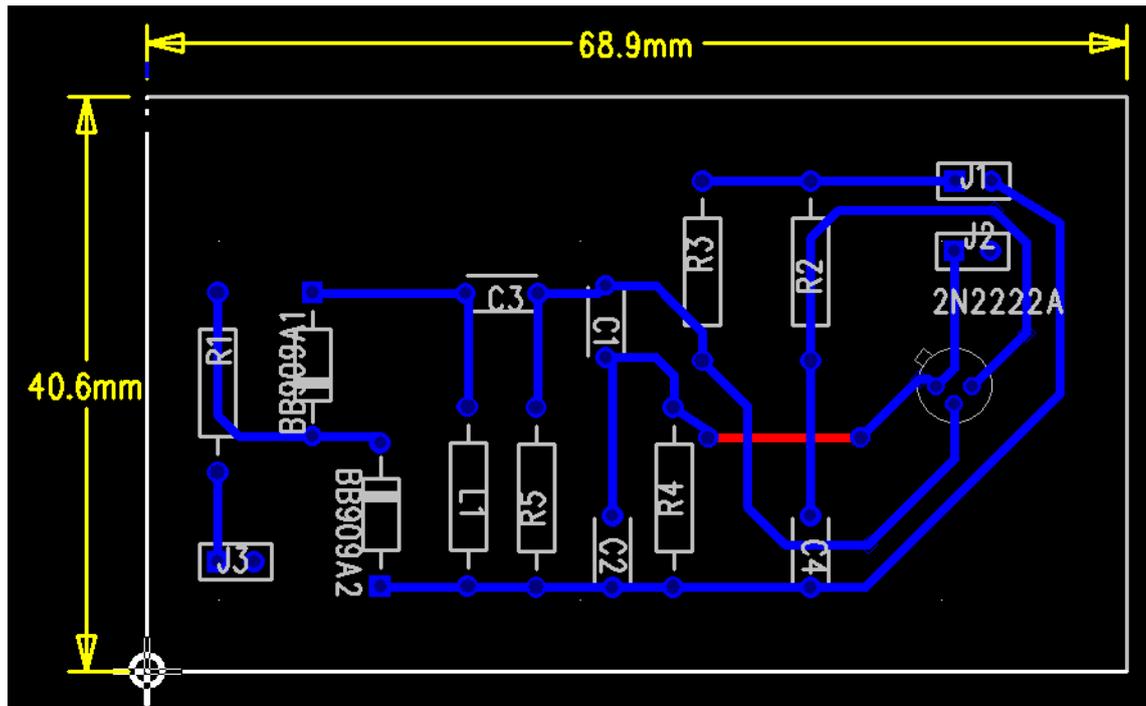


Figure 51 PCB Layout with dimensions



Figure 52 Milled Circuit board top side with soldered components

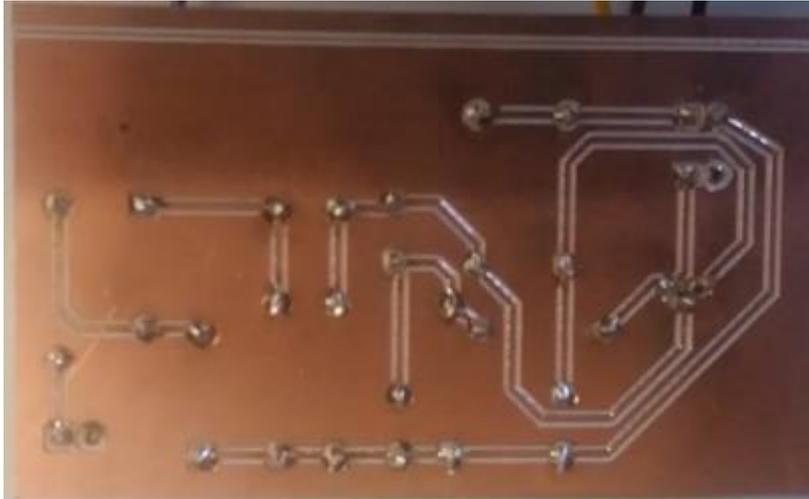


Figure 53 Milled Board Bottom side with solders.

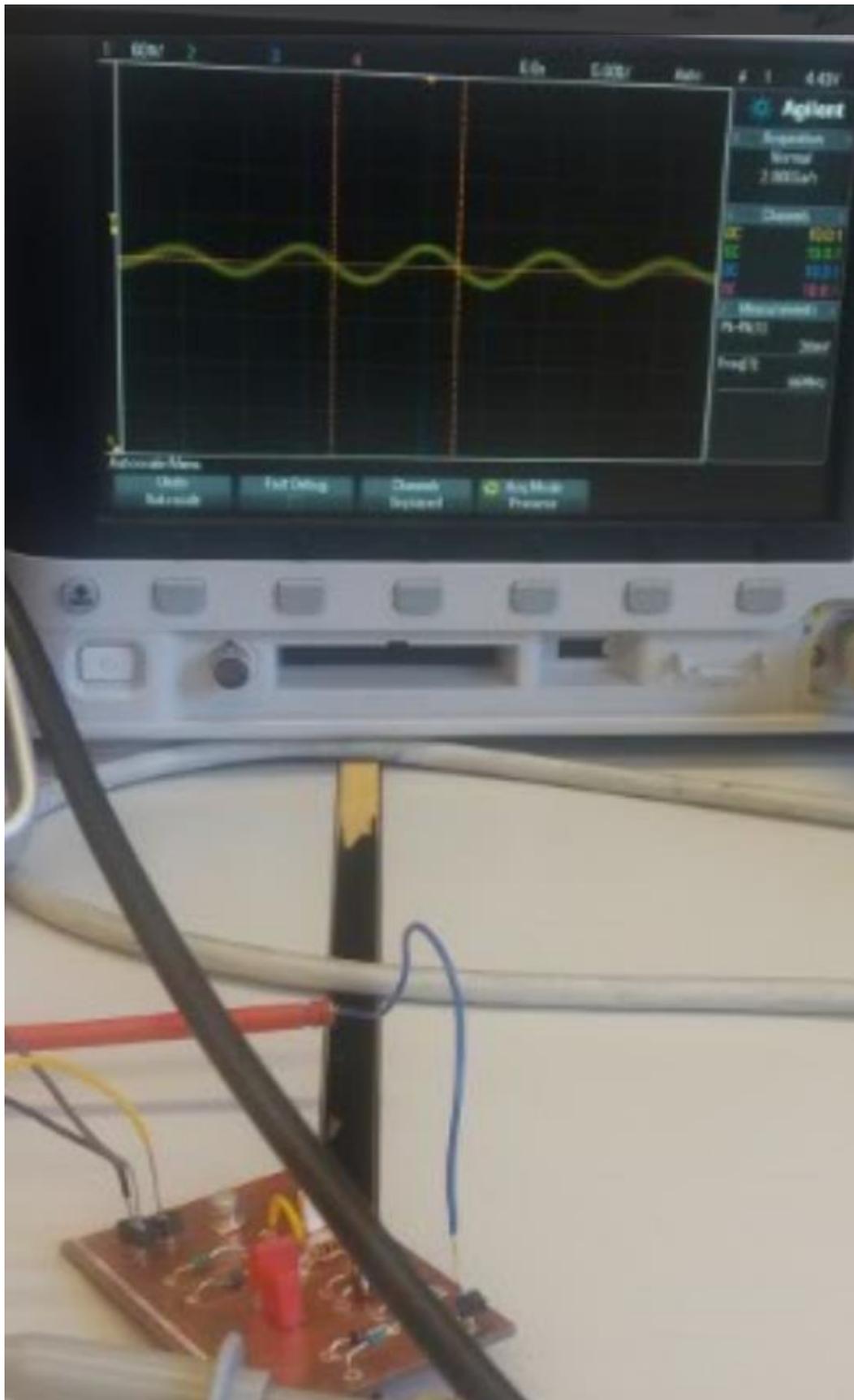


Figure 54 PCB measurement

D Simulation Result with BB112 Varactor Diode

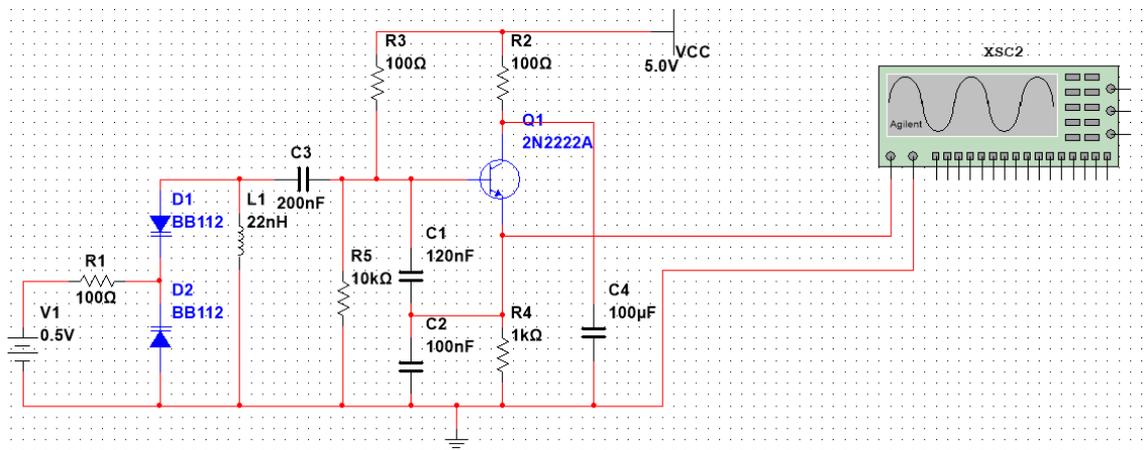


Figure 55 Simulation Setup

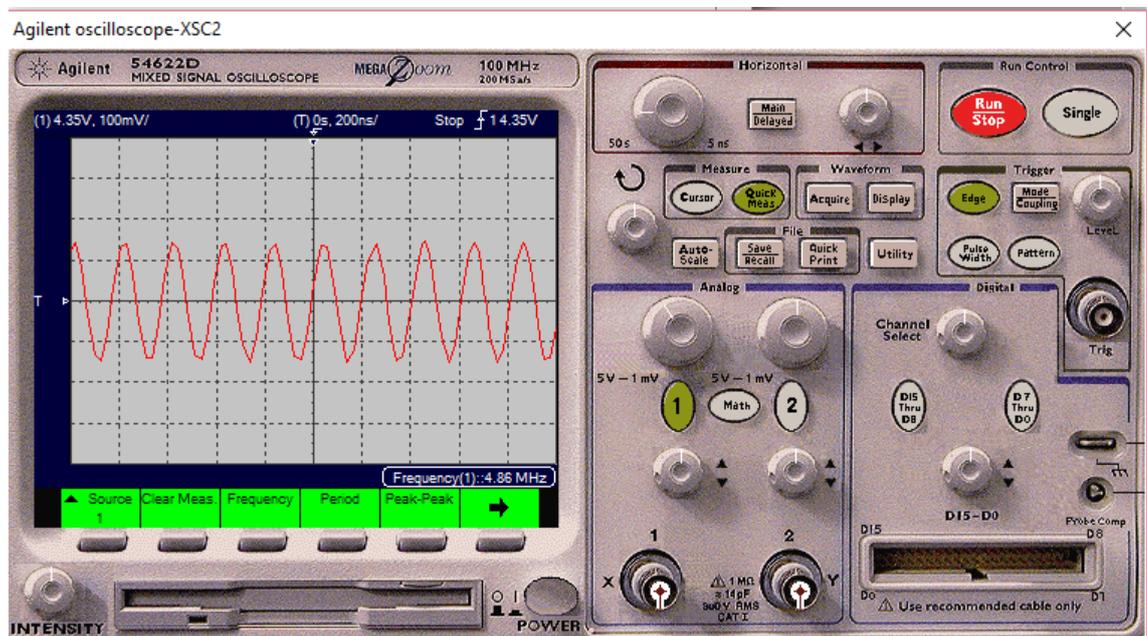


Figure 56 Simulation result at 0.5V