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The Impact Of Loop Filter In Phase Locked Loop

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Phase Lock Loop is one of the most essential techniques today and it is used for many different purposes. Typical cases are frequency synthesizer, radio receiver, clock recovery and FM demodulation. Especially as a frequency synthesizer, PLL is a core component in wireless communication devices. One of the most important components of the PLL is loop filter since it gives a decisive impact to the whole system operation. This thesis is focused on specifying the effect of loop filter by designing two different analog loop filters and comparing their outputs.

There are a lot of different loop filters that can be used for various PLL systems. Two representative loop filter models were selected, and they were designed to make proper operation with other components. Among many various types of PLL, this thesis covers the analog PLL, therefore loop filters were implemented on the printed circuit board with analog components. Pole and zero points were tried to be designed to be equal so that the other factors can be measured. Other analog components that construct PLL are from MiniCircuit. Hold-in, Pull-in range and phase noise were measured with spectrum analyzer. Especially, the method of hold-in range calculation is introduced and calculated and measured results are compared.

With suitable connections of components, whole PLL systems were implemented. The importance of loop filter is specified with the results although it presented considerable discrepancy between expected and practical results. Further studies might be improved by adding frequency divider on the feedback loop and measuring transient response that depends on the transfer function of the system. Designing loop filters with different pole and zero points would give some different results in the aspect of phase noise.

Keywords	PLL, Loop filter, Frequency Synthesizer, Phase Noise

Contents

List of Abbreviations

PLL	Phase Locked Loop
IC	Integrated Circuit
VCO	Voltage Controlled Oscillator
LO	Local Oscillator
PFD	Phase Frequency Detector
CP	Charge Pump
RF	Radio Frequency
XOR	Exclusive OR
APLL	Analog Phase Locked Loop
LPLL	Linear Phase Locked Loop
DPLL	Digital Phase Locked Loop
ADPLL	All Digital Phase Locked Loop
PCB	Printed Circuit Board
DC	Direct Current
Nano (n)	10^{-9}
Farad (F)	Unit of Capacitor
LBW	Loop Bandwidth

1 Introduction

Phase Locked Loop is one of the most important techniques frequently used in communication applications. It can be utilized in frequency synthesizers, clock recovery radio transceiver and FM modulation. Because of the recent advances in integrated chip (IC) design techniques, it became more reliable and economical and its usefulness increased rapidly. Currently the whole PLL circuit is integrated in a single chip and it can be easily applied and integrated to other bigger circuits.

A typical PLL consist of variable frequency oscillator and a phase detector. The oscillator generates a periodic signal and phase detector compares the signals to match the phase of the input signal and oscillator signal. Oscillator can track the input signal frequency and it can generate multiple frequencies of input signal by adding N divider in the feedback loop.

Among a lot of components that are used in PLL, loop filter is the most vital component since it determines most of the output dynamics. By determining the bandwidth, type and order of the loop filter, system designer can control a trade-off between noise and frequency acquisition. There are many different types of loop filters that can be used. However, they all should meet the requirements of the system they will be used in. The aim of this thesis is to specify the importance of the loop filter in PLL system.

2 Theoretical Background of PLL

2.1 PLL Basics

PLL has voltage-controlled oscillator and phase detector with negative feedback so that the oscillator holds the constant phase compared to the reference signal [1]. Phase detector compares the phases of reference signal and feedback signal. Proportional to phase difference of two signals, phase detector results in current pulses. In loop filter they are filtered and integrated as a voltage, and that voltage controls output frequency

of VCO. Output signal of VCO is fed back to the phase detector so that it can compare two signals again. Figure 1 shows a general PLL block diagram. [2]

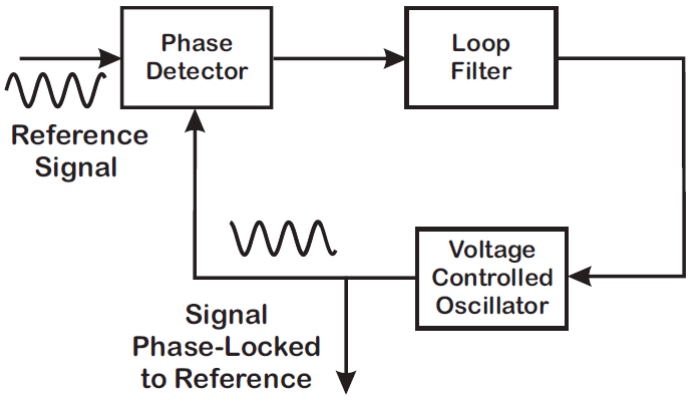

Figure 1. A general PLL block diagram (Copied from Abramovitch [3])

If a loop filter and VCO are analog elements and the linear element is used as a phase detector, this is analog PLL or linear PLL (APLL or LPLL). If a loop filter and VCO are still analog elements but digital phase detector (for example, XOR gate or J-K FF) is used, it is digital PLL (DPLL). If all the elements are not linear but digital, this system is all-digital PLL (ADPLL). [1]

2.2 Linear Analysis of PLL

2.2.1 Constant Error Signal and Locked State

In the figure 2, when the VCO output frequency is f_o and N divider is used in the feedback path, the signal is divided by N and fed back to the phase detector. Phase detector compares reference signal and the feedback signal. When the two signal inputs have same frequency, the output of phase detector will be constant, which means that loop is “locked”.

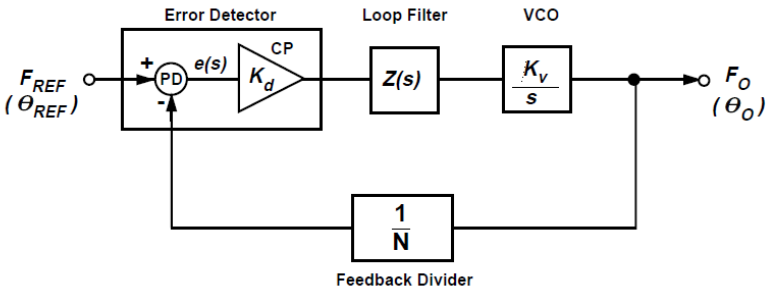

Figure 2. Basic PLL model (Copied from Analog Devices [4])

Error signal is proportional to the phase difference of the two input signals of phase detector. Relationship between error signal and phase difference can be described as the equation 1.

$$e(s) = \theta_{REF} - \frac{\theta_O}{N} \tag{1}$$

Since the differential form of phase is frequency, equation 1 can be described again as equation 2.

$$\frac{de(s)}{dt} = F_{REF} - \frac{F_O}{N} \tag{2}$$

When the error signal is constant, left side of the equation 2 is zero, therefore the relationship between reference frequency and output frequency can be described as equation 3.

$$\frac{F_O}{N} = F_{REF} \tag{3}$$

Therefore, if there is a frequency divider at the feedback loop, output frequency is N times of reference frequency when the phase difference of two signals is constant. [1]

$$F_O = N * F_{REF} \tag{4}$$

PLL is usually used as a frequency synthesizer since it can generate high frequency with high stability of reference frequency. Crystal oscillator is usually used since it is super reliable and stable frequency source, although the generated frequency is normally low.

2.2.2 Negative Feedback Model Analyzation

PLL can be analyzed with a negative feedback system model. Assume the model has forward gain G(s) and feedback gain H(s). Figure 3 is simple block diagram of negative feedback system.

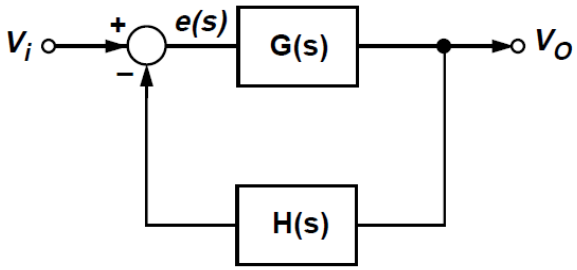

Figure 3. Standard negative-feedback control system model (Copied from Mike Curtin and O'Brien [1])

As mentioned above, output signal of phase detector, which can be called as an error signal, is proportional to the phase difference of the reference signal and feedback signal. Error signal will be constant when two signals are on the same frequency. Equations 5,6 and 7 will be used for later analysis. [1]

$$Forward\ Gain = G(s), [s = j\omega = j2\pi f] \tag{5}$$

$$Loop\ Gain = G(s) \times H(s) \tag{6}$$

$$Closed\ Loop\ Gain = \frac{G(s)}{1 + G(s)H(s)} \tag{7}$$

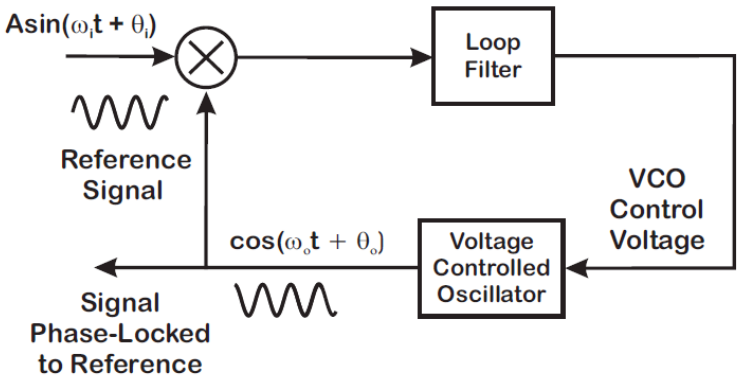

Figure 4. A classic mixing phase-locked loop (copied from Abramovich [3])

Since analog PLL is the main topic in this study, linear analysis of APLL will be studied in this part. As shown in figure 4, a sinusoidal signal at the reference input of APLL can be written as below.

$$\upsilon_i = R_1(t) = Asin(\omega_i t + \theta_i) \tag{8}$$

Then the output signal from the VCO into the mixer can be described as below.

$$v_o = VCO_{out}(t) = \cos(\omega_o t + \theta_o) \tag{9}$$

The output signal of the mixer in figure 4 is presented as following.

$$v_d = Mixer_{out}(t) = AK_m \sin(\omega_i t + \theta_i) cos(\omega_o t + \theta_o) \tag{10}$$

K_m is the gain of the mixer.

Analysis of PLL can be easily done with many simplifying steps. One of them is using the trigonometric equation in terms of PLL:

$$2\sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) = \sin\big((\omega_i + \omega_o)t + \theta_i + \theta_o\big) + \sin\big((\omega_i - \omega_o)t + \theta_i - \theta_o\big) \tag{11}$$

Let $\theta_d = \theta_i - \theta_o$. Assume that high frequency term of the equation 11 is attenuated by the low pass filter and frequencies of output and input signal are same($\omega_i \approx \omega_o$) so that the difference can be incorporated into θ_d.

To avoid nonlinear analysis, one more approximation method can be used. For small and slow varying θ_d,

$$\sin\theta_d \approx \theta_d, \cos\theta_d \approx 1, and\ {\theta_d}^2 \approx 0 \tag{12}$$

This is useful for analyzing the locked loop but is not helpful for analyzing the loop that has large θ_d.

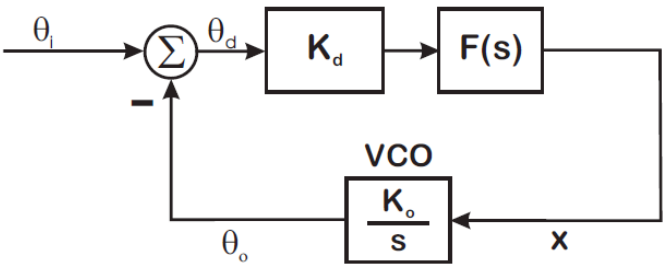

Figure 5. PLL block diagram with simplifying steps (Copied from Abramovitch [4])

Simplified block diagram is provided in Figure 5. Most of the analyses are done in this way. [4]

For the model in Figure 5 with closed loop negative feedback system, transfer function from reference phase input to VCO phase output, T(s), can be obtained as

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{K_d F(s) K_o}{s}}{1 + \frac{K_d F(s) K_o}{s}} = \frac{K_d K_o F(s)}{s + K_d K_o F(s)} \tag{13}$$

In the same way, transfer function from the reference phase input to the phase error, $S(s)$, can be obtained as

$$S(s) = \frac{\theta_d(s)}{\theta_i(s)} = \frac{1}{1 + \frac{K_d F(s) K_o}{s}} = \frac{s}{s + K_d K_o F(s)} \quad (14)$$

These equations can be used for specifying transient response regarding phase input. [4]

2.2.3 Type and Order of the System

Type of the system refers to the number of poles at the origin in the loop gain G(s)H(s).

For example:

$$\mathrm{G(s)H(s)} = \frac{5}{s(s+5)} \quad (15)$$

Since there is only one pole at the origin, this system is type one.

The order of the system refers to the number of poles of the loop gain or to the highest degree in the characteristic equation which is defined as following.

$$1 + \mathrm{G(s)H(s)} = 0 \Delta \mathrm{C.E.} \quad (16)$$

Then, the characteristic equation of the equation 15 is presented below.

$$1 + \mathrm{G(s)H(s)} = 1 + \frac{5}{s(s+5)} = 0 \quad (17)$$

$$\mathrm{C.E.} = \mathrm{s(s+5)} = 5 = s^2 + 5s + 10 \quad (18)$$

The highest degree of the equation 18 is 2. Therefore, for the given loop gain, it is type one second order system. [5]

2.2.4 Steady-State Error

Steady state error evaluation can be measured with the final value theorem. It should be examined to specify whether the steady state and transient response characteristics are adequate as required. It is described in the equation 19.

$$\lim_{t\to\infty} \theta_d(t) = \lim_{s\to 0}[s\theta_d(s)] \tag{19}$$

As regards the phase input, the phase error can be described in the way shown in equation 14.

$$\theta_d(s) = \frac{1}{1 + G(s)H(s)}\theta_i(s) \tag{20}$$

Three different inputs can be applied to the system. They are typically indicated as step position, velocity, and acceleration. The response of type 1, 2, and 3 system will be presented.

Step position input is described as:

$$\theta_i(t) = C_p, t \geq 0 \tag{21}$$

Laplace notation of the step posiotion input can be written as below.

$$\theta_i(s) = \frac{C_p}{s} \tag{22}$$

C_p is the magnitude of the phase step in radians. It indicates the shifting of the phase to the input signal by C_p in radians.

Step velocity input is described as:

$$\theta_i(t) = C_v t, t \geq 0 \tag{23}$$

Laplace notation of the step velocity input can be written as below.

$$\theta_i(s) = \frac{C_v}{s^2} \tag{24}$$

C_v is the magnitude of the rate of phase change in radians per second. It indicates the frequency shifting in radians per second for input signal.

Step acceleration is described as following.

$$\theta_i(t) = C_a t^2, t \geq 0 \tag{25}$$

For the Laplace notation can be written as below.

$$\theta_i(s) = \frac{2C_a}{s^3} \tag{26}$$

C_a is the magnitude of change of the frequency rate in radians per second squared.

Transfer function of loop gain $G(s)H(s)$ for type 1, 2, and 3 can be assumed as:

Type 1

$$\mathrm{G(s)H(s)} = \frac{K}{s(s+a)} \tag{27}$$

Type 2

$$\mathrm{G(s)H(s)} = \frac{K(s+a)}{s^2} \tag{28}$$

Type 3

$$\mathrm{G(s)H(s)} = \frac{K(s+a)(s+b)}{s^3} \tag{29}$$

The final value of steady state error with step phase input for a type 1 system can be described as:

$$\theta_d(s) = \frac{1}{1+\frac{K}{s(s+a)}} * \frac{C_p}{s} = \frac{(s+a)C_p}{s^2+as+K} \tag{30}$$

$$\lim_{t\to\infty} \theta_d(t) = \lim_{s\to 0} s * \frac{s+a}{s^2+as+K} * C_p = 0 \tag{31}$$

Therefore, when a step phase is applied as an input to type 1 system, the final value steady state error is zero.

In the same way, applying three different input for three different type of system, result table can be obtained as shown below.

Table 1. Steady state phase errors for various system types (Copied from Garth Nash [5])

	Type 1	**Type 2**	**Type 3**
Step position	Zero	Zero	Zero
Step velocity	Constant	Zero	Zero
Step acceleration	Continually increasing	Constant	Zero

Zero phase error indicates that two input signals have same phase at the phase detector.

Constant phase error indicates that the phase difference exists between two input signals of the phase detector.

Continually increasing phase error indicates that the phase changes with time rate. It means the system is out of locked state.

The required system type for certain input can be obtained with the table 1. For example, if the designer wants to build the output of the system to follow the step frequency with zero phase error, the system must be type 2 at least. [5]

2.3 Hold-in, Pull-in, Lock Range

Hold-in, pull-in, and lock range are key performance parameters of PLL. They determine the required conditions of locked or unlocked state. Assume the reference input frequency ω_{in} is varied from the frequency below $\omega_o - \Delta\omega_H$ to the frequency above $\omega_o + \Delta\omega_H$.

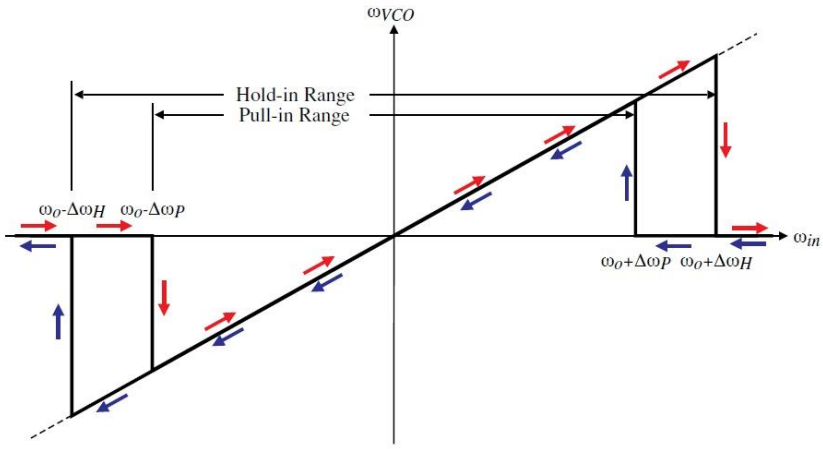

Figure 6. Hold-in, pull-in range description (Copied from Class Note ECE 6440 [6])

As described in figure 6, at first, PLL is out of lock state. After the frequency entered in pull-in range, the system achieves locked state. It maintains locked state until the input frequency deviates from the hold-in range.

2.3.1 Hold-in Range

In hold-in range, an APLL can statically maintain phase tracking. Over the phase error of $\pm\pi/2$, it cannot track the phase. Hold-in range can be specified by calculating the input frequency offset that causes the phase error of $\pm\pi/2$.

The input frequency, input phase, and Laplace notation of the input phase can be described in the equations 32, 33 and 34.

$$\omega_1 = \omega_0 \pm \Delta\omega_H \tag{32}$$

$$\theta_1(t) = \Delta\omega_H t \tag{33}$$

$$\Theta_1(s) = \frac{\Delta\omega}{s^2} \tag{34}$$

Phase error is multiplication of input phase and error transfer function as described in the equation 14.

$$\Theta_e(s) = \Theta_1(s)\, S(s) = \frac{\Delta\omega}{s^2}\frac{s}{s + K_o K_d F(s)} \tag{35}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\Theta_e(s) = \frac{\Delta\omega}{K_o K_d F(0)} \tag{36}$$

For large variation of phase difference, sinusoidal signal of phase error should be applied instead of only error phase.

$$\lim_{t\to\infty} \sin\theta_e(t) = \frac{\Delta\omega_H}{K_o K_d F(0)} \tag{37}$$

Hold-in range can be specified at the point of phase difference of $\pm\pi/2$. [6]

$$\Delta\omega_H = \pm K_o K_d F(0) \tag{38}$$

2.3.2 Lock Range

Lock range is the frequency range that PLL can be locked within one single-beat note between reference frequency and output frequency. Assume that at first, the loop is in unlocked state. The reference frequency and reference signal of PLL can be described as the equations 39 and 40.

$$\omega_1 = \omega_0 + \Delta\omega \tag{39}$$

$$v_1(t) = A\sin((\omega_0 + \Delta\omega)t) \tag{40}$$

Output signal of VCO and phase detector can be described as below.

$$v_2(t) = B\cos(\omega_o t) \tag{41}$$

$$v_d(t) = K_d \sin(\Delta\omega t) + higher\ frequency\ terms \tag{42}$$

Assume that the higher frequency terms are filtered in the loop filter. The output of the loop filter is specified as:

$$v_f(t) \approx K_d|F(j\Delta\omega)|\sin(\Delta\omega t) \tag{43}$$

This signal makes frequency modulation of the output signal of VCO as described in the figure 7.

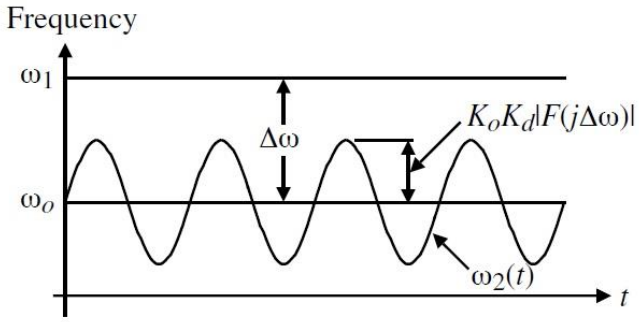

Figure 7. Frequency modulation of the output signal of VCO (Copied from Class Note ECE 6440 [6])

Locked state can be obtained if the amount of output modulation is same as, or bigger than the frequency difference of input and output of PLL. In other words, locked state can be attained if the presented equation 44 is satisfied.

$$\Delta\omega \leq K_o K_d|F(j\Delta\omega)| \tag{44}$$

Therefore, lock range can be specified as the equation 45.

$$\Delta\omega_L = \pm K_o K_d|F(j\Delta\omega)| \tag{45}$$

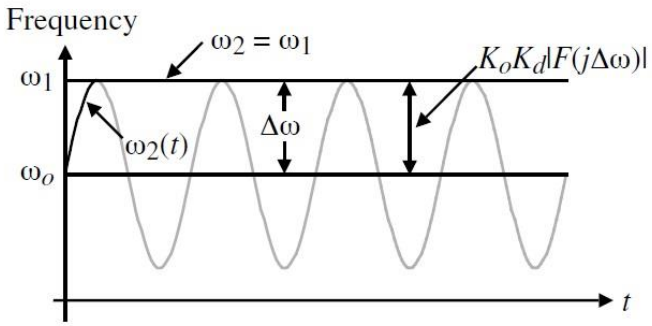

Figure 8. Frequency modulation bigger than lock-in range (Copied from Class Note ECE 6440 [6])

Figure 8 describes the case that the modulation component is bigger than the frequency difference of input and output. PLL is locked in one single beat note. [6]

2.3.3 Pull-in Range

In the pull-in range, APLL will always acquire locked state but it needs some time to be locked. Assume the loop is unlocked at first and the reference frequency is described as the equation 46.

$$\omega_1 = \omega_o + \Delta\omega \tag{46}$$

Also, assume that the VCO frequency is oscillating at the center frequency of ω_o.

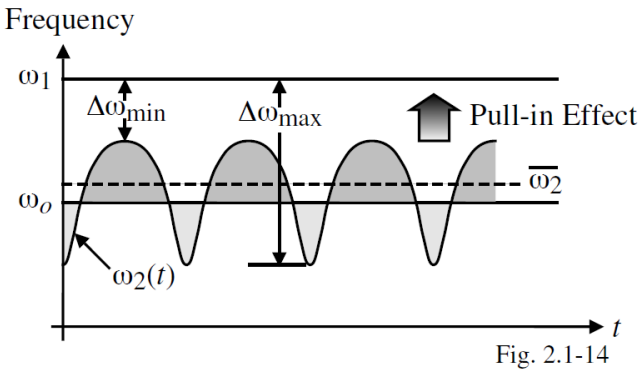

Figure 9. Pull-in effect description (Copied from Class Note ECE 6440 [6])

Because $\Delta\omega_{min}$ is less than $\Delta\omega_{max}$ as shown in figure 9, the average value of the VCO output frequency is pulled toward to ω_1.

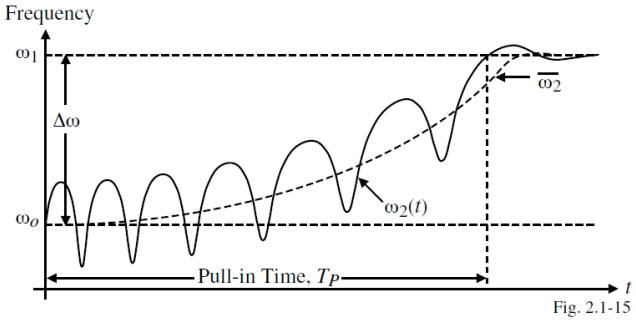

Figure 10. Practical pull-in process (Copied from ECE 6440 [6])

The time that the output frequency takes to get approached to the reference frequency is called pull-in time. Figure 10 describes pull-in process as regards time. [6]

2.4 Phase Noise

For the oscillator design, one of the most important things that should be considered is frequency stability. Long-term stability refers to the variations of the output signal for the long period of time. It is defined as a ratio of the frequency difference, $\Delta f/f$, usually expressed in percentage or in dB.

Short-term stability refers to the variations for a short period of seconds or less. These variations can be random or periodic. It can be measured with a spectrum analyzer normally. Figure 11 shows a typical result of spectrum analyzer measuring single tone signal, with random and discrete frequency components causing a broad skirt and spurious peaks.

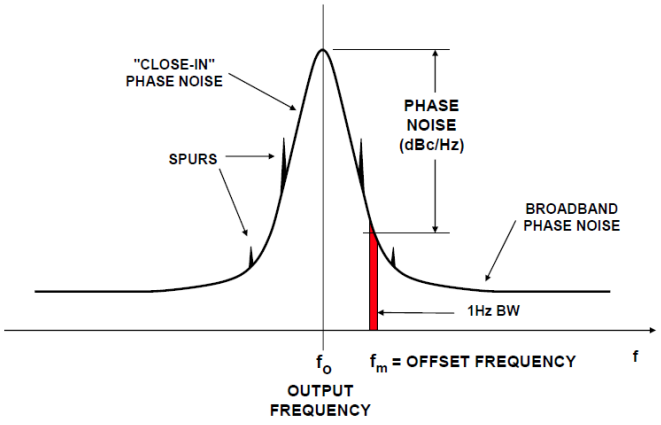

Figure 11. Oscillator phase noise and spurs (Copied from Analog Devices [4])

Clock frequencies in the signal source, power line interfaces, and mixer products would cause the discrete spurious components. The broadening of phase noise is caused by random noise fluctuation. Thermal noise, shot noise, and/or flicker noise in active and passive devices can be a reason of the phase noise.

The result of spectrum analyzer measuring phase noise shows the noise power in a 1Hz bandwidth as the function of frequency. Phase noise is defined as the ratio of the noise in a 1Hz bandwidth at a specified frequency offset, f_m, to the oscillator signal amplitude at frequency f_o.

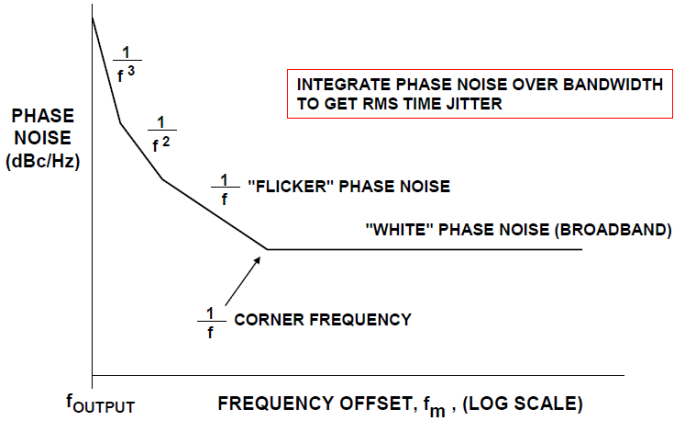

Figure 12. Phase noise in dBc/Hz versus frequency offset from output frequency (Copied from Analog Devices [4])

The characteristic of an oscillator in terms of its single-sideband phase noise can be presented as shown in Figure 12. The phase noise in dBc/Hz is described as a function of frequency offset, f_m, with the log scale for the frequency axis. The actual curve is approximated with several regions. Each region is described with the slope of $1/f^x$. The region with $x = 0$ corresponds to the white phase noise region, and with $x = 1$ corresponds to the "flicker" phase noise region. [4]

3 Components of PLL

3.1 Phase Detector

Frequency mixer is used for the APLL and its analysis methods were introduced in the previous chapter. Among many kinds of phase detectors, two representative phase detectors constructed with digital logic elements will be discussed after the additional discussion about mixer as a phase detector. They are not better than mixer in the aspect of noise performance. However, they have better pull-in range and are more manufacturable, especially for high speed applications. Besides, their low frequency response is frequently linear, rather than sinusoidal, which is a big advantage for analyzing.

For the analysis of digital phase detectors, different view is required from that of classical mixing detectors. First, they have nonlinear behaviors, but their low frequency behavior is frequently linear. Second, their circuits are built to deal with specific circuit conditions rather than for simple and general analysis. Finally, there is no best phase detector for all cases. Therefore, different types of phase detectors should be used for different cases. [3]

3.1.1 Mixer

Mixing phase detector has better noise performance since it operates at all amplitudes of the input and VCO signals, rather than quantizing them to 1 bit. Figure 13 describes the operating range of the mixing phase detector.

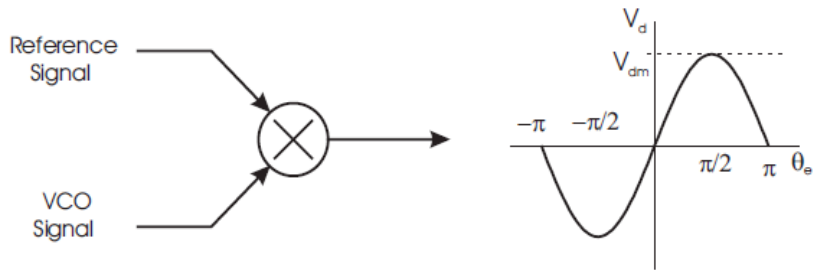

Figure 13. Classic mixing phase detector (Copied from Abramovitch [3])

But the fact that its gain is dependent upon the signal amplitude makes its analysis much difficult. Moreover, the mixer is nonideal component, therefore its nonideality should be considered in the aspect of whole loop response.

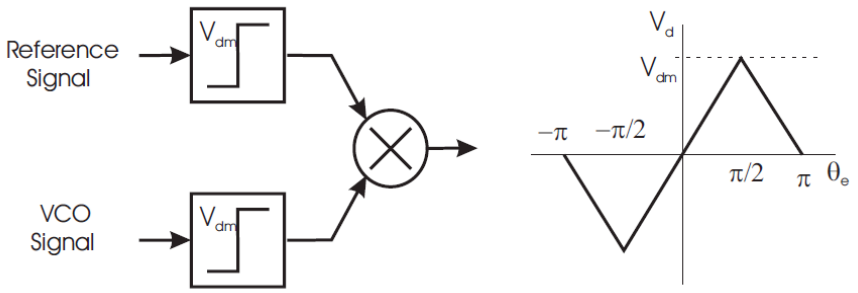

Figure 14. Overdriven mixing phase detector (Copied from Abramovitch [3])

Instead of sinusoidal clock, some loops want to have a square wave clock. If the mixer is over-driven, in other words, if the input signal is so large that the amplifiers saturate, the output signal will have a rectangular signal. Over-driven mixer operation is described in Figure 14. [3]

3.1.2 XOR

Phase detector with same operation can be implemented with Exclusive-OR (XOR) gate as shown in Figure 15. One of the advantages is that it is not dependent on input signal amplitude anymore. Moreover, it has larger linear range than a mixing phase detector.

But the disadvantage is that the relative duty cycles of the input and VCO signal affect the linearity of the baseband response.

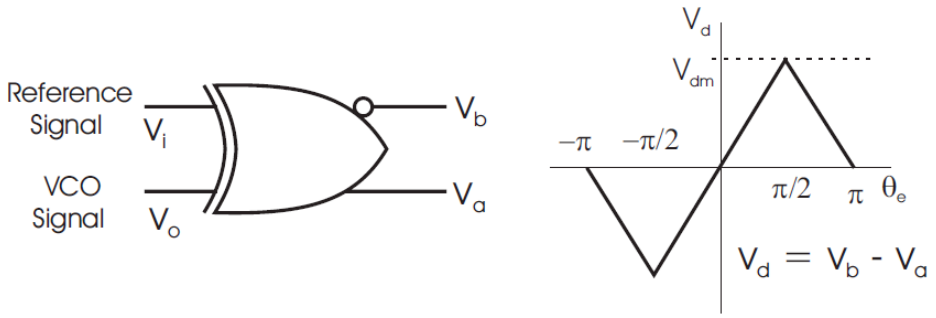

Figure 15. Operating range of XOR gate as a phase detector (Copied from Abramovitch [3])

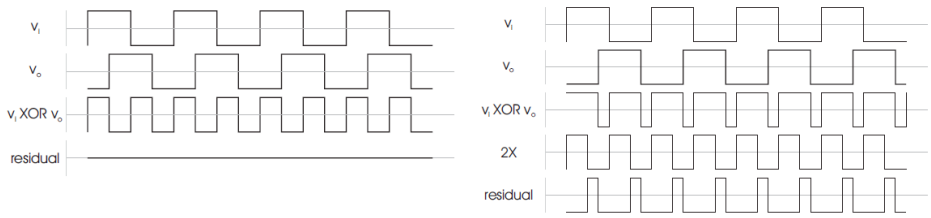

Figure 16. Phase detection using XOR gate. (Copied from Abramovitch [3])

On the left of the Figure 16, phase shift of $\pi/2$ between two inputs makes zero baseband component of the phase detector output. On the right, additional phase shift of $\pi/4$ makes $v_d/2$ baseband component of the phase detector output. This output is divided into a 2X frequency signal and a residual signal. The average of 2X signal is 0 and the average of residual signal is proportional to the baseband phase error. [3]

3.1.3 Phase-Frequency Detector

One of the most popular phase detectors is Phase Frequency Detector (PFD), typically constructed by two D-flip flops and a charge pump (CP) as described in figure 17. Each of the output of D-flip flop enables positive and negative current sources. Note that D-flip

flops are positive-edge triggered in this design. Possible logic states are shown in the table 2.

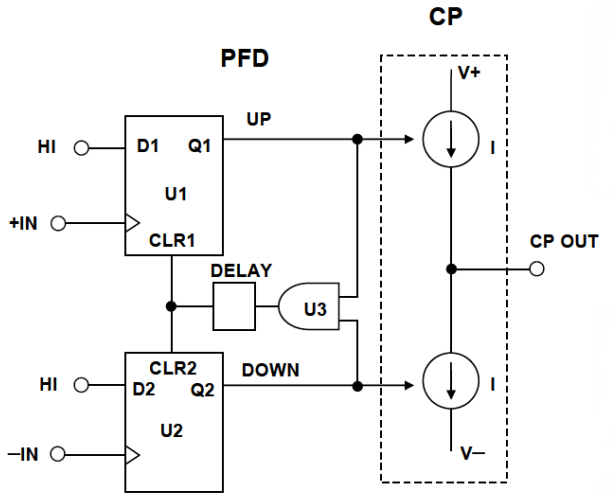

Figure 17. Popular implementation of a phase frequency detector (Copied from Analog Devices [4])

Table 2. Possible states of phase frequency detector (Copied from Analog Devices [4])

UP	DOWN	CP OUT
1	0	+I
0	1	-I
0	0	0

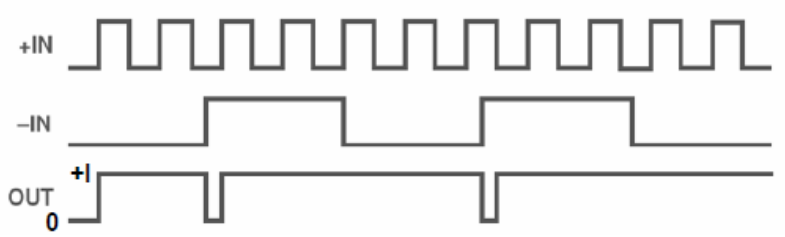

Figure 18. CP Out of the case of frequency lock and phase lock (Copied from Analog Devices [4])

If the system is out of lock and the frequency at -IN is much lower than the frequency at +IN, as shown in Figure 18, the output of CP is in the high state for most of the time. The first rising edge on +IN makes high state of output until the first rising edge on -IN occurs. This output is practically the input of the VCO, which makes the frequency on -IN higher. If the frequency on -IN is much higher than the frequency on +IN, the output of CP will be in the low state for most of the time. This will lower VCO input and the frequency at -IN will be much closer to that at +IN to make the locked condition.

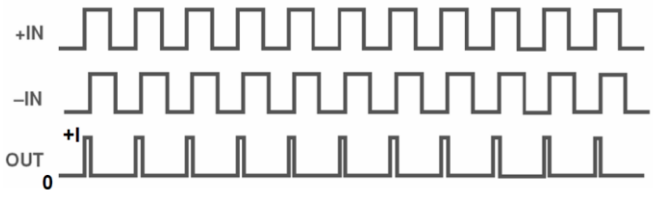

Figure 19. In frequency lock but slightly out of phase lock (Copied from Analog Devices [4])

Figure 19 describes the case when two inputs are frequency locked and close to phase lock. As +IN is leading -IN, the output is a series of positive current pulses. These pulses will drive the VCO so that the frequency on -IN become phase-aligned with the frequency on +IN. In this case, if there were no delay component between U3 and the CLR inputs of U1 and U2, the output could be in high-impedance mode, producing neither positive nor negative current pulses. It is not desired for suitable operation.

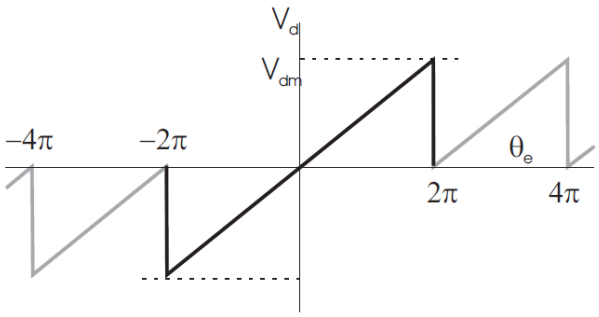

Figure 20. Phase detection using phase frequency detector (Copied from Abramovitch [3])

The VCO starts drifting when a significant phase error developed and started producing either positive or negative current pulses. Over quite long period of time, this cycling

affects the output of the charge pump to be modulated by a signal that is a subharmonic of the PFD input reference frequency. As this signal could be a low frequency signal, it would not be filtered by the loop filter and would make big spurs in the VCO output spectrum. This phenomenon is called “black-lash” or “dead zone” effect. [4]

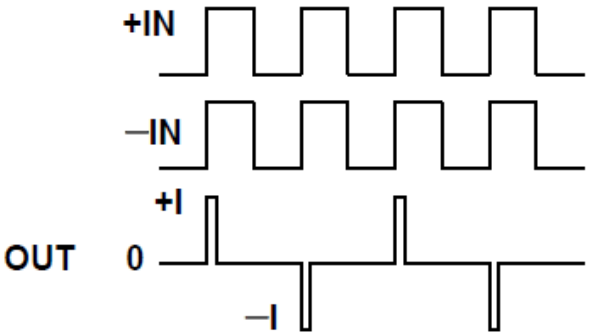

Figure 21. In frequency lock and phase lock (Copied from Analog Devices [4])

The delay element between the output of U3 and the CLR inputs of U1 and U2 ensures that does not happen. With that, even if two +IN and -IN signals are totally frequency and phase aligned, there would be current pulses at the output of the charge pump. Figure 21 describes the desired output with delay element. [4]

3.2 Voltage Controlled Oscillator

Voltage controlled oscillator is one of the most important components in PLL. The output voltage of phase detector derives VCO after filtered in the loop filter. Figure 22 describes typical characteristic curve of VCO.

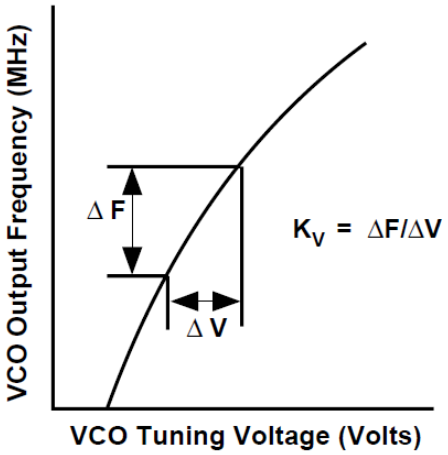

Figure 22. Sensitivity of VCO (Copied from Mike Curtin and Paul O'Brien [1])

The VCO frequency will be changed by $K_v * V_{control}$, where K_v is the VCO sensitivity with the unit in MHz/V and $V_{control}$ is the tuning voltage of VCO.

The relationship between phase and frequency is specified as following.

$$\theta = \int \omega \, dt \tag{47}$$

θ is phase and ω is frequency. Since the frequency is derived from the voltage for the VCO, the equation can be modified as below.

$$\theta_{out} = \int K_v * V_{control} dt \tag{48}$$

θ_{out} is output phase of VCO. Since the phase of the system is an issue for the system and the frequency is time derivative of phase, VCO behaves like an integrator in the loop. [7]

3.3 Loop Filter

The output of phase detector has high frequency component which is not desired for the input of a VCO. For an analog mixer as a phase detector, the output of mixer has multiple

and difference frequency components of two inputs. Since the difference frequency component is desired as an input of VCO, higher frequency components should be filtered.

Loop filter determines most of the output dynamics. It has a transfer function which introduces poles and zeroes to the system and poles determine the bandwidth of the whole system. Since higher order loop filters provide better noise cancelation, loop filter of order 2 or more is usually used for the system.

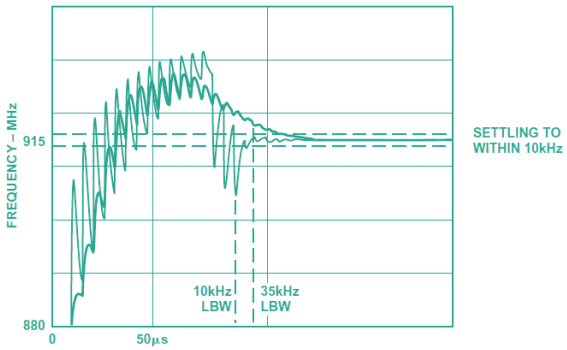

Figure 23. Lock time comparison between 35-kHz LBW and 10-kHz LBW. (Copied from Fox A. [2])

The trade-off exists for choosing loop bandwidth. Smaller loop bandwidth is desirable because total noise would be minimized. However, the system will result in slower frequency acquisition. In other words, it will need much time to obtain required frequency. Figure 23 shows the comparison of lock time for different bandwidth loop filters. [1, 2, 8]

4 Design

4.1 Voltage Controlled Oscillator Characterization

The goal of this study is to design PLL generating 100MHz at VCO. ZOS-150+ VCO from MiniCircuit is used in the circuit. Since the tuning voltage range is from +1V to +16V according to the datasheet, output frequency is measured at every 1V input voltage in table 3 to present the frequency feature. Power levels are measured at those points as

well. There are harmonics component at the output as the VCO is nonlinear component. Also, 2nd and 3rd harmonics frequencies are measured.

Table 3. ZOS-150+ VCO tuning sensitivity characterization with harmonics components

Voltage/Harmonics	1	2	3
1	70,6	140,23	210,3
2	77,4	153,28	230,6
3	82,8	164,93	246,9
4	88,2	175,5	263,0
5	93,1	185,75	278,7
6	99,0	196,10	294,5
7	104,4	207,21	310,9
8	110,2	219,4	328,2
9	116,1	231,16	347,2
10	121,9	243,78	365,5
11	128,7	255,86	384,5
12	134,9	269,12	404,4
13	141,7	282,71	423,0
14	148,4	296,30	445,2
15	155,6	309,57	465,4
16	162,4	324,13	487,0

2nd and 3rd harmonics frequencies are double and triple of the first order frequency term which are not desired in this study. The first order term is important, and it is described in the figure 24 so that the performance of the VCO can be monitored easily.

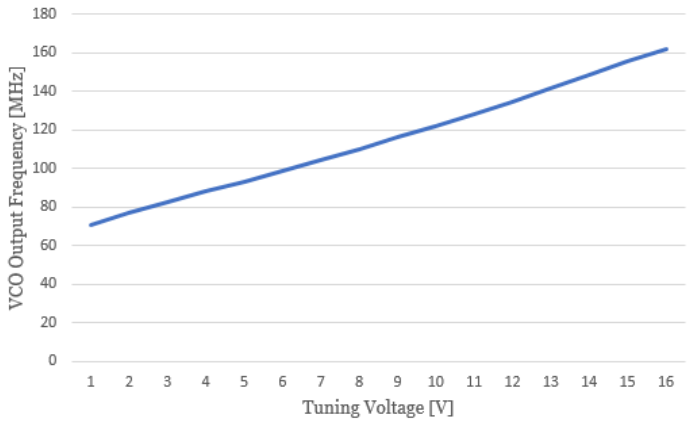

Figure 24. ZOS-150+ VCO Tuning sensitivity graph from 1V to 16V

Results shows that ZOS-150+ VCO has linear tuning sensitivity. Tuning sensitivity at every point is consistently 5.8MHz/V which is same as the datasheet. Since the tuning sensitivity vicinity of 100MHz is important in this design, tuning voltage of every 1MHz VCO frequency point from 91MHz to 110MHz is measured to present accurate tuning sensitivity around 100MHz.

Table 4. ZOS-150+ VCO Tuning sensitivity table from 91MHz to 110MHz

Frequency [MHz]	Tuning Voltage [V]
91	4,62
92	4,82
93	5,01
94	5,2
95	5,39
96	5,58
97	5,77
98	5,97
99	6,14
100	6,33
101	6,5
102	6,69
103	6,87
104	7,05
105	7,23
106	7,4
107	7,57
108	7,74
109	7,90
110	8,08

Data from table 4 can be visualized as figure 25.

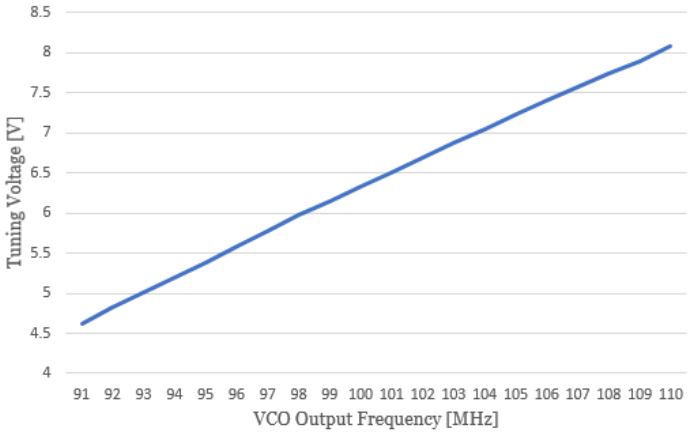

Figure 25. ZOS-150+ VCO tuning sensitivity graph from 91MHz to 110MHz

Tuning sensitivity between 91MHz to 110MHz is specified constant 5.8MHz/V and this value can be used for the calculation later.

Table 5. ZOS-150+ VCO Power in dBm for the voltage from 1V to 16V with harmonics components

Voltage/Harmonics	1	2	3
1	9,47	-24,11	-17,72
2	9,57	-18,21	-17,14
3	9,64	-16,00	-16,84
4	9,75	-14,85	-16,63
5	9,81	-14,15	-16,42
6	9,76	-13,81	-15,96
7	9,78	-13,32	-16,43
8	9,84	-13,18	-16,32
9	9,79	-13,20	-16,13
10	9,82	-13,16	-16,75
11	9,76	-13,26	-16,86
12	9,81	-13,29	-17,04
13	9,71	-13,44	-17,5
14	9,71	-12,26	-18,70
15	9,60	-13,35	-18,86
16	9,56	-13,63	-18,10

Power level of VCO should be considered since mixer is dependent on the power levels of its inputs. As specified in the table 5, all power levels of first order term for every 1V input voltage are between 9.9dBm and 9.5dBm and they are not significantly variable each other. Therefore, the power output of VCO can be simply assumed 9.5dBm.

4.2 Loop Filter Design

Two different loop filters will be implemented in this design. For easy comparison, same type but different form of loop filters will be designed. First one is single-pole, single-zero passive filter. It has two resistors and one capacitor. Electrical schematic of it is described in figure 26.

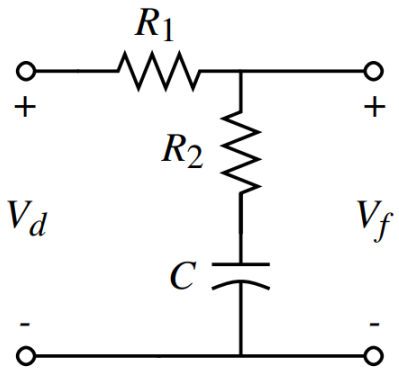

Figure 26. Schematic of single-pole single-zero passive loop filter (Copied from Class Notes ECEN 620 Network Theory: Broadband Circuit Design [9])

The transfer function of this loop filter is specified as equation 49 and 50.

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{49}$$

$$\tau_1 = R_1 C \qquad \tau_2 = R_2 C \tag{50}$$

Since the pole point is lower than the zero point, it is called lag-lead filter. From the transfer function, gain bode plot of this loop filter can be drawn as figure 27.

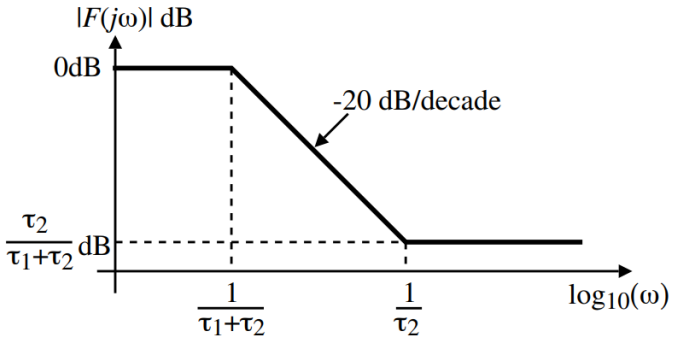

Figure 27. Gain bode plot of single-pole single-zero passive loop filter (Copied from Class Notes ECEN 620 Network Theory: Broadband Circuit Design [9])

Since there is no pole at the origin, this loop filter can be used for designing type-1 PLL.

Second loop filter is single-pole single-zero active loop filter. It has an op-amp, three resistors and a capacitor. Electrical schematic of it is described in figure 28.

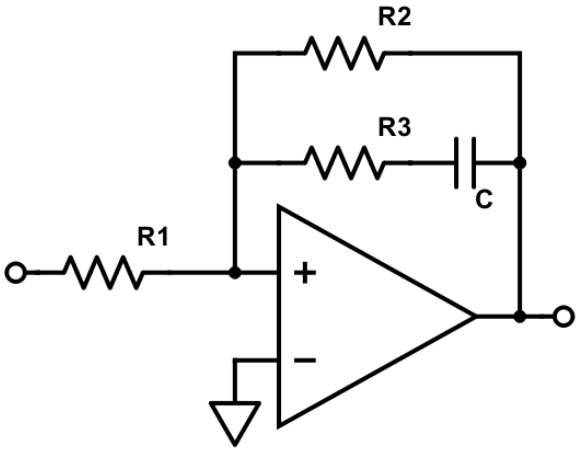

Figure 28. Schematic of single-pole single-zero active loop filter

The transfer function of this loop filter is specified as equation 51 and 52. [10]

$$F(s) = -K_a \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{51}$$

$$\tau_1 = R_2 C \qquad \tau_2 = R_3 C \qquad K_a = \frac{R_2}{R_1} \tag{52}$$

Since those two loop filters have same type of transfer functions, bode plot can be described alike in this case also. However, the biggest difference from the previous is that the total gain can be controlled with the resistance value in this case. It will affect the whole operation and their results will be compared.

4.3 Phase Detector Characterization

Double balanced mixer ZX05-1L+ from Minicircuits will be used as a phase detector. As described in the equation 10, the output of mixer is the multiplication of two input signals. Input reference signal will be applied to RF port and VCO output signal will be applied to LO port.

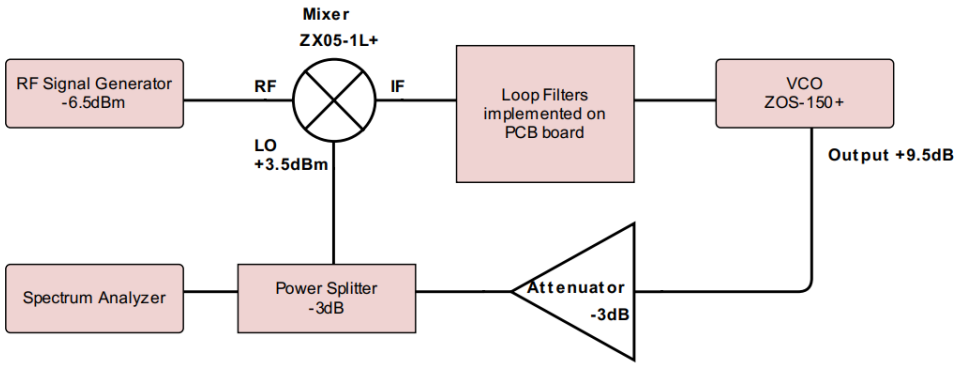

Figure 29. Block diagram of the whole designed set

Whole test block diagram is described in figure 29. According to the reference, if the power of RF signal is within 10dB of LO power level, the IF output power and RF power will not have a constant ratio of conversion loss [12]. In other words, RF and IF power will not show a constant difference in dB and that will hinder the accuracy of total test set. Therefore, the design should have 10dB power difference between RF and LO port. Power splitter is required to feed both LO port of mixer and input of spectrum analyzer to examine the output of VCO and each output is 3dB attenuated compared to the input of it. Since recommended LO power of ZX05-1L+ frequency mixer is +3dBm [10], typical output power of VCO is +9.5dBm and 3dB is attenuated by power splitter, about 3dB more attenuation is required, therefore 3dB attenuator is implemented at feedback loop.

For RF port, -6.5dBm power generated at the signal generator will be applied so that mixer can take the power difference of 10dB.

4.4 Polarity Inversion and Level Shifting of Loop Filter.

Loop filters will be implemented on the separate PCB boards. Since the DC polarity of mixer is negative, which means that the mixer will generate negative current proportional to the phase difference of RF and LO signal and positive current is required to operate VCO, inverting buffer is implemented for the passive loop filter. Active loop filter does not require a polarity inversion since the transfer function of equation 51 itself has negative polarity.

As described in table 4, VCO generates 100MHz frequency with the input voltage vicinity of 6.3V. There is a limit for DC current that mixer can generate. At least it cannot generate a DC voltage of 6.3V. Therefore, bias voltage of VCO should be set by adding level shifter. It can be implemented with potentiometer and DC voltage.

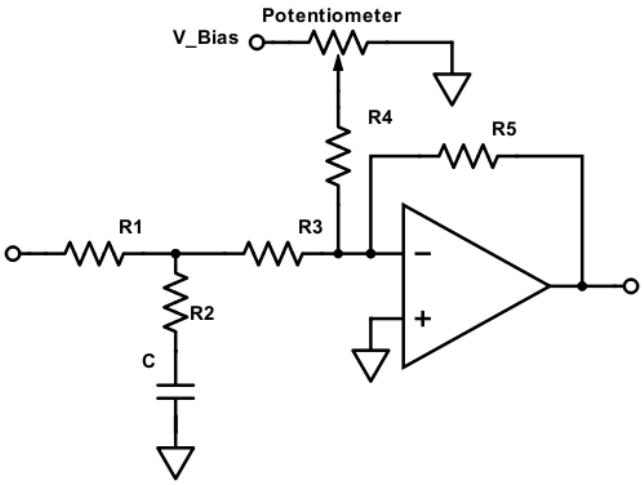

Figure 30. Passive loop filter set

Figure 30 describes a set of the passive loop filter, level shifter and inverting buffer. Level shifter is integrated with inverting buffer to minimize the noise. For the unity gain of the inverting buffer, resistance value R3 and R5 should be same. As the op amp set behaves

like a voltage summer, resistance value R3 and R4 should be equal as well. For even distribution of bias voltage with the control of potentiometer, it would be better to have an identical potentiometer resistance with R4. To conclude, it would be best to set R3, R4, R5 and potentiometer resistance in same value. Bias voltage applied to the potentiometer should be negative value since it will go through the polarity inversion with inverting buffer and will be eventually applied to VCO as a positive voltage.

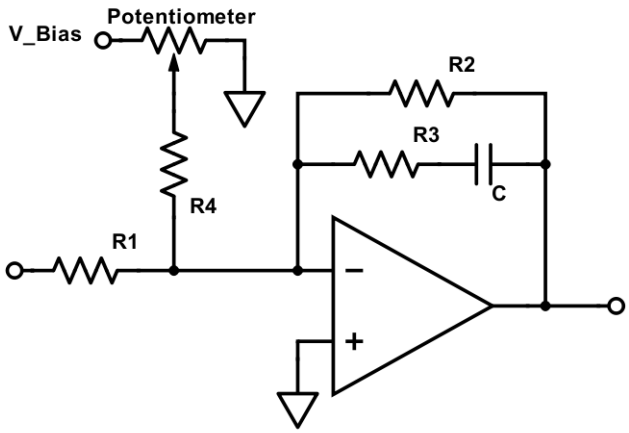

Figure 31. Active loop filter set

Figure 31 describes a set of active loop filter and level shifter. As mentioned before, for the active loop filter, inverting buffer is not required since the loop filter itself has a polarity inversion. The negative bias voltage for the loop filter should be applied as well. In this case also, resistance of potentiometer, R1, R4 value should be same because this set behaves like a voltage summer.

5 Measurement

5.1 Pole and Zero Points Calculation

Loop filter should have a low pole point to get enough attenuation for high frequency terms. Passive loop filter set with real resistance and capacitance value is described in figure 32.

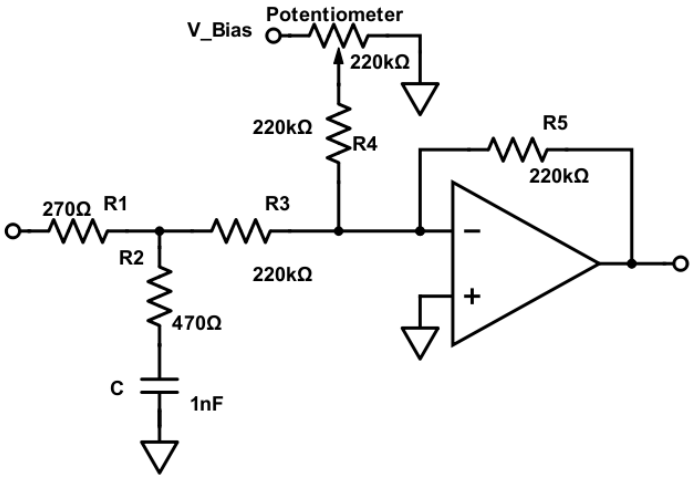

Figure 32. Passive loop filter set with resistance and capacitance value

For the passive loop filter, 270 ohms resistor is used in series and 470 ohms resistor is used in parallel. Note that the output impedance of mixer is 50 ohms and it affects to the series resistance. One Nano farad (F) capacitor is used. Pole point f_p and zero point f_z of this loop filter is calculated as the equations 53 and 54.

$$f_p = \frac{1}{2\pi * (270 + 470 + 50) * 10^{-9}} = 201[\text{kHz}] \tag{53}$$

$$f_z = \frac{1}{2\pi * 470 * 10^{-9}} = 338[\text{kHz}] \tag{54}$$

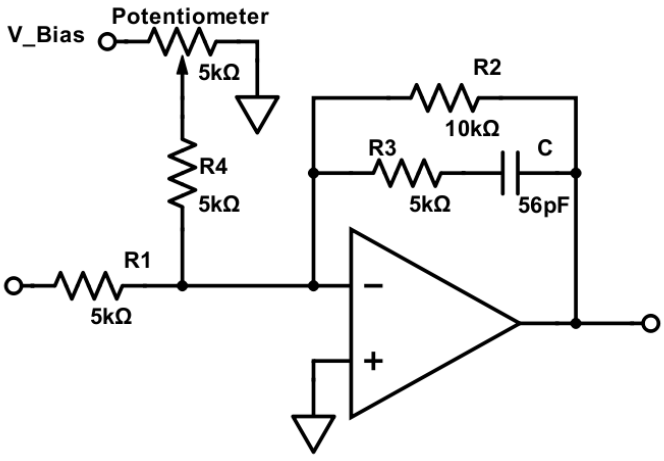

Figure 33. Active loop filter set with resistance and capacitance value

Resistor and capacitor used in active loop filter is described in figure 33. Pole and zero point can be calculated as following. Since the mixer output impedance 50 ohm cannot affect the series resistance R1 drastically, it can be ignored.

$$f_p = \frac{1}{2\pi * (10+5) * 10^3 * 56 * 10^{-12}} = 189[\text{kHz}] \quad (55)$$

$$f_z = \frac{1}{2\pi * 5 * 10^3 * 56 * 10^{-12}} = 568[\text{kHz}] \quad (56)$$

5.2 Hold-in Range Calculation

From the equation previously mentioned, hold-in range of each loop filter can be calculated. Before that, mixer constant should be measured with following test set described in figure 34. [11]

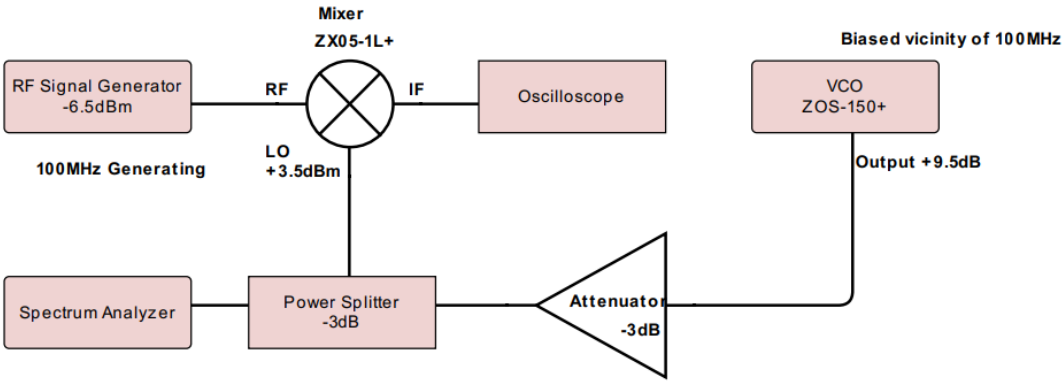

Figure 34. Mixer constant measurement test set

VCO should be biased to have output frequency of 100MHz so that mixer can generate close to DC voltage. The amplitude of the output sinusoidal wave of mixer observed at oscilloscope can be used as a mixer constant in a calculation. Mixer constant is specified as 4.475/2=2.2375V/rad. Captured data can be seen in the appendix 1. VCO constant is specified as 5.8 MHz/V=36.424 Mrad/s/V from the figure 25.

Hold-in range of passive loop filter is calculated as the equation 57.

$$\Delta\omega_{Hp} = \pm 2.2375 * 36.424 * 10^6 = 81.5[\text{MHz}] \quad (57)$$

Hold-in range of active loop filter is calculated as the equation 58.

$$\Delta\omega_{Ha} = \pm 2.2375 * 36.424 * 10^6 * 2 = 163[\text{MHz}] \quad (58)$$

Since the gain of active loop filter is 2 which is the ratio of R2/R1 in the test set, the hold-in range of active loop filter is twice that of passive loop filter.

5.3 Hold-in Range, Pull-in Range Measurement

Hold-in range can be experimentally specified by adjusting the input reference frequency. The loop should be locked to begin with. After adjusting a bias voltage to take 100MHz output frequency of VCO, reference signal of 100MHz frequency should be applied to the RF port of mixer. Then the loop will be locked. Hold-in range is the maximum frequency range of signal generator that the system can maintain a locked state.

Pull-in range can be experimentally specified by increasing or decreasing the input reference frequency. The loop should be unlocked to begin with. After adjusting a bias voltage to take 100MHz output frequency of VCO, input frequency much lower than 100MHz or higher than 100MHz should be applied to the RF port of mixer. The system will be still out of locked. When the input frequency is increased or decreased toward to 100MHz, loop will be locked at some point. Pull-in range is the frequency range it achieves the locked state. Centered at vicinity of 100MHz, both side of range should be measured. [11] Measured hold-in and pull-in ranges for both loop filters are presented in the tables 6 and 7.

Table 6. Hold-in and Pull-in range of active loop filter

Active Loop filter	Range higher than 100MHz	Range lower than 100MHz	Total range

Hold-in range	98.499MHz - 100MHz	100MHz – 101MHz	2.501MHz
Pull-in range	99.01MHz – 100.013MHz	100.013MHz – 101.01MHz	2MHz

Table 7. Hold-in and pull-in range of passive loop filter

Passive Loop filter	Range higher than 100MHz	Range lower than 100MHz	Total range
Hold-in range	9.52MHz - 100MHz	100MHz – 100.605MHz	1.085MHz
Pull-in range	99.98MHz- 100.184Mhz	100.184MHz – 100.370MHz	390kHz

5.4 Phase Noise Measurement and Comparison

Phase noise can be measured with spectrum analyzer. Most of the spectrum analyzers have phase noise calculation function itself. The data will be captured at the frequency offset of 100kHz and 200kHz for each loop filters. Tables 8 and 9 show the result of the phase noise measurement. Detail captured data of the phase noise can be seen in appendix 3.

Table 8. Phase noise with active loop filter

Offset Frequency	Phase Noise (dBm/Hz)
100kHz	-89.28
200kHz	-103.65

Table 9. Phase noise with passive loop filter

Offset Frequency	Phase Noise (dBm/Hz)
100kHz	-94.3
200kHz	-74.01

6 Discussion

The first goal to achieve a locked state of the analog PLL system was attained successfully, and two outputs were compared. Although the result of passive loop filter achieved locked state, it had so much spurious signals at every 230kHz offset frequency point at the output. The total shape of the output is presented in the appendix 2. Power levels of the output were far lower than expected value of 4dBm. Furthermore, the power difference of spurious signal and the carrier signal was not big. Desired data could not be attained with those problems.

At first, the goal of the thesis was to compare the pure passive and active loop filter so that the noise can be compared for both cases. However, because of the polarity problem, inverting buffer which has an op amp was used for the passive loop filter and that means that it is no longer pure passive filter. When the pole and zero points were a little changed by changing resistor and capacitor, the output could not achieve the locked state. To start with, the pole and zero points were meant to be designed to have far different point for two loop filters to compare the difference of phase noise. Because the system was so fragile, there were somewhat suitable pole and zero points to achieve locked state so those points couldn't be designed to be too different. Instead, after that, they were tried to be designed to be subequal. However, because of the limits of the passive components in the laboratory, they were not even designed really close each other for each loop filter. Therefore, they could not make meaningful comparison for the outputs.

Calculated hold-in range and measured one were too different. Error from the mixer constant measurement with oscilloscope, which presented so much noise, and the accuracy of manual method to measure the pull-in and hold-in range could be the reason. However, the hold in range of active loop filter was much wider than the one of passive loop filter as expected because of the gain it has. The impact of gain of the loop filter to the hold-in range was verified from this fact although the amount of different is not exactly twice.

7 Conclusion

In this thesis, the whole PLL system and their components are discussed, analyzed, and measured. The whole theoretical part of the system is discussed, and each component is studied and analyzed. Loop filters are designed, and pole and zero points are calculated in a proper method. System parameters are measured with spectrum analyzer and oscilloscope. The final goal of this study is to specify the importance of the loop filter in the whole PLL system. Main factor to impact hold-in and pull in range is the difference of gain of loop filter. Expected results are measured at the end and the impact of loop filter is verified.

There are many ways to improve this study. First, there are many other methods to minimize the entire noise. For example, crystal oscillator could be used for the frequency

source instead of the signal generator in the laboratory. Noise coupling part for the direct power supply in the loop can be added. However, because the main purpose of this thesis was to design proper loop filter and achieve locked state, designing pole and zero points is more concentrated on the process. Loop filters were implemented with passive and active components soldered on the printed circuit board and determining pole and zero points underwent a great amount of trial and error. Those processes consumed a lot of time.

In this design, there is no frequency divider in the system. Although it will not be pure analog PLL, if the system is altered a little bit, frequency divider can be added at the feedback loop and multiplied output frequency can be measured at the output.

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Captured Mixer Constant on the Oscilloscope

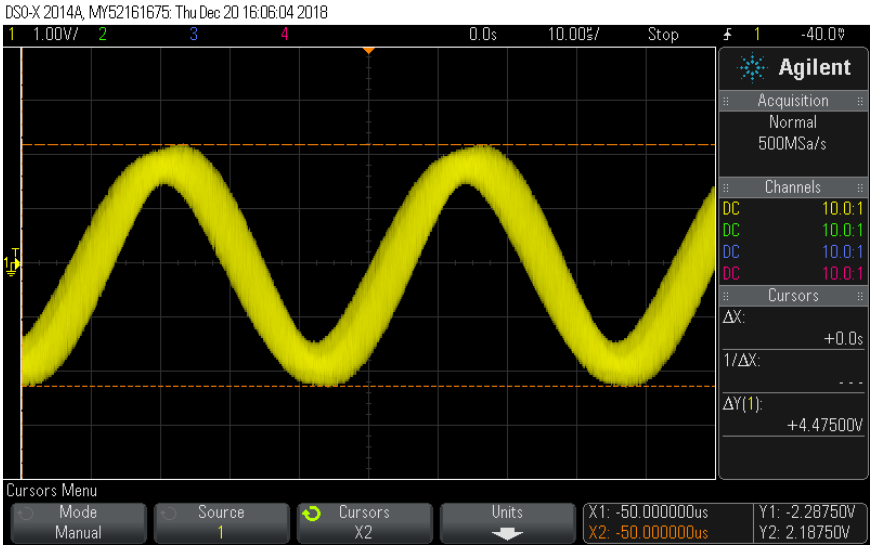

Figure 35. Mixer constant captured at the oscilloscope

Overall captured shape of the output

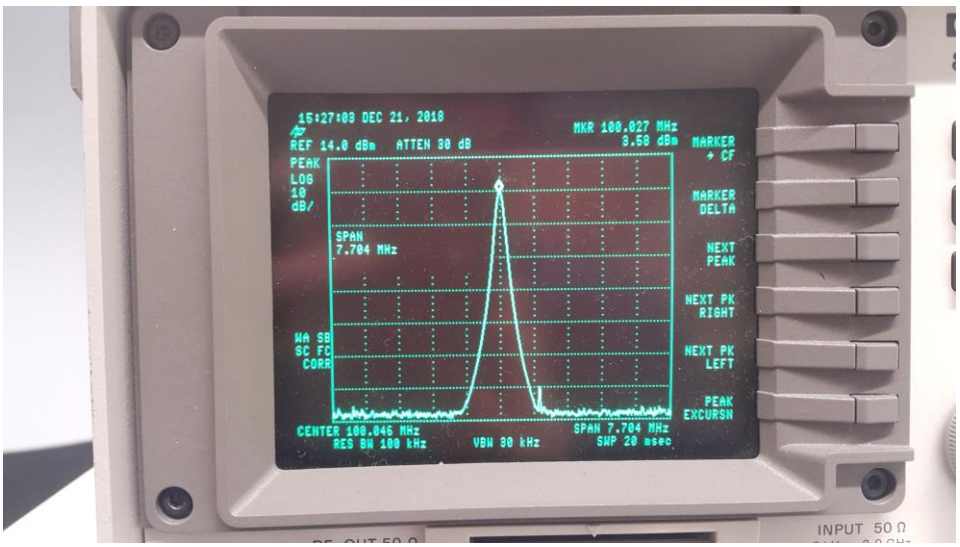

Figure 36. Overall captured shape of the output with active loop filter

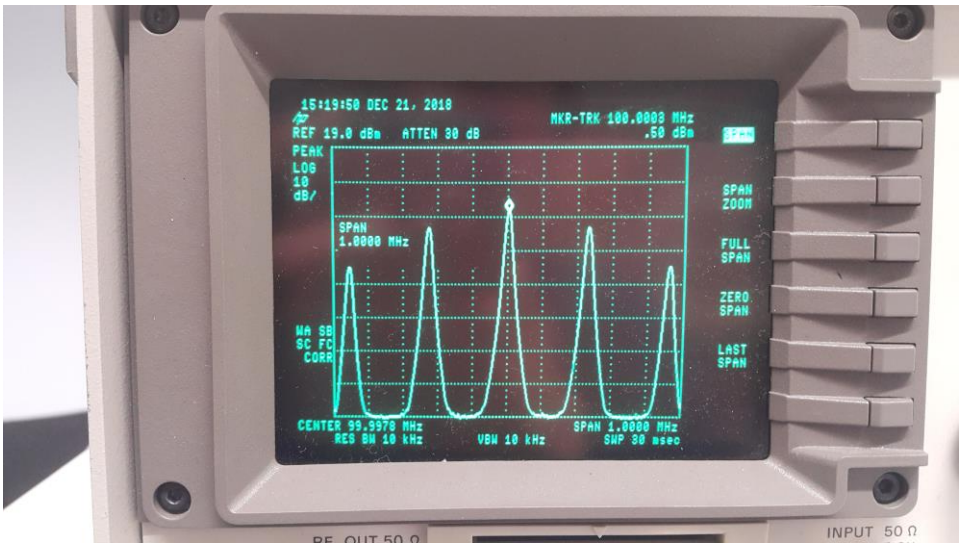

Figure 37. Overall captured shape of the output with passive loop filter

Phase noise captured on spectrum analyzer

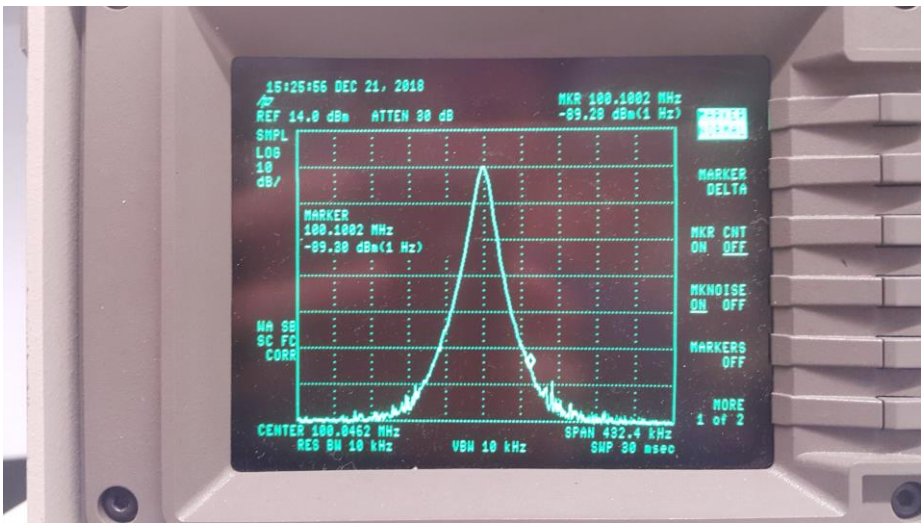

Figure 38. Phase noise of the system with active loop filter offset frequency of 100kHz

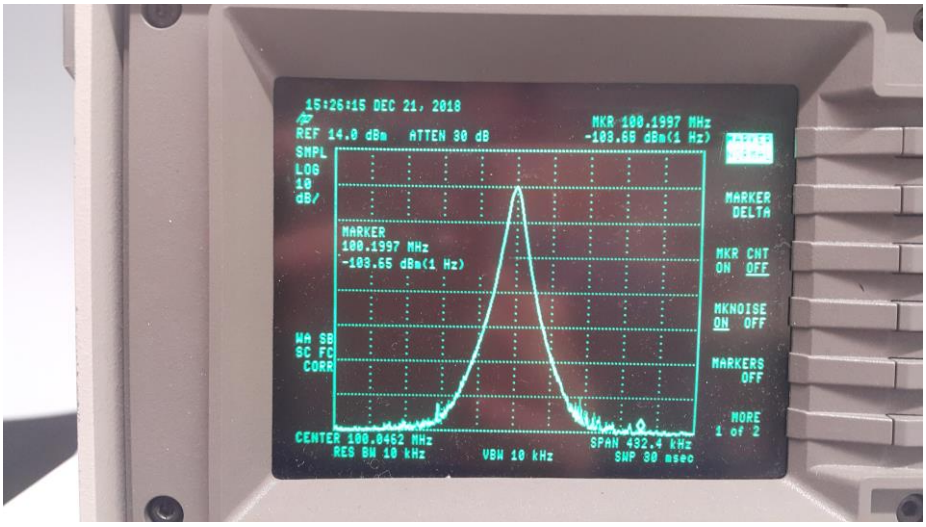

Figure 39. Phase noise of the system with active loop filter offset frequency of 200kHz

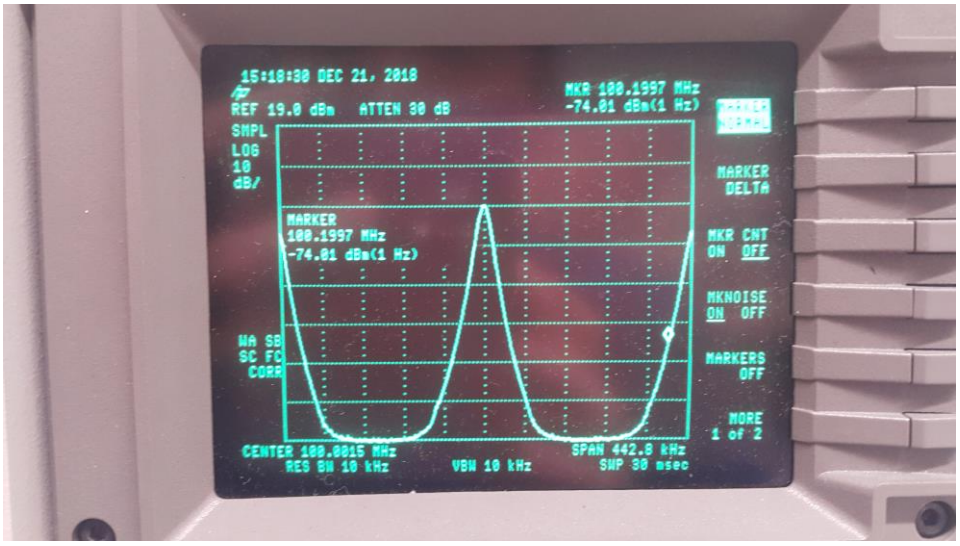

Figure 40. Phase noise of the system with passive loop filter offset frequency of 200kHz

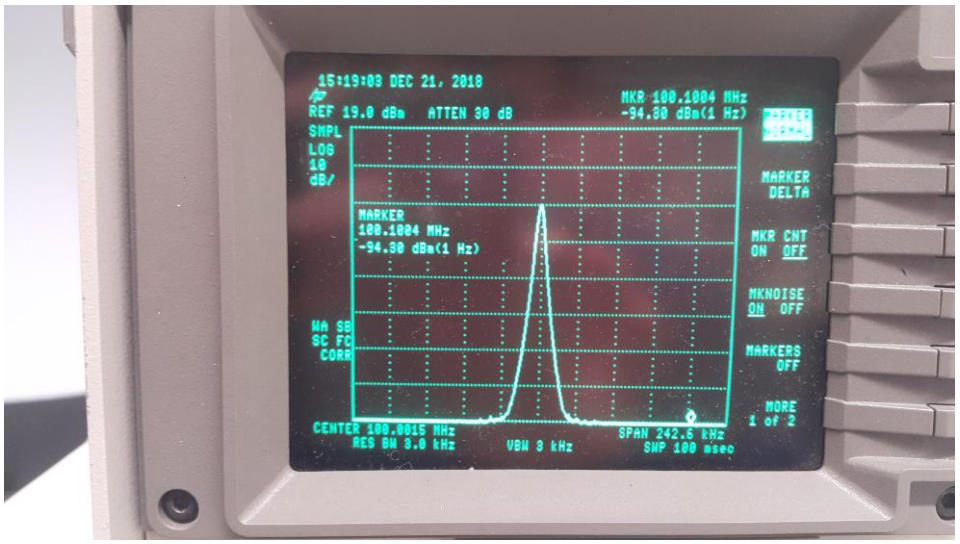

Figure 41. Phase noise of the system with passive loop filter offset frequency of 200kHz