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USE OF STRESS SCREENING IN ELECTRICAL SYSTEM PRODUCTION QUALITY CONTROL

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USE OF STRESS SCREENING IN ELECTRICAL SYSTEM PRODUCTION QUALITY CONTROL

The contemporary complex electrical and electronic systems set high demands on production quality control to enable meeting customer expectations and to minimize costs caused by field failures. Product reliability in the context of safety-critical systems is particularly essential.

This thesis studied the applicability of highly accelerated stress screening (HASS) for an electrical system manufacturer to improve quality and reliability of products. The objective was to find cost-effective screening methods by using published literature and prior research conducted by the Manufacturer. Screen proofing was not within the scope of this thesis.

A study was conducted on HASS and related topics of product reliability, environmental stresses and economic considerations of screening based on literature to allow for an understandable report. HASS was then applied on an industrial system in a case study. The current state of system reliability was analyzed and suitable methods and product levels of stress screening were mapped to enable improvement. Based on the information initial stress screening profiles were defined for the case products and present and proposed production testing processes were compared. Proposals were given on how to proceed with screening specifications.

From the results HASS was found to be capable of improving product reliability and quality. The determination of reliability objectives for the products, the quality of failure analyses and the verification of product monitoring ability were recognized as the most important opportunities of development.

KEYWORDS:

HASS, stress screening, quality, reliability, electronics, failure, production

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RASITUSSEULONNAN KÄYTTÖ SÄHKÖJÄRJESTELMÄN TUOTANNON LAADUNVALVONNASSA

Nykyaikaiset monimutkaiset sähköiset ja elektroniset järjestelmät asettavat korkeat vaatimukset tuotannon laadunvalvonnalle, jotta tuotteet vastaavat käyttäjien odotuksia ja asennuksen tai käytön aikana ilmenneiden vikojen kustannukset pysyvät mahdollisimman alhaisina. Tuotteiden luotettavuus on erityisen oleellista turvallisuuskriittisten järjestelmien kohdalla.

Opinnäytetyössä tutkittiin vahvasti kiihdytetyn rasitusseulonnan (highly accelerated stress screening, HASS) sovellettavuutta erään sähköjärjestelmän valmistajan tuotteiden laadun ja luotettavuuden parantamiseen. Tavoitteena oli löytää tehokkuuden ja taloudellisuuden osalta tasapainotetut seulontamenetelmät hyödyntämällä julkaistua kirjallisuutta sekä valmistajan omia aiempia tutkimuksia. Seulonnan koestus oli rajattu työn ulkopuolelle.

Työssä koostettiin kirjallisuuteen perustuva HASS-tutkimus, jossa käsiteltiin ymmärrettävän lopputuloksen vuoksi myös aiheeseen läheisesti liittyviä muita asiakokonaisuuksia. Lisäksi menetelmiä sovellettiin teolliseen järjestelmään tapaustutkimuksessa. Järjestelmän luotettavuuden nykytila analysoitiin ja soveltuvat testimenetelmät ja tasot, joilla tuote tulisi testata, kartoitettiin. Tuloksina määriteltiin alustavat rasitusseulontaprofiilit kohdetuotteille sekä vertailtiin nykyisen ja ehdotetun tuotantotestauksen ominaisuuksia. Seulonnan käytännön määrittelyyn annettiin ohjeita jatkoa varten.

Tulosten perusteella todettiin, että tuotteiden luotettavuutta ja laatua on mahdollista parantaa HASS-menetelmillä. Tärkeimmiksi kehityskohteiksi määriteltiin tuotteiden luotettavuustavoitteiden selvittäminen, vikaantumisanalyysien tarkentaminen sekä testinaikaisen valvontakyvyn varmistaminen.

ASIASANAT:

seulonta, laatu, luotettavuus, rasitustestaus, elektroniikka, vikaantuminen, tuotanto

CONTENT

SYMBOLS AND ABBREVIATIONS

Symbols

A	Acceleration in g units or area
AF	Acceleration factor
BW	Bandwidth [Hz]
D	Fatigue damage or displacement
E_a	Activation energy [eV]
F	Force
K	Kelvin
N	Number of cycles
R	Reliability or temperature range
SS	Screen strength
T	Temperature in [K]
TDE	Test detection efficiency
Tu	Tustin
a	acceleration
eV	electronvolt 1.6×10^{-19} J (joules)
f	frequency
g	gravitational acceleration 9,81 m/s^2
g_{RMS}	Effective value of acceleration over a specified bandwidth normalized to g units
k	Boltzmann's constant 8,617·10–5 eV/K
t	Time
β	Material parameter of fatigue accumulation
θ	MTBF, Mean time between failure
λ	Failure rate
σ	Stress [F/A] or standard deviation

Abbreviations

AOI	Automatic optical inspection
ASD	Amplitude spectral density
AST	Accelerated stress testing
BGA	Ball grid array
CA	Corrective action
DoF	Degree of freedom
DUT	Device under test
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOL	End of life
ESD	Electrostatic discharge
ESS	Environmental stress screening
EST	Environmental stress testing
FAI	First article inspection
FCT	Functional test
FLT	Full life time
FRCA	Failure root cause analysis
HALT	Highly accelerated stress testing
HASA	Highly accelerated stress audit
HASS	Highly accelerated stress screening
HW	Hardware
IC	Integrated circuit
ICT	In-circuit test
MTBF	Mean time between failure
NDF	No defect found
PCBA	Printed circuit board assembly
POF	Proof of screen
R&D	Research and development

RMA	Returned material analysis
RMS	Root mean square
ROI	Return of investment
RTT	Rapid thermal transition
SMD	Surface mount device
SOS	Safety of screen
SUT	System under test
SW	Software

1 INTRODUCTION

The potential of stress screening to improve the quality of a manufactured electrical system is studied in this thesis. The high level objective of the project is to improve Manufacturer's business by catching and investigating sub-standard products before they are shipped out. Contribution to the objective is made within the thesis by determining the screening requirements for excellent quality control and improvement and by reflecting to existing production testing activities. The warranty and reputational costs associated with system failures can potentially be reduced by implementing the actions.

The development of electronics into more and more dense designs and the use of complex supply chains in manufacturing of electrical systems create challenges to production quality and product reliability. The issues include potentially uncompatible alternative subcontractor (e.g. component or board supplier) combinations and even counterfeit components. This is a particularly important topic for safety critical systems manufacturers. A failure of such a system may have catastrophic consequences both economical and human. Another view on manufacturing quality importance is when a system with tens of years of expected lifetime is considered. Such systems must tolerate a great amount of cumulated stress during their service life. For obvious reasons, the possibilities to increase product reliability by stress testing are of major interest to such companies.

The topic has been studied with increasing intensity from the late 1980s [1]. Several textbooks have been published on reliability engineering covering stress testing and are referred to in this thesis [1] [2] [3] [4] [5] [6]. Literature concludes that traditional stress screening practices like burn-in are inadequate to deal with the current reliability issues of high quality systems. Instead, many studies propose the use of highly accelerated stress screening methods and a cause-effect approach to reliability improvement. High economic gains are reported across the industry, but few in-detail papers are published due to significant competition advantages provided by mastering the techniques [7] [8] [9].

This thesis aims to answer the common questions regarding stress screening such as the following: "How to test? What stresses should I use and how severe? How do I know I'm not breaking good hardware? It sure is expensive, why should I test?" The thesis begins with an overview on electronics quality and reliability with definitions of main concepts. It is followed by a stress screening study based on literature in which also the methods of life

testing are outlined, as life testing is an inseparable part of stress screening [2] [6] [10]. The last part is a case study of applying the methodology on an industrial system. The case study is based on literature study and historical data. The outputs of the case study are initial requirements of fault precipitation and detection for stress screening of the case system and guidelines on further actions.

2 DEFINITIONS

2.1 Quality and reliability

The following widely accepted definitions for the terms quality and reliability are used in this thesis. They originate from European Organization for Quality Control, as stated by Pascoe [4].

The quality of a system is *"the degree to which it meets the requirements of the customer. With manufactured products, Quality is a combination of Quality of Design and Quality of Manufacture."*

Reliability describes the ability of a system to perform its designed functions in the time domain. It is defined as *"the measure of the ability of a product to function when required, for the period required in the specified environment. It is expressed as a probability."*

2.2 Electrical system testing

This thesis studies the possibilities of testing a functional system to improve quality. The system under test (SUT) consists of printed circuit board assemblies (PCBA), power supplies, power and data interconnection cable harnesses, connectors, terminals, housing and other mechanical parts. The system structure and hierarchy is presented in Figure 1.

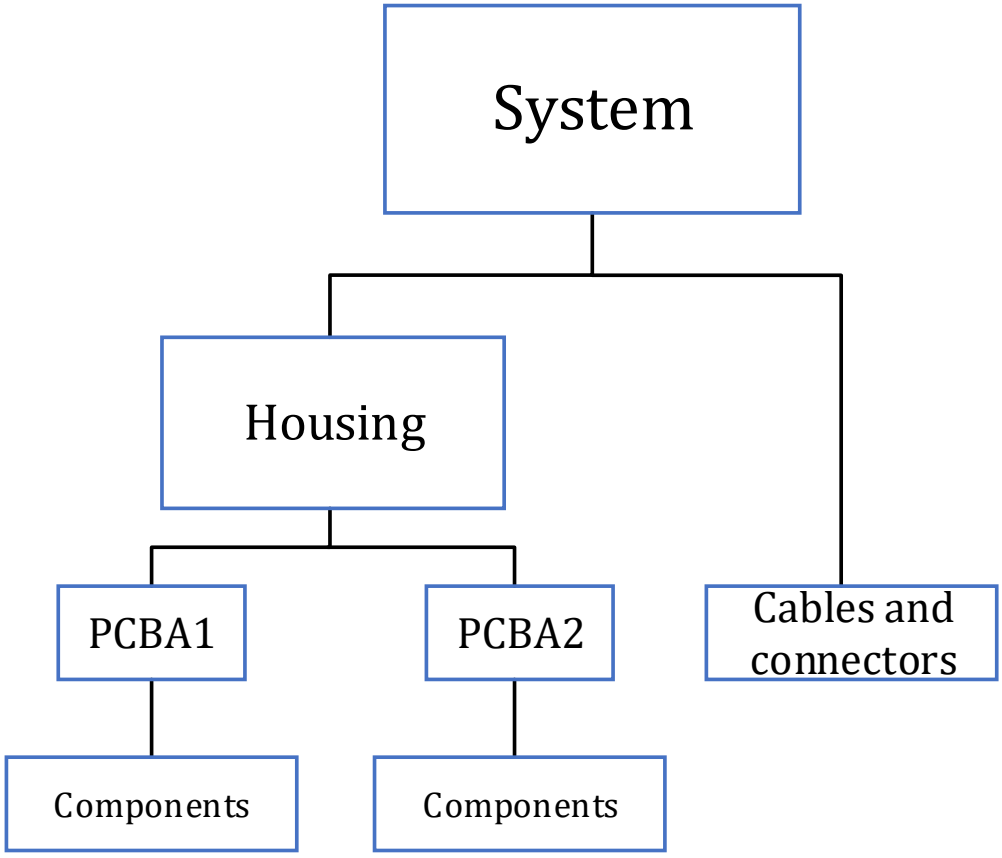

Figure 1. Hierarchical diagram of a sample electrical system according to reference [4].

In any system testing, the SUT function must be verified. Thus, system should fulfil its specification on both what it should and should not do. Testing can be sorted to 1. White box testing and 2. Black box testing by the type of test stimuli and monitoring. White box testing concentrates on the actual functionality of the components and circuits inside the system and thus refers to a lower layer test. It may incorporate manipulation of the internal signals of the system and application may be required to achieve the most efficient test conditions. Black box testing refers to testing in which only the input and output signals are monitored to verify a correct response. The exact inner functionality of the system and its modules and components to produce a corresponding output signal to given input signal is irrelevant. The benefits include that the SUT configuration will be close to what will be delivered, hence relevancy of findings is self-evident. It should be noted however, that understanding the system internals may be useful to specify the black box test structure correctly [5].

2.3 Accelerated stress testing

Accelerated stress testing (AST) refers to a set of methods and processes targeted to improve and maintain the product robustness cost-effectively by using environmental stresses beyond product specifications. Thus, AST is not a test to "spec" but a test to failure [3]. High stress levels result in a shorter testing time and lower cost, hence the word accelerated. The methods can be applied in product development, design verification, manufacturing quality control and returned material analysis [1] [2] [6].

AST incorporates the philosophy of always trying to make the product better. This does not depend on the particular method or the phase of the product lifecycle during which the methods are being used. The purpose of testing is to find problems and correct them [1] [2]. The subject is discussed more in Chapter 6.

2.4 Environmental stress screening

Environmental stress screening (ESS) is defined in literature as a production quality control process of stressing a product by employing selected stimuli. The testing strength can be significantly higher compared to production testing in benign conditions as shown e.g. in a study conducted at AT&T [8]. The objective is to find weak units by precipitating latent defects to patent defects, which are then detectable by monitoring. Thus, ESS consists of two inseparable parts: stressing the product and testing and monitoring its condition [11]. The process especially focuses on catching defects that would cause a product failure within a short period of time if delivered to field undetected [6]. These are referred to as early failures or infant-mortality failures in literature [1] [3] [5] [6]. ESS is claimed to be especially beneficial to highly complex, safety-critical systems [5].

This definition of ESS is used in this thesis. It follows that ESS is a process to uncover products that fail to meet the reliability and lifetime requirements designed in during the product development [6] [10] [11]. The target of ESS is not to find design errors, but exceptions in the production and assembly of the product and its components.

ESS is a screen meaning 100 % of products are tested. It is usually a binary pass/fail test that is targeted to be a proof of compliance to product specifications or standard/contractual requirements. ESS as a concept does not include the possibilities of

product improvement provided by testing results. This is why alternative screening methods have been developed within the AST field.

2.5 HASS and HASA

The term highly accelerated stress screening (HASS), invented by Gregg Hobbs [2] [7], is frequently used in literature. It refers to manufacturing screening process using the AST philosophy. The term is used to separate HASS from traditional ESS and highlight the aspect of extreme stress levels used. Another fundamental difference to ESS is that HASS is discovery testing, meaning it is designed to find (and correct) errors, not just to test for e.g. compliance to product specifications. It follows that HASS is not intended to prevent failures but on the contrary, its purpose is to cause failures that can then be fixed by failure root cause analysis and corrective action of the design, process, handling or whatever is found to be the cause [2] [4]. HASS is also a process whereas ESS may be called a "test". Testing is only a part of HASS process of reliability improvement [12].

Certain amount of time-compression is achieved by exposing the SUT to significantly higher stresses than those it will encounter in the field. That is, the test results are obtained in a shorter time, lowering cost of testing and speeding up corrective action process. A HASS profile must be designed to use the highest stress levels and the highest stress type combination count possible (or reasonable), and the duration of testing must be the shortest that is effective [3] [6] [7]. Still, HASS is a nondestructive test designed to screen out weak units while not causing unacceptable fatigue to units with the desired strength. The passed units will be shipped out after the test [5] [7].

When using highly accelerated stress audit (HASA) less than 100 % of products are screened. This is the only difference to HASS [3] [6]. Hence, the term HASS will be generally used in this thesis to refer to both variants as it is a widely recognized term and the difference is ignorable in most cases. The shift from HASS to HASA can be considered when the failure rate is low and the manufacturing process well controlled [2]. HASS is discussed in more detail in Chapter 6.

3 PRODUCT FAILURES AND RELIABILITY

3.1 Background of electronics reliability engineering

The reliability of electronics has traditionally been dealt with by models that predict the failure rate, or mean-time-between-failures (MTBF) for a certain product or component. The prediction method models a system's reliability as a series of the reliabilities of its components. Individual component reliability is based on historical data. Modeling is based on assumption of a constant failure rate and is expressed using an exponential equation. Equation (1) is the common notation of MIL-HDBK-217F [13], where $R(t)$ = reliability at time t and θ = MTBF.

$$R(t) = \mathrm{e}^{-\frac{t}{\theta}} \tag{1}$$

The failure rate λ is often illustrated by the bathtub curve in Figure 2. Products are thought to have an inevitable failure behavior following the shape of the curve. Initially, higher failure rates are expected due to an immature product and production process. Then, the useful life region is entered, where the constant failure rate is described by $\lambda \approx (MTBF)^{-1}$. In the wear-out or end-of-life (EOL) region the failure rate increases again due to different wear-out mechanisms in the product.

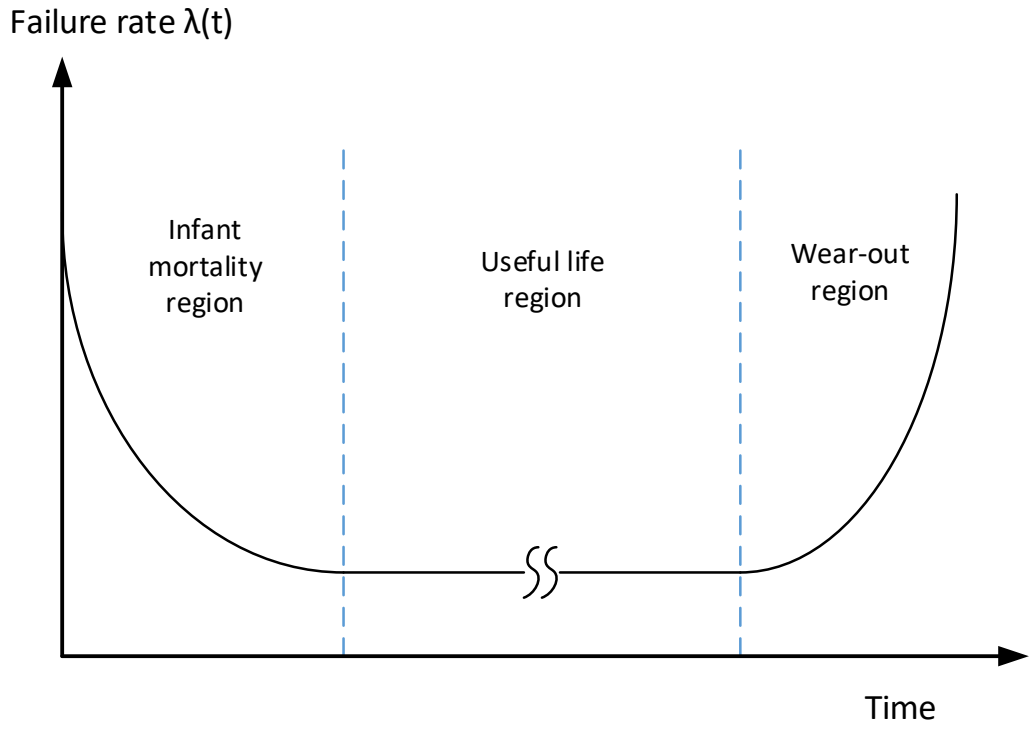

Figure 2. The bathtub curve and 3 regions of product lifecycle.

Another traditional convention related to reliability engineering is the calculation of acceleration factors on component life using the Arrhenius' equation. It is used to model the effect of elevated temperatures to component life. The acceleration factor is dependent on the activation energy of the chemical reaction of interest and the temperature delta. The Equation (2) below is Arrhenius' equation arranged to be used with semiconductor devices where AF = acceleration factor, E_a = activation energy of chemical reaction [eV], k = Boltzmann's constant $8{,}617 \cdot 10^{-5}$ eV/K, T_1 = reference temperature [K], T_2 = elevated temperature [K] [4].

$$AF = \mathrm{e}^{\frac{Ea}{k}(\frac{1}{T_1}-\frac{1}{T_2})} \tag{2}$$

According to Pascoe [4], there are shortcomings to this theory. The correct value of activation energy to model a certain failure mechanism in a certain component may be difficult to determine. An error of 0.1 eV results in approximate 2:1 error in the *AF*. Referring to tabulated survey results on activation energies in a comprehensive temperature effect study [14], deviations in the values are so great that authors conclude that reliability prediction based on Arrhenius model will not have much correlation with the realized

reliability. Another result was that there were no steady-state temperature dependencies in any of the failure modes in the temperature range -55…+125 °C, but dependencies start to increase at 150 °C. Several other authors report similar results of little correlation between predictions and actual data [2] [6] [12].

The need for an updated approach to reliability engineering should be obvious and is already adopted in many companies. By modern techniques, it has been found that almost all failures are "caused". That is, they are not due to component internal, inevitable and constant-rate malfunction but rather caused by some external event. This calls for re-considering the applicability of reliability models to electronics design, as the external events do not demonstrate the constant failure rate that is a central assumption in those models. The scrapping of the constant failure rate concept leads to the possibility of creating products that virtually never fail [2] [4]. The challenge is that there is no mathematical basis as comprehensive as within the MTBF paradigm, because a more experimental and application-specific approach is required.

Reliability models may still be useful for modeling the wear-out part of the bathtub curve in some cases, but the earlier parts of the product life cycle are certainly dominated by external failure mechanisms. This being concluded, no further discussion of the reliability prediction is included in the thesis.

3.2 Strength, stress and stress testing

A product fails when the stress on it is higher than its strength. Both the stress environment and product strength are values with a distribution. In addition, the environmental factors are only controllable to some extent by the manufacturer. A practical case of the relations of stress and strength may look like the Figure 3 below [6]. High reliability can be achieved by designing and manufacturing the product so robust that the strength distribution does

not overlap with the field stress distribution. In the case of Figure 3 the possibility of failure exists in the hatched area.

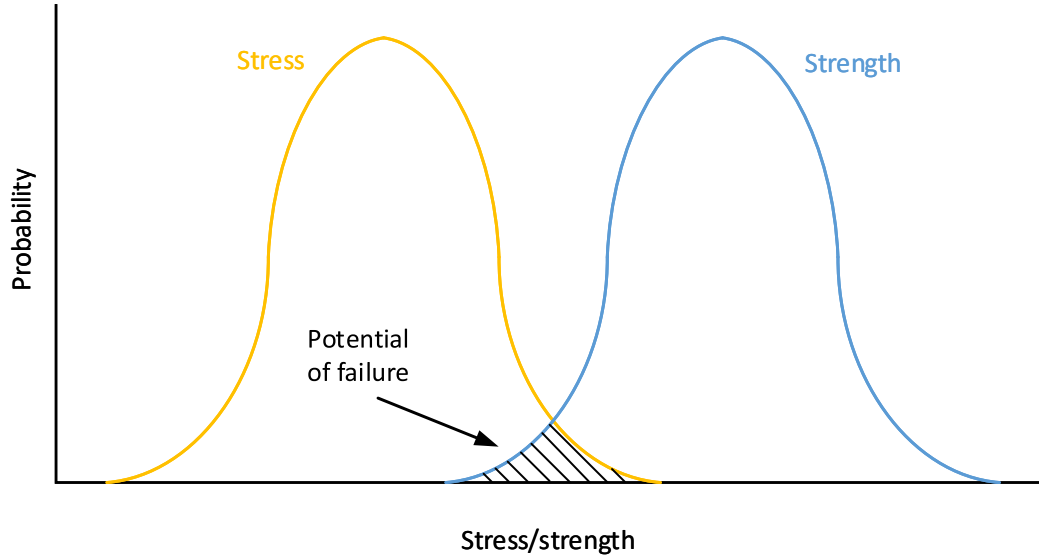

Figure 3. Stress and strength distributions and overlapping zone of potential failure [6].

The role of stress testing is to stimulate and monitor the product before the production is started (life testing) or a product is shipped (stress screening). This is achieved by artificially creating the stress in a controlled environment. Both of these processes contribute in improving the bathtub curve in the manner presented in Figure 4. Various design or process related defects may be found before the product leaves the manufacturer. Once these are fixed, the strength distribution of Figure 3 may be moved so far to the right, that the stress and strength distributions do not overlap. Thus, the potential failure area becomes 0, as does the product failure rate in the idealized case [1].

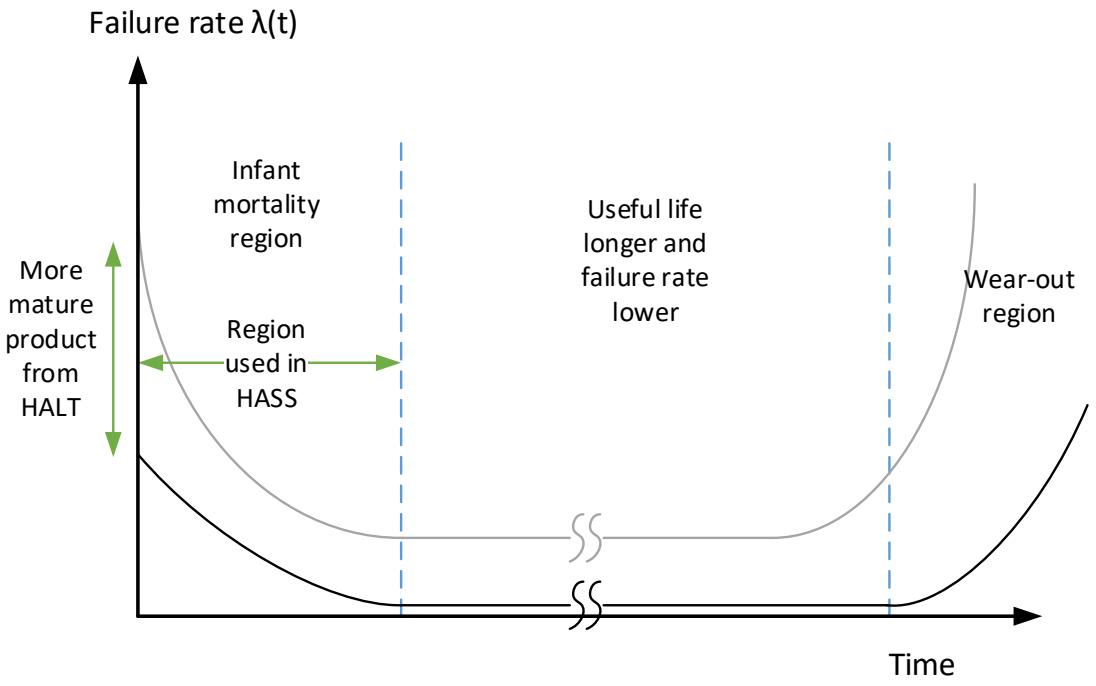

Figure 4. Effect of stress testing to the bathtub curve. The initial curve from Figure 2 is left in place for comparison [1].

The strength distribution of electronic products is generally of bimodal type. This fundamental nature of the reliability of electronics is an important consideration in stress testing, because the failures showing up early in the product lifespan are caused by different failure modes from those at the EOL zone [1].

The product failures should be categorized by the type of stress environment that leads to failure. Another categorization must be made by the physical phenomenon and mechanism that cause the failure. These differences are discussed in further chapters in more detail, as they determine the process of effective stress testing.

3.3 Failure types

According to reference [1], types of stress failures can be divided into 3 classes.

- Threshold stress failure: A certain stress level at which a product stops functioning correctly or breaks.
- Cumulative stress failure: A failure caused by fatigue induced by repeated stress, where the intensity of applied stress is not capable of causing a detectable failure immediately, but when repeated it will eventually cause a product failure.
- Combined threshold and cumulative failure: Some failure types may be only noticeable when a combination of the stress types are applied.

Threshold failure type is quite a straightforward concept. It is the absolute maximum tolerated stress value for a product. If the product is stressed beyond this, an immediate failure occurs. In practice, the limiting values will have a certain amount of distribution [1]. The information on the values and their distribution should be collected from AST (e.g. HALT) results.

Cumulative failure type is a challenge to stress testing, as it causes permanent damage to the DUT. If a product is put through a production stress screen that causes a significant yet non-detectable level of cumulative damage, there is a possibility that a weak product is shipped out and an early failure occurs later [1]. To control this risk, the safety of the screening process must be verified using the process of proof of screen (POS). The development of stress screening profile is discussed more in Chapter 6.

However, cumulative failure types can be discovered by stress testing. If a product has a weak site within it, e.g. a poor solder joint, stress may cumulate very rapidly on the site. This will lead to the destruction of the defective site while the lifetime of the rest of the product (or a completely healthy product) is not significantly consumed by the test [7].

Some failure types may require both of the stress modes described above. A defective site may require a certain threshold stress after which lower stress level starts to cumulate fatigue damage more rapidly [1]. Obviously this type is a great challenge to stress screening.

3.4 Physics of failure

The physical phenomena causing failures are key factors when discussing product reliability and stress testing. POF approach aims to solve the issues of the old methods

discussed in Section 3.1. As pointed out, the actual failures occurring in the field are usually traceable to a so-called extrinsic cause: application of component, conditions of manufacturing, storage, transport, manufacturing process quality, installation, field use, maintenance and so on [6].

The specific failure modes caused to products by the conditions mentioned above have such an enormous number of variables, some of which may be very difficult to determine, that the prediction of field reliability using a model may be practically impossible [6]. This must not be interpreted as abandoning good design practices, though. The product and the use environment should still be analyzed in the early design phase to gain as good a view on stress margins, reliability and failure mode effects as possible [4]. Later, feedback is received from testing and failed units from both factory and field. These cases must be investigated thoroughly to completely understand why the product failed. This means the actual physical mechanism causing the failure. If this can be accomplished, the failure can usually be prevented from recurring by removing the pinpointed weakness in the product.

Understanding the failure mechanism also enables the application of optimized stress testing to verify the corrective action and to catch other defective units at the factory before shipping. One or more stress stimuli may be able to effectively excite a certain failure mechanism. The advantage of this can be taken if the POF is understood. However, determining the POF may be a very challenging task and it requires special equipment and competence [1] [2] [6]. These processes of root cause analysis and corrective action are discussed in Chapter 4.

3.5 No defect found

The no defect found (NDF) phenomenon covers a significant part of returned material in many electronics industries, estimates varying from 50 % to 90 % of the returns [15] [16]. It is a major cause of cost and challenge to manufacturers. NDF means that a product is reported to be faulty but the described failure cannot be reproduced or duplicated at the returned material analysis depot of the manufacturer. This leads to the situation where it is uncertain if the product has a fault in it at all or if the report is caused by a user or an operating error. Obviously, if the problem is not observed, it cannot be fixed. The fraction of returns caused by user error are out of the scope of stress screening but it should be noted that it may be significant depending on the product in question. Inadequate operating

instructions may be the root cause and the problem should be treated as a product design error.

The explanations to the population that has a defect but cannot be diagnosed can be diverse. A comprehensive cause-effect diagram for NDF electronics is developed in reference [16]. In the study the factors resulting in NDF events are split in the following manner:

1. People-related

   Lack of competence of technical personnel, bad communication of failure descriptions and even fraudulent behavior are factors of people-induced NDF cases.

2. Machines-related

   Limitations of measurements and testing instrumentation (software, resolution, calibration, interference on measurement etc.) in the returned material analysis (RMA) may lead to non-detected faults and NDF cases.

3. Methods-related

   Suboptimal failure analysis methods and processes might lead to inability to detect failures even if the equipment were adequate. If the field conditions cannot be replicated the fault may not be observed. Improper handling of returns is also a significant factor. Some failures may be healed by conditions during transport, as well as new failures may be introduced e.g. by electrostatic discharge (ESD) or mechanical vibration and shock.

4. Intermittent failures

   Products may contain various intermittent faults that may be difficult to observe. These can be located in PCB, components, interconnections, connectors, cables or software and be of several modes.

Large numbers of failed products are claimed to be caused by improper handling throughout the product lifecycle. The effects are ESD events and PCB contamination, which both can lead to intermittent failure modes that may be very difficult to diagnose. Both risks should be minimized by appropriate processes that cover the complete lifecycle with no gaps [4]. The product handling and test equipment requirements in stress screening activities are definitely not an exception to this.

Another major cause of NDF returns are software (SW) faults. It often happens that certain operating conditions cause SW to malfunction or get stuck. The failure may not necessarily be only due to SW error but may also be caused by a shift in related hardware properties. The fault is usually cleared by itself or after reset when the conditions shift again. The issue may be tricky to diagnose in the field. Some parts might be changed and then sent to RMA for research. For this reason reliability considerations are extremely important in SW development. The system should allow an effective testing mode with excellent coverage and collect as good environmental information on fault events as possible [2].

Stress screening can be used very effectively to help in NDF troubleshooting, as stated by Hobbs [15]. This can be achieved by using a HASS detection screen to stimulate and monitor a product returned from the field and declared NDF. Detection screen with temperature cycling and low level modulated random vibration has been found to simulate effectively many field environments and make the intermittent faults detectable in RMA.

4 IMPROVING PRODUCT RELIABILITY

4.1 Failure root cause analysis

The ability to analyze and correctly identify root causes behind product failures is essential to a manufacturer planning to employ any kind of stress testing, as stated in Section 3.4. An effective stress testing arrangement only precipitates and detects product failures, it does not improve quality or reliability at all [6]. A careful analysis of the detected failure is where the reliability improvement begins. Reference [1] suggests to ask "Why?" 5 times to get from a general fault description to the root cause. Unfortunately, answering the questions may be extremely difficult.

A comprehensive and systematic failure analysis process should be implemented and performed for all failures observed. The process must progress from a more general inspection to ultimately destructive operations such as sectioning of products if needed. This approach aims to avoid compromising the evidence of the failure before documenting it. According to references [1] [6], an example of a failure analysis procedure flow could be the following:

1. General investigation: Functional testing, optical inspection. Verify the problem exists. Use detection screen if required according to Section 3.5.
2. Non-destructive investigation:
    a. X-ray
    b. Scanning electron microscopy
    c. Energy dispersive spectroscopy
    d. Acoustic microscopy, detection of voids and delaminations
3. Destructive investigation:
    a. Disassembly, removing components or material obstructing further analysis
    b. Sectioning or de-capsulating of products or components

A precise documentation must be kept of findings after and during all phases. The information gathered on the failure must be stored in a database so that it can be used in the future when similar issues are confronted again. As a result of the investigations, ideally a conclusion of the failure mode and root cause is drawn. In practice however, it is common that the conclusion is left incomplete or it may even be not possible to make conclusions at all with the material and equipment available [1].

Once the physical mechanism behind a failure is known, a corrective action can be taken to prevent a similar failure mode from occurring in the future.

4.2 Corrective actions

All previous discussion in Chapter 3 has been about finding the weak spots. Corrective action (CA) means a planned action to remove the weakness from the product. It can be e.g. a PCBA design revision or a component supplier change or quality assessment. The cost and benefit of implementing a corrective action should be calculated and the decision made based on the results, as the cost of CA may be high [1].

To plan and implement an effective correction to an observed failure, the root cause must be found as stated in the previous chapter. A design correction made without a complete failure analysis is an educated guess at best. CA should always be verified by e.g. repeating the test sequence during which the fault was discovered.

An interesting question related to CA when discussing in the context of AST is whether the failures found under extremely high stresses are relevant at all to the actual field use. If a fault is only created in conditions outside the product specification, one could conclude that the expensive CA process may be unnecessary. Literature strongly agrees that the faults discovered in AST are almost always relevant also in the field use and if they are not fixed, high costs can be expected later when similar faults are reported from the field [1] [2]. In a study of temperature cycling at AT&T [8], high correlation between early faults found before stress screening and faults precipitated by AST, was found. Another case study of motor control circuit boards found a high correlation between failure modes found in step stress testing and field as well [6].

5 STRESS STIMULI AND TYPICAL FAILURE MODES

5.1 Overview

Various environmental stress stimuli can be used in accelerated stress testing to excite different failure modes. Typical stress stimuli and effects are presented in Table 1. The most relevant stimuli to stress screening are then discussed in further sections.

Table 1. Stress stimuli and associated effects and failure modes [1] [17].

Stress stimulus	Effect or excited failure modes
Temperature cycling	interconnection and packaging, die-substrate, surface mount solder joint faults
High temperature	wire-bond defects, metallization faults, low design margins, chemical and diffusion processes accelerated
Low temperature	intermittent open circuits, low design margins
Vibration	structural and support problems, resonances, cabling and connectors, surface mount solder joint faults, fatigue damage
Mechanical shock	mechanical strength, adhesion and bonding defects
Power cycling	boost temperature transients, low design margins, high current densities
Voltage margining	low design margins, marginal components
Electrical overstress (overvoltage, surge, ESD, EMI)	isolation, grounding, overvoltage protection, shielding, low design margins
Clock variations	low design margins, marginal components
Humidity	corrosion, increase in contact resistance, absorption into plastic, dielectric strength decrease
Moisture resistance	humidity effects, corrosion of contacts and wires

A single failure mode may be excited by multiple stimuli. This overlap phenomenon is often illustrated by Venn diagrams. Additionally, the acceleration gradient for a failure mode as a function of stress severity can be different depending on stimuli. Thus, a failure mode may be found in stress testing by the effect of another stress than in the field environment. This does not reduce the significance of testing findings at all [1] [2].

The phenomenon can be further illustrated by considering the example of common failure mode below, mechanical fatigue due to compression and extension. This fatigue damage is mathematically formulated by Equation (3), which is known as the Miner's criterion [2] [18].

$$D \cong N\sigma^{\beta} \tag{3}$$

where:

D = cumulative fatigue damage done

N = number of cycles

σ = stress applied (F/A) (force per unit area)

β = material property

Now, if we assume the stresses generated by thermal cycling and vibration are equal in magnitude, we can easily compare the relative effectiveness of the stimuli to an example resistor. If the test system is able to achieve a thermal cycle in 10 minutes and the resistor has a resonance at 500 Hz, the ratio of accumulated damage per second (ratio of N) becomes:

$$\frac{\text{Vibration damage/s}}{\text{Thermal cycling damage/s}} = \frac{500}{1/600} = 3{\times}10^{5}$$

It is clear that in this case, huge time consumption reduction is achieved if vibration is used instead of temperature cycling in stress testing. In reality, the stress parameter is not equal, and that explains why the cause of field failures may be different.

5.2 Thermal stress

Temperature affects material properties both mechanical and electrical. It also speeds up chemical reactions and processes such as diffusion and electromigration and affects the timing and threshold voltages of e.g. digital logic circuitry, which may cause functional errors. Temperature changes cause thermomechanical stress [19].

Thermomechanical stress has been estimated to be the cause of up to 80 % of field product wear-out failures. In accelerated stress testing the primary interest is usually on the heat transfer rate. This is one of the 2 concepts presented by Pascoe [4], another being thermodynamics. The latter describes the amount of heat transferred.

Thermal stress can be applied to the DUT with a constant value and duration, or these parameters can be changed, or cycled, during the test. The first variant is often referred to as "Burn-in", and is used by component manufacturers. As stated by reference [4], it is not a recommended thermal stressing method for assembly or system level screening. The latter variant is called thermal or temperature cycling [1] [4].

However, burn-in does stimulate some failure modes. Thus, a combination of both may often create the most effective profile. A study conducted within a telecommunications equipment manufacturer concluded that thermal cycling was a more efficient stress type compared to burn-in for the particular products under test. Still, thermal cycling alone was stated to be ineffective in precipitating time-in-temperature dependent failures [1].

Thermal cycling screen takes several input parameters which affect the effectivity of the screen [4]. In addition to those in Equation (4) also temperature dwells at the high and low extremes are significant. Thermal screen strength (SS) was modelled by Eq. (4) published in RADC-TR-82-87 [20]. Test detection efficiency is the capability of the test system to detect a present fault. The exponential term models the precipitation effect of the screen.

$$SS = TDE(1 - \mathrm{e}^{-0.0023[\ln(\mathrm{e}+dT)]^{2.7}N^{0.5}R^{0.6}}) \quad (4)$$

where:

SS = Screen Strength

TDE = Test detection efficiency factor

dT = Temperature gradient (°C/min)

N = Number of temperature cycles

R = Temperature range (°C)

From Eq. (4) worth noting is the weight of the temperature ramp rate dT. It has been experimentally shown and mathematically modeled that the temperature gradient (dT) has a greater impact on screening efficiency than the actual temperature range used [4]. Rapid thermal cycling excites mismatched thermal expansion coefficients in material boundaries such as solder joints or attachments inside integrated circuits.

Examples of failure modes stimulated by combined thermal cycling and burn-in for a fiber optic communications system (in not specific order) [1]:

1. Degradation in fiber alignment in an optical component because of poor quality soldering process.
2. Loosening of an element assembled by adhesive.
3. Certain components were manually soldered, testing revealed quality issues.

In another study of temperature cycling on motherboards following failure modes were common [8]. Worth noting is that most of the problems are located within components and that the first case is caused by combined stress environment.

1. Integrated circuit (IC) package damage induced by absorbed moisture. Reflow soldering process and later temperature cycling caused open pins due to sheared ball bonds. The cause was determined to be the absorbed moisture from improper storage of the components.
2. IC silicon damage from wire bonding. Too high energy used in wire bonding caused open pins on a component.
3. Various failures in hybrid devices. Custom integrated circuits constructed with less automation and containing many internal connections presented various failure modes. Crystal oscillators had output issues due to insufficient construction, also solder joint and internal connection faults were found on some components.
4. Interconnection failures of memory card connector due to design error.
5. PCB via failures due to issues with copper plating process.
6. SMD assembly faults due to insufficient or unsoldered joints with open or shorted pins on components.

5.3 Mechanical and vibration stress

Mechanical vibration and shock create displacement in DUT and are therefore very effective in precipitating structural and mechanical faults. It can also cause intermittent or permanent failures in vibration-sensitive components such as crystals and relays. Typical failure modes include mechanical failures of large mass components due to inadequate support, loosened fasteners, defective solder joints and design violations of the "octave rule". The octave rule states that the natural resonance frequencies of a system must stand at least an octave apart so that the responses are not amplified [1] [2] [4].

DUT can be stimulated by impulse, sinusoidal or random vibration. To achieve effective and safe vibration testing, certain requirements for the stimuli are present. Shock impulses are usually not applied in production stress screening, because the peak accelerations are likely to cause unacceptable damage to the DUT.

All products have several natural resonance frequencies. The phenomenon has some analogue to the electrical RLC resonance network behavior. Considering circuit boards and similar continuous structures (plates, beams, etc.) their resonance behavior is better compared with electrical transmission lines, as the properties are distributed over their dimensions. When these resonances are excited by external input of the resonance frequency, maximum displacement occurs. Impulse (shock) and broad band random vibration excite all DUT resonances simultaneously, compared to sine vibration that can excite only single frequency at a time. As the field environment does not exhibit clean sine vibration but rather random, unpredictable type, the impulse and random vibration are the preferred modes for stress screening applications. In addition to better simulation of field stresses, these are considered to be 1. More efficient in precipitating and detection faults and 2. More safe in terms of unwanted fatigue damage accumulation to DUT. Sine vibration has applications as well. It can be used to calibrate equipment and to study DUT natural frequencies [1].

Random vibration magnitude is normally (Gaussian) distributed. Consequently, the highest probability density is located in the lowest accelerations close to 0. Sinusoidal vibration is not Gaussian distributed, instead it has the highest probability around 1 and -1 values. This means that if slowly sweeping sine was used for stress screening, the DUT resonances would be excited with high acceleration and for a relatively long time, potentially causing excessive fatigue damage.

It is not enough that vibration frequency and amplitude are random. A maximized stress screening performance is achieved only when the system has a so-called "six degrees of freedom" (6 DoF) configuration. That is, vibration is applied simultaneously both in x, y and z and in roll, pitch and yaw motions [1].

Vibration is measured in various units. The starting point is the displacement, which is usually expressed in mm. The second derivative of peak to peak displacement D is the acceleration a, expressed by Equation (5) [1] in the units of mm/s^2.

$$a = -2\pi^2 f^2 D \sin(2\pi f t) \tag{5}$$

Acceleration is often expressed using the g unit. In Equation (6), absolute peak acceleration (sinusoidal term set to 1) is normalized by Earth's gravitational acceleration by dividing by 9807 mm/s^2 to get the dimensionless acceleration A expressed in g units.

$$A = 0.00201 f^2 D \tag{6}$$

If the vibration stimulus is viewed in the frequency domain as in Figure 5, either a wide area of relatively constant amplitude spectral density (ASD) (broad band) or a sharp single spike ASD (sinusoidal) will be observed as the input stimulus. ASD is expressed in the units of tustins [Tu] with dimensions g^2/Hz. Typical Tustin values are in the range of 0.01…1 Tu.

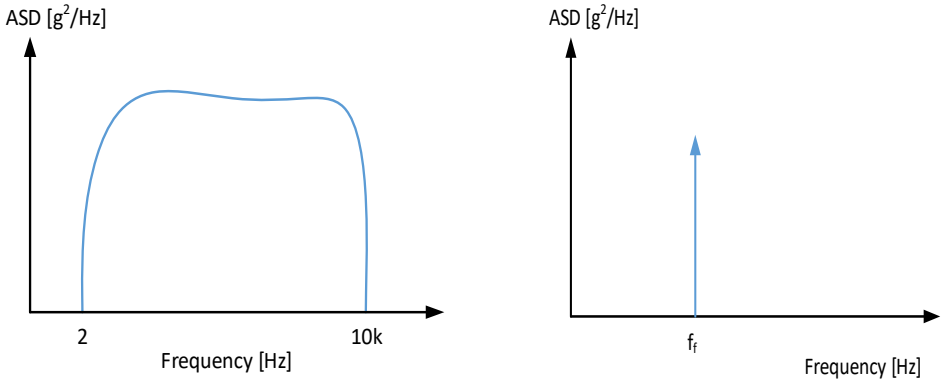

Figure 5. On the left, example of broad band random vibration ASD. On the right, example of sinusoidal vibration ASD with input frequency f_f [1].

The frequently used g_{RMS} unit, that expresses RMS acceleration in g units, is calculated by multiplying the ASD value by appropriate resonance bandwidth of DUT (Hz) and taking

square root. Resonance bandwidth(s) of DUT is typically narrow, refer to Figure 6. This means, that if a vibration table has a given g_{RMS} setting over a broad bandwidth, say 10 kHz, it does not tell anything about the acceleration on the DUT, as there are infinite number of ASD figures that will produce the same g_{RMS} over a given bandwidth. Consider the following example:

> Assume a random vibration table with a bandwidth of 2 Hz…10 kHz and vibration spectrum with nearly a "box" shape (left curve in Figure 5) and a level of 30 g_{RMS}. DUT has only 1 resonance in the test band, with a half-power bandwidth of 40 Hz (Figure 6).
>
> First, the ASD is calculated.
>
> $$ASD = \frac{{g_{RMS}}^2}{BW} = \frac{(30g)^2}{9998\ \text{Hz}} = 0.09\ \text{g}^2/\text{Hz}$$
>
> Then, the g_{RMS} (standard deviation) on the DUT is calculated as the square root of variance of ASD.
>
> $$DUT_{GRMS} = \sqrt{0.09\frac{\text{g}^2}{\text{Hz}} \times 40\ \text{Hz}} = 1{,}90\ \text{g}_{\text{RMS}}$$
>
> Most of the acceleration experienced by DUT is covered by the previous calculation. However, g_{RMS} can be calculated at 3 sigma point (3 standard deviations) to find also the higher values to be expected. Then, DUT_{GRMS} = 5.7 g_{RMS}. This covers 99.7 % of events.

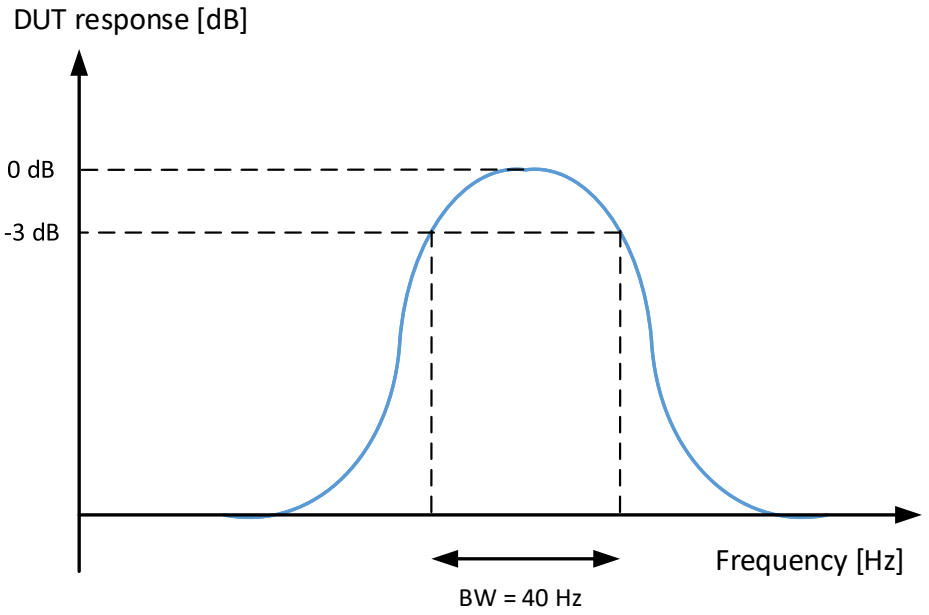

Figure 6. DUT frequency response in the case of half-power bandwidth of 40 Hz [1].

The example above should be considered when designing a vibration screen. Vibration characteristics on the DUT should be documented, as the chamber setpoint is not informative in this sense.

Other studies exist on the effects of vibration. Pachucki [9] found vibration to have a very significant effect on screening efficiency of CPU boards and to be the key stress in the screening process. With vibration applied, failure rate was 1.8 % whereas without vibration the rate was 0.6 %. It was also noticed that vibration may leave precipitated but undetected faults in the product if the detection arrangement is inadequate. Another paper [21] experimented with artificially flawed BGA soldering process and random vibration screening effect to precipitate the failures. The conclusions were that random vibration does uncover some faults but not all. It may cause some other faults as the mechanism was not completely understood.

5.4 Electrical stresses

Different electrical stresses are an important category of the stress spectrum a product encounters. They are equally important stress stimuli to be considered in stress testing. These can be further divided:

1. Voltage, current, power.
2. ESD.
3. EMI.

Most relevant to stress screening is generally the 1st category. Power cycling of DUT is a very common and effective stress that is simple to apply. It creates high current peaks caused by DUT capacitances charging and discharging, which heavily stresses sites of high current density. These are usually located at faulty areas assuming that design errors do not exist. Similar effects can be achieved by loading the DUT when applicable, generating power dissipation. These methods can be effectively combined and synchronized with rapid temperature cycling to boost the ramp rate of DUT temperature change [1].

Supply voltage variations to or within DUT can be effective means of detecting small design margins or marginal components. Supply voltage affects integrated circuits function, e.g. the timing of digital logic circuits, which may cause errors if the margins are small for some reason. Logic voltage variation may create implementation challenges to complex products with several power supplies on board. Using plain black box approach to testing may rule out this type of stress. Another related stress stimulus is clock frequency margining, with similar mechanism of uncovering marginal units.

Special case of voltage testing is electrostatic discharge (ESD). This means subjecting the DUT to high voltage peaks. ESD is usually not used in stress screening, as it is likely to cause permanent damage to the DUT. Instead, it should be used during product development to uncover potential insulation and grounding issues [1]. ESD is proposed to be a contributor to the NDF phenomenon discussed in Section 3.5, as failures induced may be intermittent and extremely hard to detect. It is certainly also the cause of multiple failures in which the fault has been located. Thus, ESD should definitely be considered in planning the stress screening process and facilities just like in the bigger picture of manufacturing, storing, delivering and installing the products [4].

Electromagnetic interference (EMI) is another electrical phenomenon which can stress the DUT by coupling into it by radiating or conducting. EMI can be used in stress screening if found appropriate for the specific DUT e.g. in HALT. More common approach to EMI testing is during the product development though as part of electromagnetic compatibility (EMC) verification testing.

5.5 Humidity and moisture stress

Humidity and moisture cause various failure modes in electronic devices. Hygrostress creates mechanical stress in a similar manner to thermomechanical stress (Section 5.2) by generating material expansion and transform due to absorbed moisture. The mechanical stress caused by moisture is formulated into an equation in reference [22]. Moisture also changes material properties such as thermal expansion and flexibility, which create similar mechanical stress when combined with changing temperature. This can cause e.g. delamination of adjacent layers in integrated circuits.

Humidity and moisture can act as electrolytes and enable electrochemical processes like corrosion and electromigration. Both cause changes in (metal) materials' structures and lead to shorts or opens in products. Corrosion happens without the presence of any other stimulus whereas electromigration happens only if an electrical bias is present. Humidity and voltage may also cause insulation breakdown if the design does not have the adequate margins.

Humidity and moisture effects on products usually occur over a relatively long time period. Hence, the stimuli may be more appropriate to highly accelerated life test (HALT, see Section 6.2) application. In production HASS, the time constraints usually prevent the application [1] [22].

5.6 Combined stresses

Some failure modes may be excited by using a certain combination of the stress stimuli, as already stated in this chapter. Common combinations are presented in Table 2. The number of possible combinations is infinite and depends on the application. The temperature is a component in almost all stress testing.

Table 2. Common stress stimuli combinations and their effects on DUT [1] [2].

Stimuli combination	Effect or excited failure modes
Temperature cycling & voltage margining	Deeper examination of design margins than with only single stress.
Temperature cycling & random vibration	Deeper examination of mechanical and structural problems, improved intermittent fault detection. Combining thermal cycling and vibration create additional stress to the DUT based on resonance characteristics shifting with temperature changes [6].
Humidity & voltage bias	Electromigration, insulation issues.
Humidity & temperature cycling	Increased corrosion and mechanical stress of component packages and connectors.

5.7 Other stresses

Stress screening arrangements must not replicate those encountered in the field or be any of those listed in Table 1. They are only required to accelerate the discovery of field-relevant failure modes and hence, only imagination is the limit when planning test profiles and stimuli to be used. However, stimuli selection should be based on facts such as the physics of failure. For electronic products screening, thermal and mechanical stress are the most common used and a good starting point [2].

6 ACCELERATED STRESS SCREENING: HASS

6.1 Introduction to accelerated stress screening

There has been a corresponding change in manufacturing stress screening as there has been in electronics reliability mindset in a wider sense described in Chapter 3. A change from compliance screening such as ESS to discovery screening is required if manufacturing quality and consequent field reliability of complex systems is to be further improved. Compliance screening here could mean a burn-in screen performed in elevated temperature by PCBA supplier because required in the contract. Failed units are repaired or scrapped. Discovery screening refers to screening which is targeted to search for areas with a potential for improvement in the manufacturing process. To achieve this, accelerated stress testing (AST) methods e.g. HASS are required. HASS also incorporates investigating and correcting the failures found, leading to improved reliability.

Regardless of being mainly used at different phases of the product lifecycle, highly accelerated life testing (HALT) and HASS are in close relationship to each other. Refer to Figure 10. HALT is mainly used in the product development and HASS in the product manufacturing. Generally, HALT can be successfully applied without the use of HASS, whereas HASS cannot be applied without HALT [7]. This fact poses a requirement to discuss the basics of the complete AST methodology. An overview of HALT and more detailed discussion of HASS is provided in further sections of this Chapter.

Higher stress levels usually mean higher fatigue for the non-defective units that leads to consumed life of a product. To control the risk of damaging good hardware in the screening process, proof of screen (POF) sub-process must be performed before production screening can take place. POF is discussed more in Section 6.4.3. It should be noted though, that all screening and even powering up a device takes away life from it. The amount of life removed is not relevant as long as confidence exists that enough life is still left [1] [2] [12].

The level at which stress screening should be performed for a system is ideally the lowest that is properly diagnosable. This usually means e.g. a single PCBA. The benefits of testing at the subassembly level compared to testing a complete system include the following: Test monitoring system is less complex, test chambers and equipment can be of a smaller scale, the failure analysis is easier as DUT (and test system) is less complex. System level screening

may still be appropriate, as it is the closest one can get to the actual product about to be shipped. This can provide unique discoveries in screening [1]. Testing level considerations are equally valid for HALT too, as stated in next Section.

6.2 Overview of HALT

A common approach to product development phase AST is HALT [2] [6] [10] [23]. Correct application of HALT or similar design ruggedization method will make the product very robust and enable the use of effective production stress screening by widening the gap between product strength and experienced stress distributions [1] [7]. Refer to Figure 3.

HALT is used to find and correct design errors and to gather data of the limit values of various stresses the product can withstand without damage [2] [6] [10]. As a result of this testing, operating and destruct limits of the product are obtained [6]. These are the essential input data needed to design a HASS. See Figure 11 for a visualization of the limits and relation to HASS. HALT should be started as early as possible in the product development cycle because design changes are more easily made. The correct time for HALT is usually when a unit with a full diagnostic capability and a reasonable representation of the final product is present (e.g. prototype of PCBA). The diagnostic capability allows for fault detection during testing. Later a system level HALT may be performed if considered beneficial. The system level test realization often becomes complex regarding logistics and fault finding. Still, it may be a useful level of testing, as the unit under test is closer to what will be shipped to the field [1].

The stress stimuli used in HALT are not required to be the same as those in the use environment of the product. Actually, the only requirement is that the stress should cause similar failure modes in the product as found in the field. The crossover effect [12] [18] may lead to a stress stimulus accelerating a certain failure mode very effectively in HALT, even though this stimulus may be different from the one causing a similar failure in the field. Refer to the example in Section 5.1.

The relevancy of HALT discoveries on a new design may be difficult to proof, as field data does not exist yet. It is concluded by several authors in the literature though that findings in HALT are usually relevant to field environment and the failure mode discovered in HALT will almost certainly cause unreliability issues if it is not fixed for production design [1] [2]

[10]. This is because of "unreliability amplification" achieved by AST [1]. The effect is shown in Figure 7. Higher stress has similar effect as lower product strength.

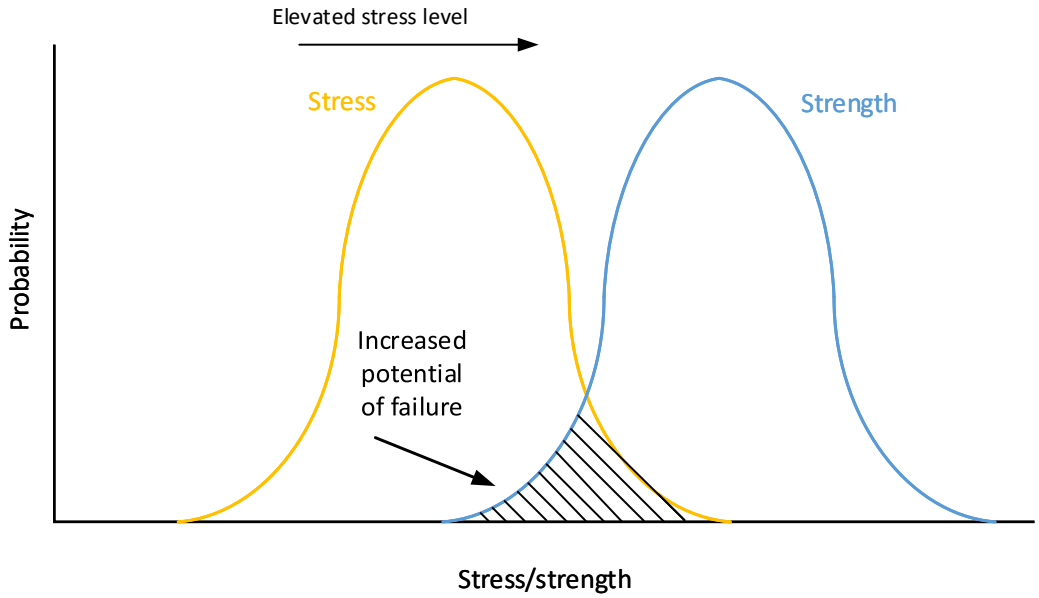

Figure 7. Elevated stress level has similar effect to reliability as does weakening of product strength [1] [6].

HALT can be visualized as a 3-phase closed loop process as in Figure 8. First, testing is planned. This includes test plan reviews with design and reliability departments. The specification of test facilities, software and people needed for testing is needed. Second, the test plan is executed and product limits are determined. The best approach is usually to start with individual stress stimuli and find the limits by stepping up the stress levels, starting from the most "gentle" stimulus in order not to break the sample too early. After that, combined stresses may be used in same step-up manner. The product will be stressed until it breaks. All faults discovered are documented and a quick fix is implemented when necessary and/or achievable to be able to continue increasing stress levels and discovering as many weak points as possible.

The loop is closed by the third phase, in which corrective actions to improve the design are planned and executed. This includes failure root cause analyses (FRCA) of the discovered failures and corrective actions (CA) of PCB layout, component or other relevant site to

remove the weaknesses. When entering a new round of HALT with new revision hardware, verification of the CA must be taken into account [1].

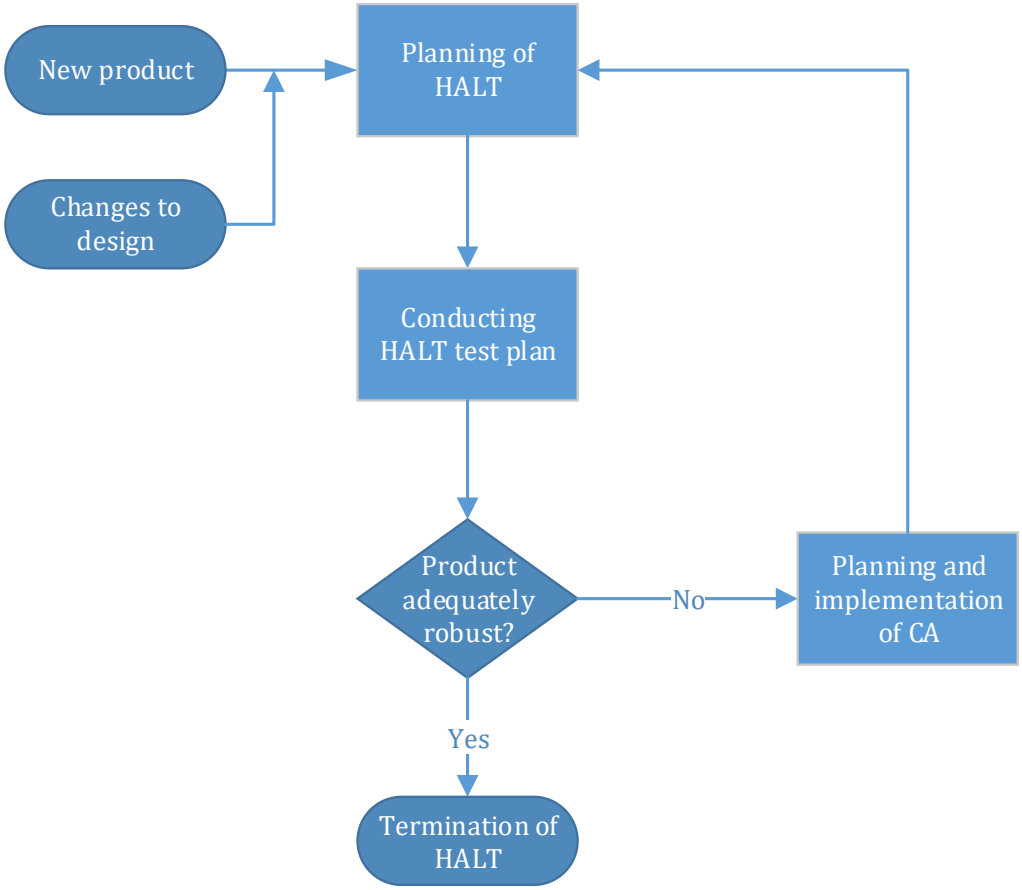

Figure 8. HALT process diagram [1].

The design HALT phase is finished when the deviation of tolerance of all the relevant stresses is at the required full life time (FLT) of the product [6]. Later in the product life cycle, a Re-HALT may be necessary to confirm the stress tolerance limits if significant changes are made to the design, components or production processes.

6.3 Structure of HASS

6.3.1 Overview of process

HASS consists of the following parts [2]:

1. Screening: product faults (including latent and patent) must be detected.
2. Failure analysis: FRCA must be completed on all findings.
3. Corrective action: faults must be corrected and the correction verified.
4. Database update: cases should be documented with care, so the knowledge gained can be used in the future.

Graphical presentation of the flow is in Figure 9 below.

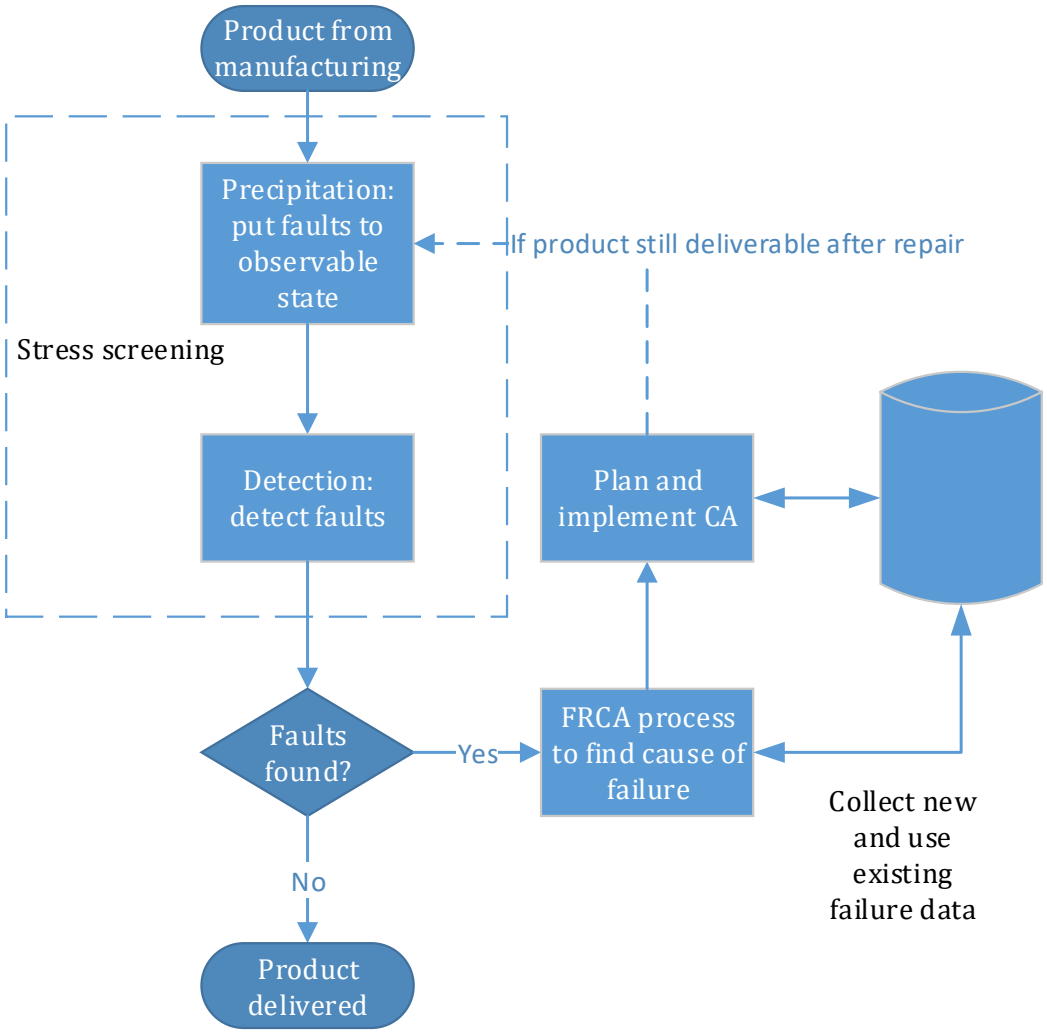

Figure 9. HASS process [1].

6.3.2 Screening

HASS screening part must 1. render the faulty sites observable and 2. detect the faults present in the DUT. This must be achieved without significant fatigue to healthy products. The demands shape the structure of HASS. Precipitating latent faults into patent, observable faults usually is achieved more quickly at higher levels of stress on the product. For this task, stress levels beyond product operational limits can be used. However, fault detection and diagnostic capability become restricted if the operational area of DUT is exceeded. The risk of precipitating and not detecting is present and as always with HASS, a quality proof of screen is required to verify the safety of testing [2].

6.3.3 Fault detection

Detecting faults requires tester equipment with capability of performing electrical measurements and issuing commands to the DUT. The tester must also simulate the use environment and interfaces for the DUT to such extent that correct operation during testing can be verified. On the DUT side, at least a testing mode in the software is probably required, maybe even a special test software. The test system software and hardware should allow for a fast assessment of all DUT functions and all circuit nodes that are accessible. All these requirements are to be met while the DUT is going through a stress profile.

Fault detection is one of the toughest challenges in the use of HASS and a critical part of screening. References [1] [2] [6] state that in many cases, a significant fraction (up to almost 100 %) of failures in electronic assemblies are intermittent. If such products were sequentially first stressed and then tested, a good chance exists that no faults would be detected. To overcome this issue, dynamic detection screening is suggested in which the testing cycles are run simultaneously with stressing the product. Vibration and especially combined vibration and temperature cycling are found to be effective stimuli during detection screens [2] [6]. A real-time monitoring of the measurements should be selected over sampling, to be able to detect intermittent faults with high frequency and low “duty-cycle” excited by vibration [1].

Another part of fault detection is the diagnostic coverage of the test system. It should be very high ranging in the area of 90…95 %. Hobbs [2] points at results from Proteus Corporation which suggest that fault coverage is often in the range of 28…45 % regardless

of estimation of "*90-95 %*" by case companies. If the test coverage is not adequate, HASS should not be applied at all, as it may turn out to be even harmful for reliability [12]. A case study on SW fault detection and test monitoring at Allied Telesis shows that HASS usually places requirements on the DUT SW too, which should allow for effective test cycle and self-diagnostics when screening [6]. A test mode may be required. However, the highest confidence on screening strength and relevancy are obviously achieved when using production SW. Thus, a balance between test capability and adequate correlation to the field SW should be the aim of design compromises.

Assuming an adequate test coverage, effective screening can be performed. In addition to "hard" failures (opens, shorts, total loss of signal etc.) prognostics or discriminators can be used to predict failures not yet become latent. This means observing an exceptional measurement of the product (such as an electrical signal, mechanical resonance, acoustic noise "signature" etc.) that is known to predict a certain failure. The application requires deep knowledge and experience of the certain failure mode but those can be gained during HALT. In a paper [24] prognostics were used successfully during proof of HASS and even as a substitute for HASS. In both applications, the DUT was still functional but a measurement revealed degradation in an indicator predicting a complete failure.

6.3.4 FRCA and CA

Once failures are observed, all findings should be investigated in adequate detail to find the root cause of the problem. The failure analysis is probably the most challenging part of HASS to accomplish. See more on failure analysis in Section 3.5. When the root cause has been determined, a corrective action (CA) can be taken. See more on CA in Section 4.2.

Although being not vital to successfully perform HASS, a database on HASS experiences should be maintained. It can provide a significant cost reduction over time in several ways. If the knowledge on HASS testing is only in the minds of individual key employees, major setbacks could be expected if those persons left the company. Good HASS data can greatly facilitate the screen configuration and verification for new designs, as often similar components and techniques are used. In addition, HASS database can help in making new designs more mature already at 1st revision. Past experiences and lessons learned can be used as reference to pick the robust design conventions and avoid repeating the same

mistakes. This can lead to huge profits if design rounds can be reduced and time to market accelerated [2].

6.4 Applying HASS

6.4.1 Development cycle

The characteristics of HASS mentioned in Chapter 2 lead to a three-phase development cycle of the screen [3]. The flow is in Figure 10. The phases 1 to 3 should be implemented when a new product is developed and brought to market.

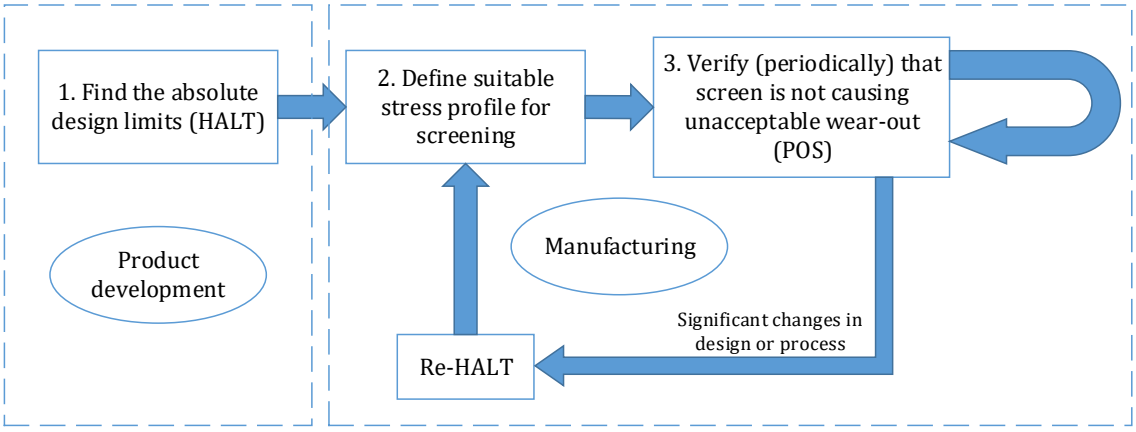

Figure 10. Development of HASS.

Phase 1 HALT:

HALT data on the strength limits of the product is needed as an initial input to HASS. See Section 6.2 and literature [1] [2] [3] [6] [10] [12] [24] for more detailed description of HALT.

Phase 2 HASS:

HASS should always be tailored to the particular product to be tested [4]. General screens may be either inefficient or unsafe or even both. See more on the stress profile configuration in Section 6.4.2.

Once the test specification is completed, reviewed and approved, the resulting test setup should be built and/or ordered and commissioned. Then, the proposed screen can be verified and tuned as necessary in proof of screen.

Phase 3 POS:

As stated in Chapter 2, HASS must not damage a good product that goes through screen and continues to delivery. This must be proven by the use of proof of screen (POS). Primary purpose of the sub-process is to ensure that no good (referring here to a flawless unit representing the designed reliability) products are damaged by screening. The effectiveness of the screen to find faults should also be verified.

POS should be conducted periodically even if there has been no major changes to the design. This is needed for controlling deviations in the testing equipment and distribution of product robustness. Please see Section 6.4.3 for a more detailed description of POS.

6.4.2 HASS profile configuration

Literature presents some guidelines to configure the correct HASS profile. However, there is no formula for calculating the correct stress levels and combinations. An effective and safe HASS requires also experimental feedback to verify the calculations. Figure 11 illustrates the relationship between HALT and HASS stress levels. It is not uncommon to employ stresses beyond the operating limits in both HALT and HASS. In HASS, these are used during the first part of the screen, precipitation [3] [6] [7].

Stress stimuli to be used in HASS are selected based on HALT results and experience. A wider range of stimuli and combinations of stimuli have often been used during HALT that is reasonable to implement in production screening. Production environment places time and cost constraints on any introduced testing, so compromises may be necessary between the extent of screening and time and materials consumed. Literature concludes that in many cases simultaneous temperature cycling and random vibration are very effective in both precipitating faults and making them detectable [2] [6].

One is usually required to gather the information available from the product in question and support it with data on other similar products if necessary. Then, a candidate HASS is defined. A perfect HASS cannot be designed at the office, instead it will be iterated experimentally. When the required stress stimuli are selected, specification of the test setup can be completed. This includes specifying the equipment such as test chambers and other requirements for the test site (compressed air, liquid nitrogen etc.) as well as product fixtures. Monitoring system is another part of test setup that needs to be specified according to the detection requirements in Section 6.3.

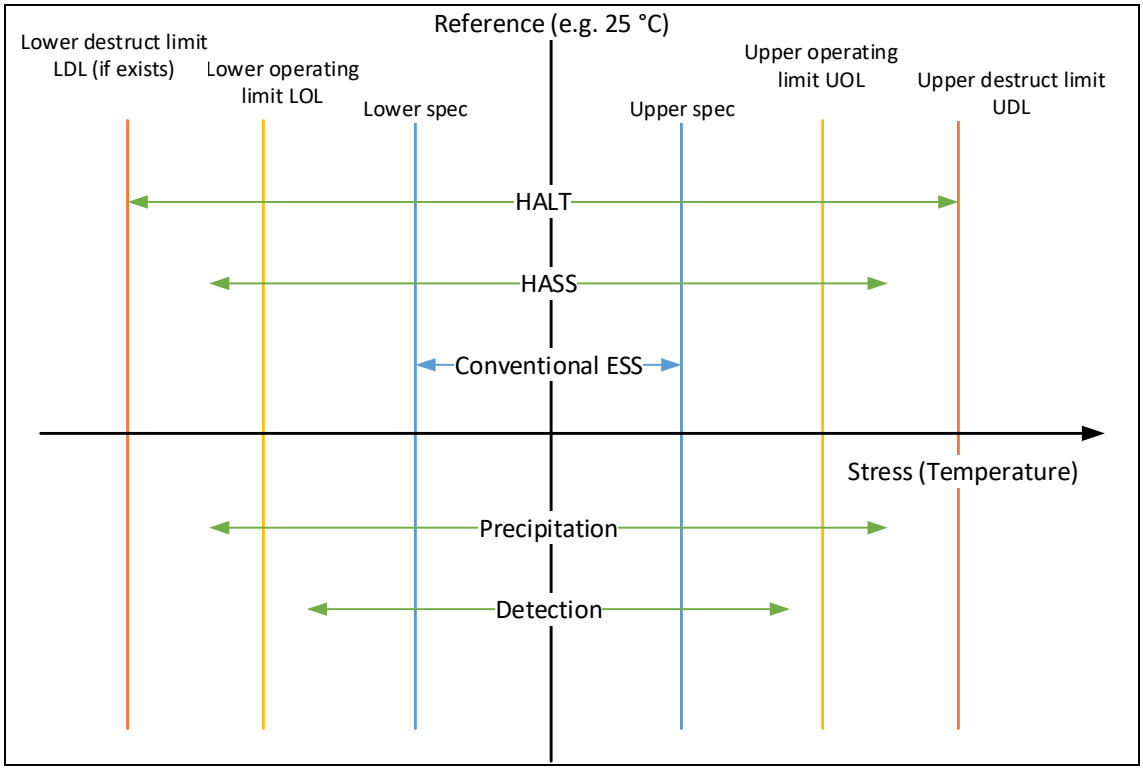

Figure 11. Example of temperature stress levels in conventional and AST processes. Upper side of horizontal axis compares HALT & HASS with a test-to-spec ESS method like burn-in. Lower side compares HASS precipitation and detection stress levels [2] [6] [12].

Figure 11 lower half shows the relations of precipitation and detection phase stress levels. In detection, the stress levels are lowered so that a non-defective product will function normally, even though the stress levels are over the product specification.

To provide some rule of thumb to start with, literature suggests to use temperature cycling range that is backed off 10…15 °C from the operating limits at both ends and vibration levels of half of the (upper) destruct limit max. for detection screen [6]. The vibration should be modulated so that the random vibration g_{RMS} level is swept from the lowest possible to the

½ of the DL continuously during temperature cycles. The purpose of vibration sweeping is to search the temperature-vibration plane to create the correct combination to make an intermittent fault observable. Vibration is the variable for the short-cycle sweeping, because temperature change is much slower to achieve. Figure 12 is below as an example to further clarify the search concept.

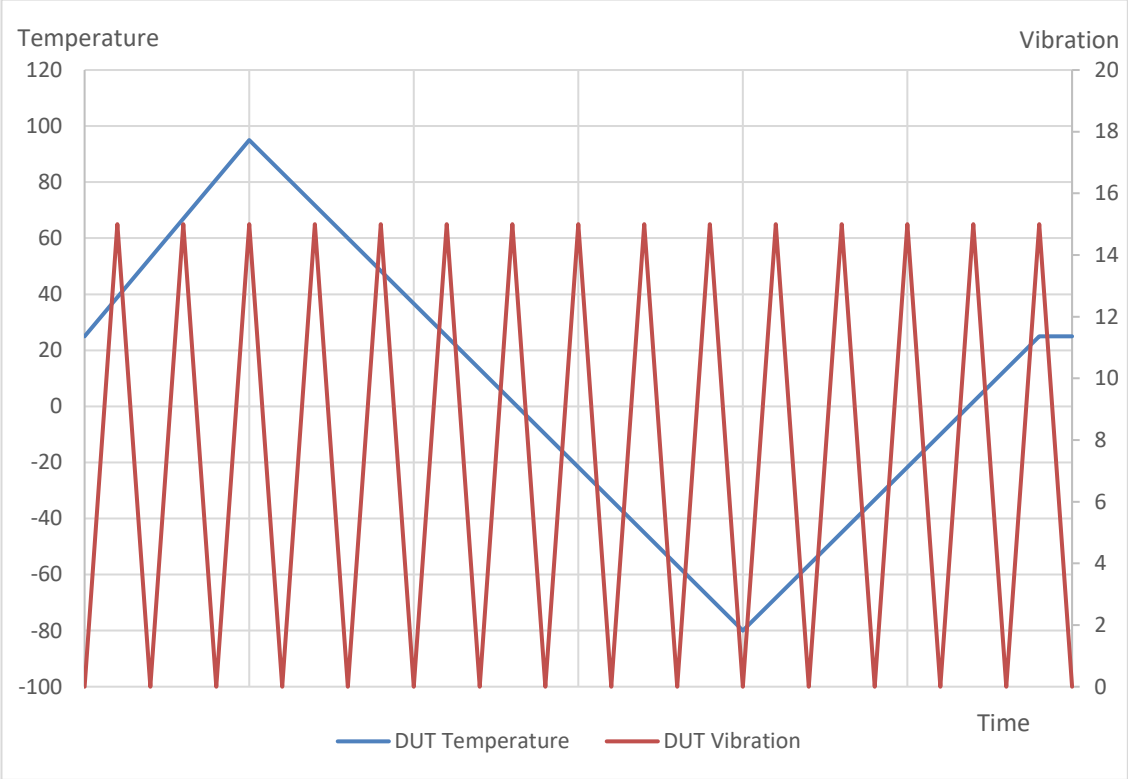

Figure 12. Example of detection screen profile with modulated vibration in arbitrary units [2].

6.4.3 Proof of screen

When a candidate HASS profile has been developed, it still needs to be verified. The aspects of interest are if the screen is able to find the weak products from the population and, even more important, if it is safe for good products. Proof of screen (POS) is used for verification. It must be performed for every position or slot in the fixture if multiple samples are to be screened simultaneously, as usually is the case in production environment screening (or at least the positions with measured highest and lowest stress levels on product).

A paper [25] states that successful HASS does not demand strictly uniform and repeatable screening for all products in different fixture positions or over time. Failure data from large sample lots run through screens with significant variation in the stress levels shows that variation neither compromises screening effectiveness nor safety. Careful POS is just needed to demonstrate this. This result is a relief to anyone implementing screening, because such a high control over the profile would be difficult, if not impossible, to achieve.

Concerning the safety of screening (SOS), the relevant question is if there is enough life left in the product after screening. As long as there is, the common question of how much life is consumed by screening is not relevant. The latter question is often a very hard one to answer as pointed out by Hobbs [2]. The SOS can be demonstrated by running the screen profile on the same samples multiple times and confirming that they are still functional. Different suggestions exist on how many cycles should be used, ranging from 10 to 50 [1] [2] [26]. If samples are run through 20 rounds of HASS and all remain operational, conclusion is that no more than 5 % of life is removed by HASS. This is usually acceptable. E.g. at Watlow, an industrial heater, sensor and controller company, HASS profile was run 30 times while monitoring the DUT to confirm the safety [6].

Effectiveness of screening may be more difficult to proof. A reference suggests using "seeded" samples that are units with intentionally created flaws to prove that screening precipitates and detects the faults [3]. This may seem to be a very tempting means to confirm the effectiveness. However, the experience of another author is, that seeded samples may lead to more questions than answers. This is because building samples that would break in the supposed manner may be a challenge [2].

6.4.4 Sampling and HASA

Stress screening can be performed for all the units manufactured (HASS) or sampling can be used (highly accelerated stress audit, HASA, or sample HASS). It is also possible to use a combination of these. E.g. when a new product production is being started, HASS may be applied for some time during the ramp-up to confirm that process quality is appropriate. Additionally, some design errors missed during the product development testing may be uncovered. When product failure rates are low, it is very unlikely to discover all problems

in HALT phase run with only a few samples. Because of this, 100 % HASS is recommended when production is being started for adequate amount of units to go through screening to build up knowledge [1]. When confidence is achieved on the quality of the new process and product, HASS may be reduced to HASA or even terminated. A similar process can be used any time when known changes are made to a product. 100 % HASS may then be used for the first batch/batches as a first article inspection (FAI) process. When it has been confirmed that quality is still high, screening may be reduced to sampling or terminated.

Considering a production product, the decision between HASS or HASA must be made by consideration of the project objectives. If HASS is used, no products will escape testing and quality improvement will certainly be possible. When using HASA, current quality is accepted, as part of products are delivered without screening. It provides possibility to detect changes in product or process that affects all or a large portion of products.

The cost of testing is greatly affected by the sampling level, as screening takes significant amount of time. A balance between the cost of testing and gained benefits must be the objective of the method of choice. Good results have been achieved with a relatively small sample size (< 6 %) when the manufacturing process is of high quality and the purpose of screening is mainly to catch deviations from the standard quality. To achieve a quality improvement however, 100 % HASS may be justified [2].

Statistical methods can be used to determine the sampling rates for HASA. These will not be discussed within the scope of this study, instead comprehensive literature on the application of the methods to stress screening can be found in references [1] [3] [6].

6.5 Objectives of stress screening

Stress screening could be seen as an insurance process to make sure that the product shipped actually is equally robust to the one that was developed using HALT. Screening is the ongoing process that monitors the complete manufacturing process for deviations. By screening at the factory, damage done by a process error or faulty component batch will be much less than if the fault discovery takes place in the field.

The objective of stress screening is to permit product reliability increase and lower the field failure rate by finding product units that do not represent the designed product, meaning they contain one or more weaknesses introduced in some point of the manufacturing chain. If such units were shipped to the field, early failures might occur. Reliability increase is only achieved through disciplined FRCA and CA processes that must be seen as integral parts of a stress screening program.

Stress screening must be economically optimized, meaning it is adjusted to an optimum between the cost related to screening and the reliability-growth-induced economic benefit gained from the process.

6.6 Economic considerations on stress screening

In this section the benefits and costs of performing AST are discussed. Due to the properties of HASS and the requirement of prior HALT, the complete AST program is considered when necessary. As with all business, running stress screening must add to a company's profit.

The implementation and use of AST tend to be expensive. Testing takes time in the product development and in production and requires working hours of designers and reliability experts, slowing time-to-market and creating labour cost. Should failing products be discovered, the analysis and correction of the problem may take even more time and effort from the reliability, quality, failure analysis and design departments. However, literature concludes that correctly and effectively implemented stress testing is certainly beneficial to both the manufacturer and the customer/end user of the product. This result is achieved when the cost of not testing is completely understood and calculated [1] [7] [10]. If AST is introduced as an alternative to existing reliability verification testing and production burn-in processes, the total time consumption will usually be lowered significantly. Various statements on reliability gains are found in literature, factors ranging from a telecommunications equipment company's 2…4 [8] to an accelerated stress testing consultant's 1000 [7].

It is claimed that HALT has the highest return of investment (ROI) of the programs in the AST field [2]. This seems to be a valid statement, considering the relative ease of even major design changes before production is started. HASS, however, has an important role in

realizing the reliability gains produced during product development AST process by confirming that the units delivered are equally robust to what was designed.

6.6.1 Benefits gained

Direct economic gains achieved by AST are reduced warranty and repair cases and the associated costs. In the worst case when a manufacturer has to replace faulty products already deployed in the field, these costs are often in the order of millions. Not as evident are the benefits resulting from the improved product reliability. It may help in market share growth by developing a reputation for reliability and lead to significant business growth.

Other benefits associated with the presence of AST equipment and experience are the ability to apply HASS in NDF troubleshooting discussed in Section 3.5 and the build-up of reliability know-how. The latter can and should be used in future product designs to reduce the time-to-market and design cost even further [1].

McLean [3] presented an interesting case study on the cost savings of introducing a HALT and HASS program to replace existing reliability program with reliability verification testing before the production start and a 100 % burn-in screening in production. He concluded a 87 % overall cost reduction with the proposed program due to reduced testing time per unit.

Calculations for HASS ROI values are rarely found in publications. A case study of application on power converters [6] estimated almost a 3:1 ROI ratio for the HASS part, when both HALT and HASS were implemented.

6.6.2 Associated costs

HASS process creates costs depending on the application. The total cost consists of planning the process, investment on testing and monitoring equipment, training of screening personnel, possibly increased production time consumption due to screening test (leading to lowered throughput or need for capacity increasing investments and also higher working hours) and consumables used by screening (liquid nitrogen, power, etc.). Also the sub-processes of failure analysis and corrective action (Chapter 4) may be counted in the cost of

HASS, even though these should be standard procedures regardless of if screening is performed.

The factors contributing to the total cost of HASS are presented in Table 3. The maturity of the product and the possible field fault data compared to the reliability objective set for the product greatly affect the extent and type of screening required and costs created. Screening performed at system level is usually the most expensive and complicated to implement, but when high reliability is required it may still be a good investment. Also the use environment of the product affects the screen profile and hence the cost of equipment and consumables [1].

Table 3. Factors affecting the cost of HASS.

Product property	Description	Effect
Reliability objective	Must be determined for a certain product. A fraction-failed criterion.	Test monitoring Test time consumption Sampling Level of testing (system – subsystem – component)
Use environment	Stress experienced by the product.	Test stimuli Stress levels
Maturity of design	How rugged the design is considered.	Test stimuli Stress levels Sampling
Current reliability	Compare to reliability objective.	Sampling Test stimuli Test or not test?

As frequently mentioned in this thesis, setting up a HASS requires data from HALT tests for the particular product. These are not considered further here, as the factors are not very different and the cost estimations can be derived from the information and references provided.

6.6.3 Optimization of screening

Optimizing a HASS process is a challenge and is only achieved through iterative development based on the feedback from the previous implementations. It is the means to minimize the cost of screening without compromising the benefits. It is often a good idea to start the screening with high sampling rates but when reliability goals are achieved, the sample size should be lowered to as low a level as possible. Refer to Table 3. Ultimately, it may be reasonable to terminate screening completely if field fault rate is very low.

The feedback can also be used to assess the stress profile and stimuli used in screening. It is usually best to focus the screening on the failure modes that are found in the field. If it is found from screening dropout data that some phase of screening profile is not effective, the profile should be changed to discontinue worthless testing. However, the purpose of screening is also to catch failures that are unexpected, so the profile should not be excessively “trimmed” [1].

7 CONCLUSION OF THEORETICAL STUDY

In Chapters 2 to 6 basic concepts and methods relevant to production stress screening were reviewed and explained. The effects of common stress stimuli on electronic products were studied in depth and a detailed discussion on the concept of HASS was presented. Remarkable reliability improvements can be achieved using HASS. It should not be treated as another new test phase but more like a new strategy of testing and improving. A clear reliability objective such as the examples in Table 4 should be defined for the product. Business case can then be calculated to decide whether HASS is suitable for the application.

HASS is a straightforward concept in theory, but application is not always as simple due to the physical and chemical processes involved. Mastering the approach based on physics of failure requires skilled experts and special equipment. Also prior HALT data on the product is important in reducing the complexity of implementation of HASS.

In Section 6.6 it was stated that stress screening creates significant costs and hence the first objective should be to evaluate and optimize the FRCA and CA processes for the returned material received before implementing any new screening. Field returns should be considered as being stress tested at the actual use environment making them valuable sources of information. If the pursued reliability improvement is not achieved via these actions and more precise monitoring over manufactured products is still required, stress screening may be a cost-effective means to proceed. The appropriate methods depending on the project objective are compiled in Table 4.

Test coverage of product under test is critical to applicability of HASS. If it is not high enough, stress screening should not be performed at all due to the risk of generating undetected damage. Thus, coverage analysis of the planned testing system should be the starting point of stress screening setup specification.

HASS enables the ongoing monitoring of product quality with various application options concerning sampling and the extent of testing, see Table 4. By these adjustments, HASS can be economically optimized for a particular use case. In addition to the obvious quality controlling aspect, it provides possibilities of continuous product improvement over a longer time span than HALT.

Obviously implementing HASS into production environment is not a task without challenge. Time consumption can be increased with several orders of magnitude if compared to basic functional test. In addition there are implementation costs from equipment and screen adjustment before it can be safely applied to production. Some changes at production sites may be required as screening equipment also takes up space. However, HASS is found to have good return of invest by companies that have published their results. This seems to be especially true if sample-based screening is used.

Table 4. Selecting correct processes to achieve a defined reliability and/or quality objective. The effects cumulate when moving down the rows.

Project objective	Applicable method(s)	Benefit	Cost effect	Implementation effects
Maintain current quality, improve product reliability.	Improved FRCA & CA	Product robustness increased over time based on field feedback.	Low	More resources required at RMA and design.
Maintain current quality, improve product reliability and production monitoring.	HASA	Feedback loop made quicker by testing before delivery.	Moderate. Adjustment between strength and cost possible by sampling principle.	Stress screening facilities required. Production line not altered as testing can be performed separately.
Improve product reliability and quality.	HASS or high-rate HASA	Extremely high production quality monitoring achieved and good representation of product population inspected.	High	Stress screening equipment introduced to production site/line. Possibly some existing testing phases replaced by stress screening.

8 CASE STUDY

8.1 Introduction

A case study to apply stress screening to an electrical system already in production was conducted with the partner company (later Manufacturer). The focus was on the methods to be used, implementation was out of scope. A mature product and production process were assumed; the important part of product life testing (HALT) to gather data to specify the screen was conducted earlier and so was out of the scope.

Specific details of the system under study cannot be published. The case study has been edited into a non-confidential form, aim being that the work still remains understandable.

8.2 Case data analysis

In this chapter the system under study and relevant data and research on it are presented.

8.2.1 System structure

System consists of printed circuit board assemblies (PCBAs), power supplies, battery, wire terminals, fuses, cables and mechanics. There is a base level specification and optional modules. The base version is considered here, optional modules are out of scope. Table 5 presents the key materials and their notation regarding this study. Refer also to Figure 1.

Only PCBA materials are considered in depth within this study. Power supply is left outside of the key materials due to lack of detailed field feedback and failure data.

Table 5. Key materials of base version.

Item #	Name	Description
1	System	Contains all other items.
2	PCBA1	Cross connection board.
3	PCBA2	Relay board.

The system is housed in a metal box in which the components are fixed in various ways. The PCBAs attach with plastic claws of the back cover on a mounting rail whereas other components are mounted with screw joints.

PCBAs 1 and 2 are interconnected by a ribbon cable. This and battery cabling are practically the only cable installations internal to the System. A large amount of cabling is brought into the System from other parts of higher level system during installation.

8.2.2 RMA results

Returned material analysis (RMA) reports were used as reference to find the fault type distribution of the products. A following simplified categorization was employed:

1. NDF, no defect found.
2. HW-failure, electrical or mechanical fault in a component or board.
3. HW-other, e.g. missing components or faulty assembly process at the factory or in the field.
4. SW & Configuration, missing/wrong software or configuration.
5. Not analyzed.

RMA of PCBA1

Fault distribution for PCBA1 is presented in Figure 13. Total of 108 boards were received.

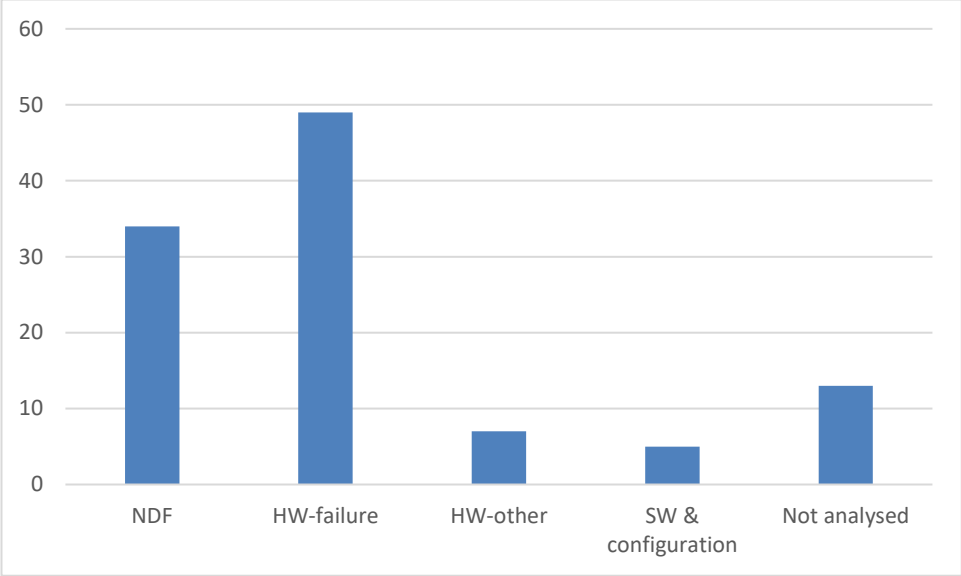

Figure 13. PCBA1 fault type distribution.

RMA of PCBA2

Fault distribution for PCBA2 is presented in Figure 14. Total of 20 boards were received.

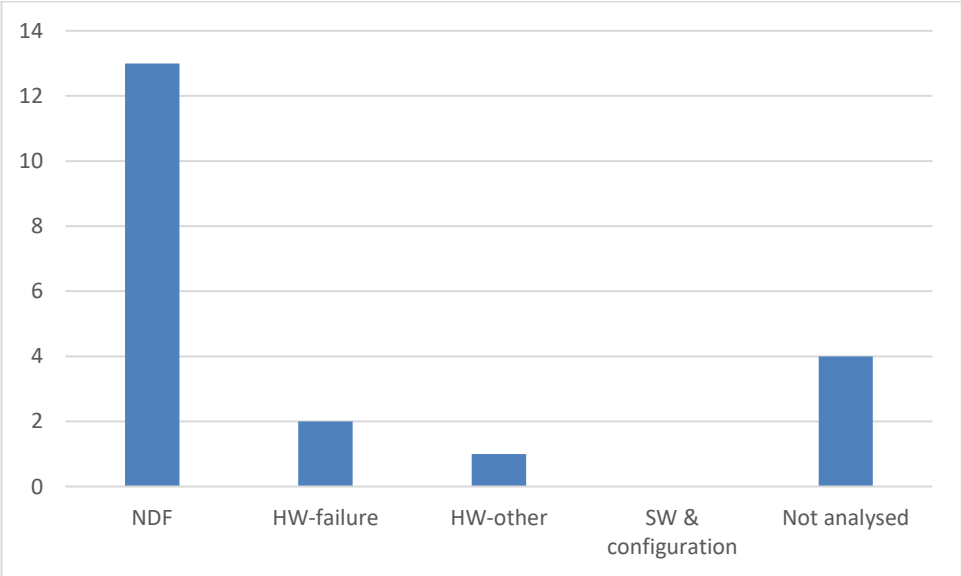

Figure 14. PCBA2 fault type distribution.

8.2.3 Failure modes in RMA

Based on the analysis results in Chapter 8.2.2 there are several failure modes. Adapted screening methods are required to screen out defective items before they are shipped out.

The failure mode data is extracted from the RMA reports. Figure 15 shows that the largest fraction of analyzed PCBA1 material is categorized as NDF. Identified failed units are mostly categorized as semiconductor device failure or assembly process failure. The latter includes e.g. missing connectors, faulty board assembly process and missing software. Also suspected field installation failure belongs to this category.

Note: The term *failure mode* is used here to describe the nature of the diagnosed failure. It must be noted, that failure mode in reliability engineering may often refer to the physical mechanism leading to a certain type of failure. These concepts are not the same, as the failure modes determined in this section are not accurate enough to reveal the failure mechanism in all cases.

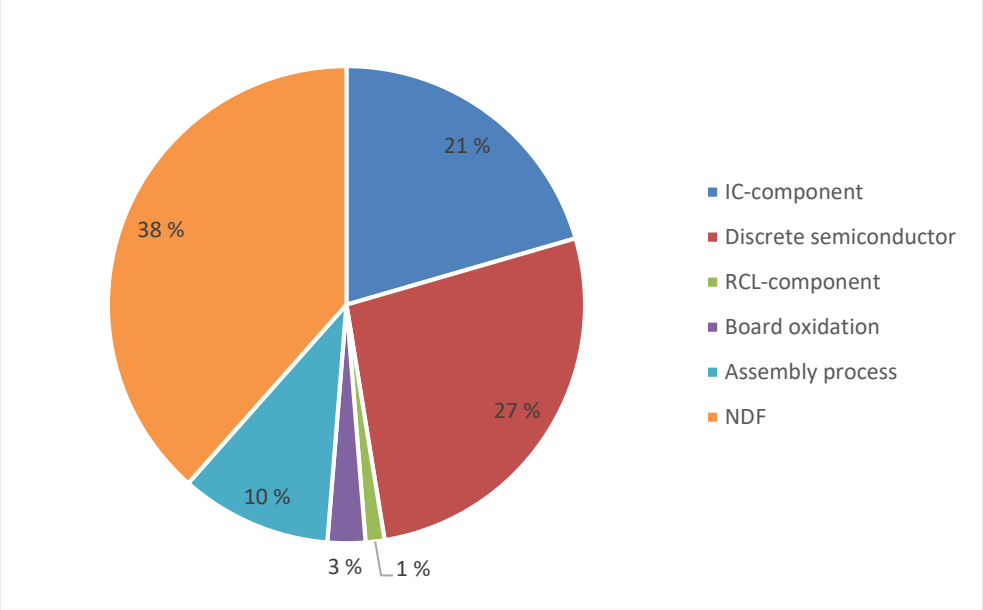

Figure 15. PCBA1 failure mode distribution.

Figure 16 shows that PCBA2 is very often categorized as NDF when returned. Findings concentrate on the power components (relays and diodes).

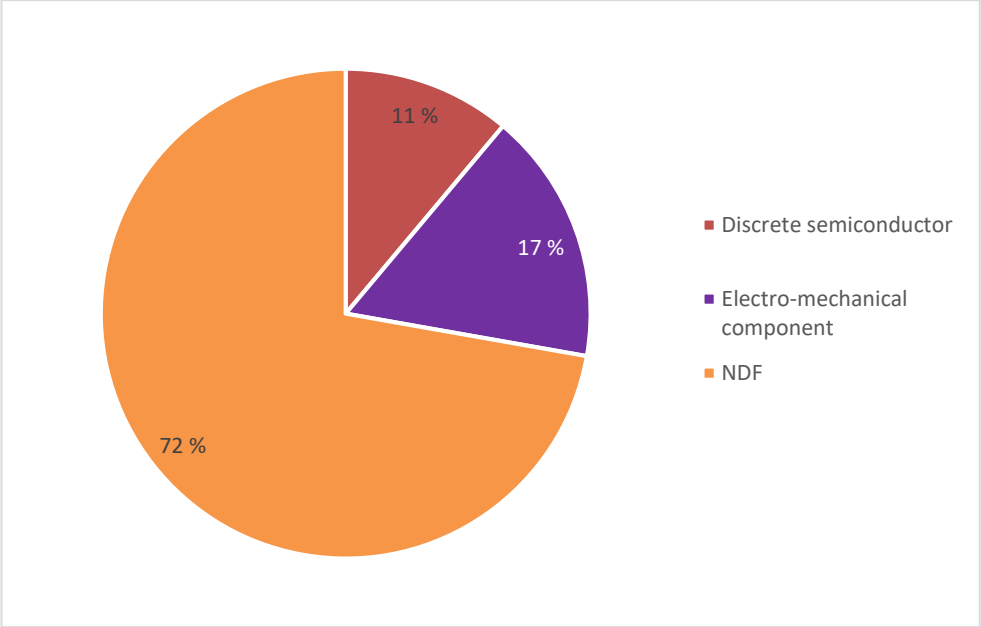

Figure 16. PCBA2 failure mode distribution.

Table 6 summarizes failure cases that have been found or suspected in the analyses.

Table 6. Failure cases based on analysis of RMA reports.

Failure ID	Component/part type affected	Failure description
1	Discrete bipolar transistor	always OFF state
2	Discrete MOSFET	burnt/case cracked
3	CMOS Shift register	short circuited
4	Microcontroller	SW not running or SW corrupted
5	Microcontroller	SW missing or wrong SW
6	SMD resistor	broken (open)
7	SMD transistor	pin not soldered properly
8	Various connectors	missing pins, covers or covers misaligned
9	Complete PCBA	corroded
10	PCB, several components	burned, possibly erroneous connection of 230 VAC

8.2.4 Failure root cause analyses (FRCA)

Studies and efforts conducted at the Manufacturer to detect causes of faults concerning the components of the System were reviewed and results summarized below. These consist of RMA deep analysis findings and other studies on the System related components.

FRCA of PCBA1

Table 7 contains only 1 report (#2) in which controlled environmental stresses (HALT chamber) are used to uncover faults in returned material. In this test no faults were discovered. The test sequence consisted of rapid thermal transitions (RTT) and combined test of RTT and random vibration. The stress levels in the test were

- - 20 °C…+85 °C (according to System specification)
- 0…5 G_{RMS}

Other studies are based on measurements in standard laboratory environment. From the stress testing point of view, other interesting studies are Ref 4, 5 and 6.

In **Ref 4** defective and non-defective boards are studied related to generation of a certain fault code. Failing boards are fixed to pass and non-failing boards are modified to fail in test. Thus, the mechanism behind the failure is uncovered.

In **Ref 5** one failure mode is solved (causing fault codes), and fix in software is proposed. In addition there are two HW-failures (microcontroller or memory related) where no specific failure mode is found and one unclear case (causing a fault code) which might be a problem in SW filtering.

In **Ref 6** root cause for products failing in production tester was found to be in the combination of HW and SW design. Certain shift registers had too tight a signal timing to work reliably.

Table 7. Summary of conducted PCBA1 failure and NDF analysis and results at the Manufacturer.

Ref #	Description	Conclusion	Note
1	PCBA1 4 pcs., Root cause analysis report	2 boards communication fault, 2 boards NDF.	Tested only in simulator using management software. No actual HW root causes found.
2	Stress Screening Test Report for returned material, PCBA1 NDF	No defects found.	Used combined temperature cycling and vibration.
3	PCBA1 (fault code), Root cause analysis report	Root cause (faulty transistor) for a single board with a specific fault code detected.	
4	PCBA1 fault code, Root cause analysis	Root cause for same fault code as Ref 3 was found by extensive study, timing of a self test.	4 factors found that affect the timing.
5	PCBA1 RMA Deep Analysis Report	4 issues studied, 1 root cause found.	
6	PCBA1 boards failing FCT tests	Boards are failing because of too tight timing of shift register operation.	

FRCA of PCBA2

Table 8. Summary of conducted PCBA2 failure and NDF analysis and results at the Manufacturer.

Ref #	Title	Conclusion	Note
7	PCBA2 root cause analysis	2 boards have same faulty semiconductor components. Possibly caused by installation work conducted with 24 V supply on. 1 NDF.	Result points at error in field installation work, not in manufacturing of product.

Table 8 shows that PCBA2 has proven to be quite a reliable product and only 1 root cause analysis has been conducted. In **Ref 7** two boards were found to be defective in similar way. These are stated to be possibly caused by installation work not performed according to instructions (24 V power on). 1 board was NDF.

8.2.5 HALT results

The PCBAs in the System have been through a highly accelerated life test (HALT) process in order to make the designs more robust and gather information on the tolerance of various stresses. This data of the actual product limits beyond specifications is essential to the development of manufacturing stress screening. Results of HALT are summarized in this chapter.

HALT of PCBA1

Table 9. PCBA1 HALT test reports used.

Ref #	Title
8	HALT Test Report
9	RE-HALT Test Report
10	RE-HALT Test Report 2
11	HALT Test Report variant 2
12	RE-HALT Test Report variant 2

PCBA1 has gone through several design rounds and also a few HALTs and Re-HALTs have been conducted. Different HALT rounds have used samples of different variants of the board (and different revisions of course), but the findings seem quite similar. See Table 10 for compilation of the limits found.

Ref 8 test was made for a relatively new product. A few problems were found, and those were fixed in later revisions. In this round very high and low temperature dwells (-90 °C & +180 °C) were used, and no permanent failures were detected. Sole vibration did not break the sample even at 50 G_{RMS}, but the combined test did loosen some capacitors.

Ref 9 was a fastHALT test that did not include all the Manufacturer's standard test steps. No critical issues were found. Temperature upper operating limit was found, but testing was not continued to destruction. Combined test loosened capacitors at a relatively high vibration level.

Ref 10 was a complete re-HALT to control product robustness after several years and design changes from the previous tests. Temperature destruction limits were again not found as the test was stopped at upper operating limit. The upper limit was caused by a serial communication failure, and the root cause for this was not found. Vibration test broke some larger components off the board (multifuse, SMD electrolyte capacitor). Combined test caused monitoring system to report "out of service" for a long time after power cycling, starting at the very first stress level. The suspected cause was DUT connector plugs.

Ref 11 was first HALT for variant 2 of the board. The full test set was conducted and very similar results obtained as from the previous test round. Temperature testing was stopped by the same fault code as the previous test, and testing was not continued to destruction. However, during the hot test, when the temperature was decreasing towards ambient another fault code became active. The root cause was not confirmed, but a connector or multifuse problem was suspected. The system did not recover by itself. Vibration and combination tests had virtually the same results as the previous test.

Ref 12 was a re-HALT for the variant 2. The results are quite similar to the previous test, except that no vibration destruction was achieved and a new problem at the cold thermal test was found. At -60 °C or below, the system started to activate several fault codes. A single fault code was considered to be the cause for the rest. The root cause for the fault code was determined to be the slow start-up of a crystal oscillator.

Table 10. PCBA1 HALT results.

		Chamber Set point level in Ref #				
Test ids	**Stress margins**	**8**	**9**	**10**	**11**	**12**
Cold thermal	Temperature LOL	<-100 °C	<-100 °C	< -100 °C	< -100 °C	-50 °C < -100 °C without power cuts
	Temperature LDL	<-100 °C	<-100 °C	< -100 °C	< -100 °C	< -100 °C
Hot thermal	Temperature UOL	50 °C	110 °C	110 °C	110 °C	110 °C
	Temperature UDL	>180 °C	>120 °C	> 120 °C	> 110 °C	> 150 °C

		Chamber Set point level in Ref #				
Test ids	**Stress margins**	**8**	**9**	**10**	**11**	**12**
Change of temperature	Thermal Transitions	From -90 °C to +50 °C	-	5 cycles from 100 °C to -90 °C	5 cycles of -90 °C to 100 °C	5 cycles from 100 °C to -40 °C
Vibration test	Vibration OL	>50 G_{RMS}	-	40 G_{RMS}	30 G_{RMS}	> 50 G_{RMS}
	Vibration DL	>50 G_{RMS}	-	40 G_{RMS}	30 G_{RMS}	> 50 G_{RMS}
Combined temperature and vibration	Combined OL	From -90 °C to +50 °C 0 G_{RMS}	From -90 °C to +100 °C >50 G_{RMS}	9 G_{RMS} 100 °C	> 45 G_{RMS} -90 °C to 100 °C	> 45 G_{RMS} - 40 °C to 100 °C
	Combined DL	From -90 °C to +50 °C 27 G_{RMS}	From -90 °C to +100 °C >50 G_{RMS}	36 G_{RMS}, from 100 °C to -90 °C	> 45 G_{RMS} -90 °C to 100 °C	> 45 G_{RMS} - 40 °C to 100 °C

HALT of PCBA2

Table 11. PCBA2 HALT test reports used.

Ref #	Title
13	HALT Test Report
14	RE-HALT Test Report

PCBA2 has been through HALT only 2 times. Tests have been conducted for a relatively new product. PCBA2 has not experienced as many design changes as PCBA1, but the data might still be slightly outdated. See Table 12 for compilation of the limits found.

Table 12. PCBA2 HALT results.

		Chamber Set point level in Ref #	
Test ids	**Stress margins**	**13**	**14**
Cold thermal	Temperature LOL	< -100 °C	<-100 °C
	Temperature LDL	< -100 °C	<-100 °C
Hot thermal	Temperature UOL	150 °C	120 °C
	Temperature UDL	> 160 °C	>170 °C
Change of temperature	Thermal Transitions	-90 °C - 140 °C	-
Vibration test	Vibration OL	0 G_{RMS} (25 G_{RMS})	-
	Vibration DL	40 G_{RMS}	-
Combined temperature and vibration	Combined OL	-90 °C - 140 °C, 9 G_{RMS} - 45 G_{RMS}	From -90 °C to +120 °C >50 G_{RMS}
	Combined DL	-90 °C - 140 °C, 9 G_{RMS} - 45 G_{RMS}	From -90 °C to +120 °C >50 G_{RMS}

Ref 13 reports the results of the first HALT, utilizing the full test set according to Manufacturer's specifications. The thermal upper operational limit was set by optocoupler leaking. The hot test was stopped by activation of voltage regulator protection circuit, destruction was not reached.

The product was found to be very vulnerable to vibration, as the relay contacts were bouncing already at the first level of vibration stressing causing various symptoms.

Destruction was reached when a relay contact was broken. Once all the relays were moved off the board, the board started to tolerate high levels of vibration. The particular relays causing problems were pinpointed.

Ref 14 was a fastHALT to verify that the issues found in previous revision were corrected. The optocoupler heat tolerance was found to have increased by 50 °C. However, the issue of vibration sensitive relays was still present.

Also new issues were found. In the hot test a 230 VDC output RMS level started to fall at 60 °C. The root cause of the failure was not found. Serial communication suffered from errors at the combined temperature and vibration test, the cause was a bad connector contact.

8.2.6 Current production testing

Current production testing activities of the System and its components are reviewed in this chapter. The testing of PCBAs is divided into two parts. For the bare PCB electrical testing for all nets is usually required. A more comprehensive testing is specified for the assembled PCBA.

The coverage analyses for discussed PCBAs are pending at the Manufacturer. These were not performed within the scope of this study. The coverage analysis for System is unavailable as well and was not performed within the scope of this study.

Production testing of PCBA1

Summary of PCBA1 testing related specification is in Table 13. As stated in **Ref 16**, electrical testing of bare PCB must be performed according to Manufacturer standard (**Ref 15**). This means a 100 % electrical test, no stress testing is specified.

Table 13. Manufacturing and testing specifications for PCBA1.

Ref #	Document	Description
15	PCB Manufacturing requirements	Manufacturer standard for bare PCB manufacturing
16	PCB specification	Product specification for bare PCB
17	Production Test Specification	Contains all testing for PCBA

PCBA testing is specified in **Ref 17**. For PCBA1 following are required:

- ICT, all possible components measured.
- AOI, after reflow and after wave soldering.
- FCT including
    - Hardware functionality.
    - Fuses.
    - Software programming and verification.
    - Interfaces and functions of board.
    - Serial communication interfaces.

No burn-in or stress screening is specified. 100 % of products are tested.

Time consumption:

- ICT < 60 s.
- AOI < 30 s.
- FCT < 180 s (without programming).

Production testing of PCBA2

Table 14. Manufacturing and testing specifications for PCBA2.

Ref #	Document	Description
18	PCB specification	Product specification for bare PCB
19	Production Test Specification	Contains all testing for PCBA

Summary of PCBA2 testing related specification is in Table 14. Electrical testing of bare PCB is required as stated by **Ref 18**. This is not further specified.

PCBA testing is specified in **Ref 19**. For PCBA2 following are required:

- ICT, all possible components measured.
- AOI, after reflow and after wave soldering.
- Visual test, connectors orientation and alignment.
- FCT including
    - Hardware functionality.
    - Fuses.
    - Interfaces and functions of board.

No burn-in or stress screening is specified. 100 % of products are tested.

Time consumption:

- ICT < 30 s.
- AOI < 30 s.
- Visual < 15 s.
- FCT < 45 s.

Production testing of System

Ref 20: Production Test Specification

Following tests for complete System are specified in **Ref 20**:

- Visual test with a checklist.
- FCT including
    - Voltage measurements of the system.

No burn-in or stress screening is specified. 100 % of products are tested.

Time consumption:

- Visual test < 60 s.
- FCT < 60 s.

8.3 Application of stress screening

In this chapter the application of highly accelerated stress screening (HASS) to the System is discussed based on Chapter 8.2 and the theoretical part of this thesis. See Chapter 6 for information on HASS.

8.3.1 Methods

The specific stress stimuli and other requirements to address a certain fault type are discussed in this section.

NDF

No-defect-found returns are the most challenging portion of all, because even the failure site is not known. There probably exists a division to actual faults within the system and "user-error" type of cases where the system is thought to be defective even though it performs as it should. The latter obviously is not an issue tackled by production screening.

Within this category, little numerical data exists. Instead, a few hypotheses based on experience are presented. Further investigation of field returns is required to gather data to prove the hypotheses.

Hypothesis 1: Faulty cabling

Cabling of the system is not tested for manufacturing errors. Loose crimping of connector pins may cause intermittent or permanent malfunctions of the system. This usually leads to activation of fault code(s) in the system. Fault codes may or may not point at the correct error site. Assumption is that often the PCBA with fault code is thought to be faulty when the error is actually located in the cabling.

Screening requirements for failure type:

1. System under test must contain all parts that are going to be shipped, including cables.
2. Good diagnostic coverage, all functions of the system testable and diagnosable.
3. Combined thermal cycling and low level of vibration to stress the system during test. Objective is to stimulate possible intermittent faults.
4. Deep understanding of the system is required from the operator to find the faulty site in case of failed test.

Hypothesis 2: Faulty PCBA

Some electronics faults are intermittent and may be observable only at certain environmental conditions. To be able to observe the fault, the conditions may have to be replicated or simulated. This may be achieved (or promoted) by stress screening. Only when the failure and root cause are found, appropriate stress screening (and corrective action) can be established.

One cause of PCBA faults that appear NDF is probably electro-static discharge (ESD). Stress screening methods at RMA may help locating also these hidden failures, even though corrective action may not be possible by product, design or component changes.

Screening requirements for failure type:

1. Correct stress specification according to failure mode.
2. Good diagnostic coverage, all functions of the board testable and diagnosable during stress screening.
3. Test setup with capability for all applicable functions.

Hypothesis 3: Misleading fault codes and signal LEDs

It is assumed that sometimes good boards are returned because a fault code or an error LED suggests a failure in that board. This information (or interpretation) is not always correct. Problems cannot be solved only by production screening, also further study of such cases is required to validate the hypothesis.

Semiconductor device faults

Semiconductor failures are a significant issue based on historical data in Chapter 88.2.3. In Table 6, IDs 1…4 represent this category. Part of the deep analyses conclude a semiconductor failure as well. It is likely that some of these could be detected by screening before shipping the products. These also may be caused by ESD event in some phase of product life cycle, as discussed in the NDF part of this section.

Possibly some of the faults in this category are already patent faults at the factory meaning that no special arrangements are needed to make the faults detectable. Thus, no stress screening is needed for these cases. Instead, a final functional screening test with good diagnostic coverage should be implemented for the boards.

The test setup should be a system simulator, with cabling and loads at the interfaces as close to field environment as reasonable.

Screening requirements for failure type:

1. Good diagnostic coverage, all functions of the board testable and diagnosable.
2. Test setup with capability for all system functions.

The rest of the faults are latent, meaning they are undetectable at normal factory or laboratory environment at the time of manufacturing. These faults may be internal to semiconductor components or they may be assembly quality issues e.g. poor solder joints.

Finding these defective but still operational units requires transforming the latent faults to patent, making them detectable by functional or in-circuit testing (ICT). If the product is not screened out at the factory, the transformation process happens by the effect of environmental stresses in the field, leading to an early failure case. By stimulating the failure mechanism in question using artificial stresses, the transform process may be accelerated to completion at the factory.

Challenge in determining screening methods is that very little actual root cause data is available on the products. Without this information, only assumptions can be made on the most efficient stress methods to precipitate semiconductor latent faults that are undetectable.

Screening requirements for failure type:

1. Correct stress specification according to failure mode.
2. Good diagnostic coverage, all functions of the board testable and diagnosable *during* stress screening.
3. Test setup with capability for all applicable functions.

The 3rd subtype of semiconductor issues are design-margin-related problems. A good example would be the timing of a logic IC, which generally is variable with temperature and supply voltage. This type of problems should be eliminated during HALT tests at the product development phase. It has happened though that design margins have been small enough for a component supplier change or a different component batch to start causing serious issues.

Screening requirements for failure type:

1. Good diagnostic coverage, all functions of the board testable and diagnosable.
2. Test setup with capability for all system functions. Special arrangements to modify the logic supply voltages on board.
3. HASS chamber with capability of fast thermal transitions.

Passive component faults

Only 1 RMA return is recorded where an SMD resistor was broken (PCBA1). Based on the data, passive components do not seem to be a major problem. Still, it may be beneficial to manufacturing quality to use stress screening to passives based on the experience. The issues and methods are quite similar to semiconductors even though the devices are simpler. One particular concern is the quality variations of electrolytic capacitors that may cause large temperature dependencies of capacitance.

Passive components from suppliers are assembled to PCBs, so there may be craftmanship quality issues both in components and the assembly process. These may be latent or patent.

Screening requirements for failure type:

1. Correct stress specification according to failure mode.
2. All nets on board measurable multiple times (continuously) with a short cycle by automated tester *during* stressing. Capability to measure component values.
3. HASS chamber with capability of fast thermal transitions and repetitive-shock vibration.
4. Test setup with capability to electrically load the board.

PCB faults

RMA reports do not contain any printed circuit board (PCB) related faults. In first HALT of PCBA1 (Table 9, Ref 8) an oscillator signal interference was assumed to be possibly caused by a stretch between component pad and via. It seems that PCB faults are not a major concern, however.

PCBs are generally sensitive to temperature and vibration stresses and combinations of these. A stress screen using such stimuli may be effective in discovering intermittent faults or weak craftmanship.

Screening requirements for failure type:

1. All nets on board measurable multiple times (continuously) with a short cycle by automated tester *during* stressing.
2. HASS chamber with capability of fast thermal transitions and repetitive-shock vibration.

Assembly process faults

In the PCBA1 RMA data there were several process related faults. These were mainly missing or misaligned connectors and missing or wrong software. Also an insufficient solder joint was found. PCBA2 data did not contain faults of this type. System level testing also uncovers some cabling installation errors.
These were all patent faults, meaning that no special arrangements are needed to make the faults detectable. Thus, no stress screening is needed for these cases. Instead, a final functional screening test with good diagnostic coverage should be implemented for the boards.
The test setup should be a fully functional simulator, with cabling as close to field environment as possible. The test operator must connect the cables to the DUT. In this process the correct installation of connectors is verified.
Screening requirements for failure type:

1. Good diagnostic coverage, all functions of the board testable and diagnosable. Software version checked.
2. Test setup with capability for all system functions.
3. Similar tester cabling to field environment or AOI if adequate to detect connector issues.

Installation faults

Field installation errors are suspected to be the cause of single PCBA1 and PCBA2 returns. These failures are created after factory, so production stress screening cannot be applied.

Conclusion of methods

Table 15. Summary of screening methods.

Fault type	Subtype	HASS required	Testing level and type required	Test setup special requirements	Notes
NDF	Cabling	Yes	System Functional test	Capability to do HASS for large DUT.	Whole delivery must be tested.
	PCBA	Yes	Board Functional test, ICT		
Semi-conductor	-	Yes	Board Functional test	Capability to alter board logic voltages.	Some faults may be detectable without HASS.
Passive	-	Yes	Board ICT		
PCB	-	Yes	Component/board ICT		
Assembly	-	No	Board Functional test, AOI		Assembly of connectors must be verified by optical inspection or by connecting test cables.

Table 15 suggests that most of the fault types can be screened at the board level. Only 1 type is considered to require system level testing with the complete System under test.

A challenge in determining an optimized set of screening stresses is the incomplete failure root cause information available, discussed in Sections 8.2.3 and 8.2.4. In addition, RMA data does not reveal certain problem components or failure modes, as products are quite robust. Thus, only a stress screen based on literature and experience can be proposed.

Based on the requirements, 2 different level screening specifications are compiled in Table 16. A 2 phase screen is proposed for PCBA testing and single phase screen for system level testing. Test configurations are based on best practices from literature on similar products.

Table 16. Board and system level screening stress specification.

DUT	HASS specification	Test setup & monitoring	Notes
PCBA *(PCBA1, PCBA2)*	1. Precipitation: Rapid thermal cycling and repetitive shock vibration combined. Power cycling of board. 2. Detection: Rapid thermal cycling and low level vibration combined. Voltage margining and power cycling on board.	1. Precipitation: No monitoring. 2. Detection: Functional testing of board, all functions.	Electromechanical devices may be very sensitive to relatively low vibration levels (PCBA2 relays, see Chapter 8.2.5). If device cannot function properly under vibration, the test may be unapplicable.
System	1. Detection: Vibration and power cycling of system.	1. Detection: Functional testing of system, all functions.	Unable to apply HASS method. A stress screen proposed for discussion.

The purpose of precipitation screen is to transform possible latent defects into observable faults. The proposed combination of stresses in Table 16 is generally thought to be effective for a broad range of failure modes on PCBAs. The complete monitoring of DUT is not possible during the precipitation screen as stresses are beyond operational limits. The purpose of power cycling is to speed up the temperature ramping and to stress high current density sites.

The purpose of detection screen is to find the often intermittent faults precipitated or already present. This is achieved by a combination of selected stresses and continuous monitoring. Purpose of stresses:

- Temperature cycling and modulated vibration are used to "search" through the T-V plane for intermittents.
- Voltage margining is used to uncover marginal components.
- Power cycling mainly to enable all diagnostic functions to be executed.

8.3.2 Stress levels

Initial stress levels for HASS must be determined based on the product limits found in HALT, see Chapter 8.2.5. For system level test such information does not exist, so an educated guess must be made. HASS is always an iterative process that is tuned to perfection over time.

Stress levels must always be tested for safety and effectiveness using Proof of Screen, see Chapter 8.3.5.

PCBA1 stress levels

Table 17. PCBA1 stress levels for all stresses during screening.

Screening phase	Stress type	Level/Rate	Duration
Precipitation	Rapid thermal cycling	-100…+130 °C > 60 °C/min	2 cycles.
	Repetitive-shock vibration with 6 degree of freedom	½ of DL with the equipment used.	
	Power cycling	ON when heat ramp up, OFF when heat ramp down. Cycling during temperature dwells.	
Detection	Slow thermal cycling	-80…95 °C	1 cycle.
	Repetitive-shock vibration with 6 degree of freedom	0…½ of DL with the equipment used. Modulated.	Over whole test time.
	Power cycling	ON for sufficient time to perform voltage margining and diagnostics.	As many cycles as possible during the thermal transient cycle (=test duration).
	Logic voltage margining	3.0…3.6 V	1 cycle / power cycle.

PCBA2 stress levels

Based on HALT results, a complete HASS cannot be applied to PCBA2 due to vibration sensitive relays. Instead, a limited HASS is proposed. Temperature cycling is also abandoned, as it may not be cost effective without vibration.

Table 18. PCBA2 stress levels for all stresses during screening.

Screening phase	Stress type	Level/Rate	Duration
Detection	Power cycling	ON for sufficient time to perform voltage margining and diagnostics.	2 cycles.
	Logic voltage margining	3.0…3.6 V	1 cycle / power cycle.

System stress levels

System is a large and heavy unit with no applicable robustness data available. Actual HASS cannot therefore be applied. Stress screening may be useful though, but screen development will require more experimental work than with PCBAs. In Table 19, a mild screen is proposed to start experimenting with.

Table 19. System stress levels for all stresses during screening.

Screening phase	Stress type	Level/Rate	Duration
Detection	Repetitive-shock vibration	0…2 Grms. Modulated.	5 cycles = 10 min
	Power cycling	ON for sufficient time to perform diagnostics.	2 cycles or more if diagnostics allow.

8.3.3 Samples tested

Table 20. Factors affecting the determination of HASS sample rate.

Process variants	Screen coverage (units tested)	Cost of testing	Effect on manufacturing quality
HASS	100 %	Maximum	Good possibilities of improvement.
HASA	< 100 %	Lower than HASS, relative to sample rate.	Maintain the current level. Possibility to quality gains, but not guaranteed.

Table 20 shows that decision between HASS or sample HASS (= Highly accelerated stress audit, HASA) must be made by consideration of the project objectives. See more on the sampling considerations in Section 6.4.4.

8.3.4 Results

Initial HASS specifications are presented. Profiles must be proofed and tuned experimentally using appropriate procedures. More information on profile proofing can be found in Section 8.3.5.

Common challenge to the screening of all types is the test system ability to detect faults. In all cases, full diagnostics should be examined while the DUT is going through a (detection) stress profile. More on setup specification and fault coverage requirements in Section 8.3.5. An ICT test required for passive components in Section 8.3.1 cannot be run during vibration, so also these faults should be detectable by the tester system.

For system level HASS cannot be applied with the information currently available. Instead, a stress screening profile proposal is presented to allow for discussion.

PCBA1 HASS profile

For PCBA1 2-phase screen is developed to gain the full potential of HASS. The profile is presented below. For more information on the levels, refer to Section 8.3.2.

Designed precipitation screen is in Figure 17. DUT powering state is graphed as a dimensionless ON-OFF square wave, HIGH state = DUT powered and LOW state = DUT unpowered. Following specification is in Table 21.

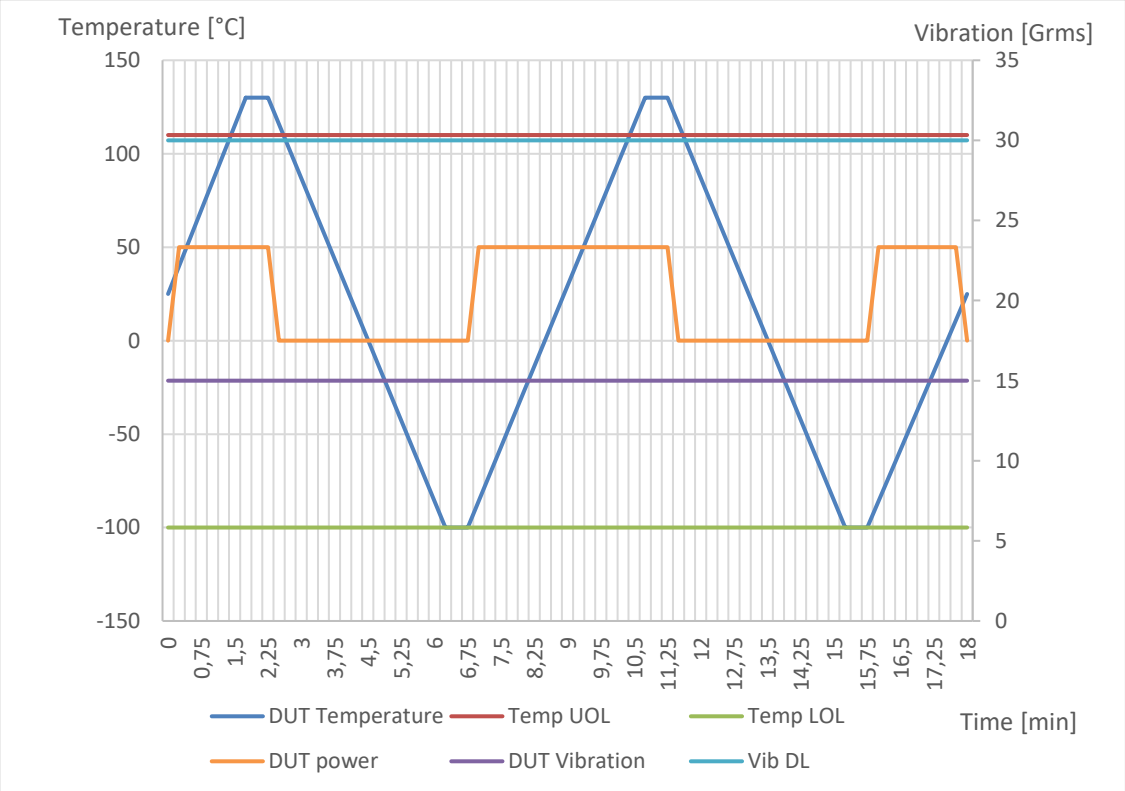

Figure 17. PCBA1 precipitation screen profile.

Table 21. PCBA1 precipitation screen specification.

Specification	Value	Note
Temperature cycles	2 complete	Test starting and ending at room temperature.
Temperature ramp	> 60 °C/min	Time consumption can be lowered with higher ramp. Use as high ramp as equipment allows.
Temperature dwell	30 sec	
Vibration	constant high-level (½ DL)	
Power cycling	ON when temperature ramping up OFF when temperature ramping down	
Time consumption	18 min	

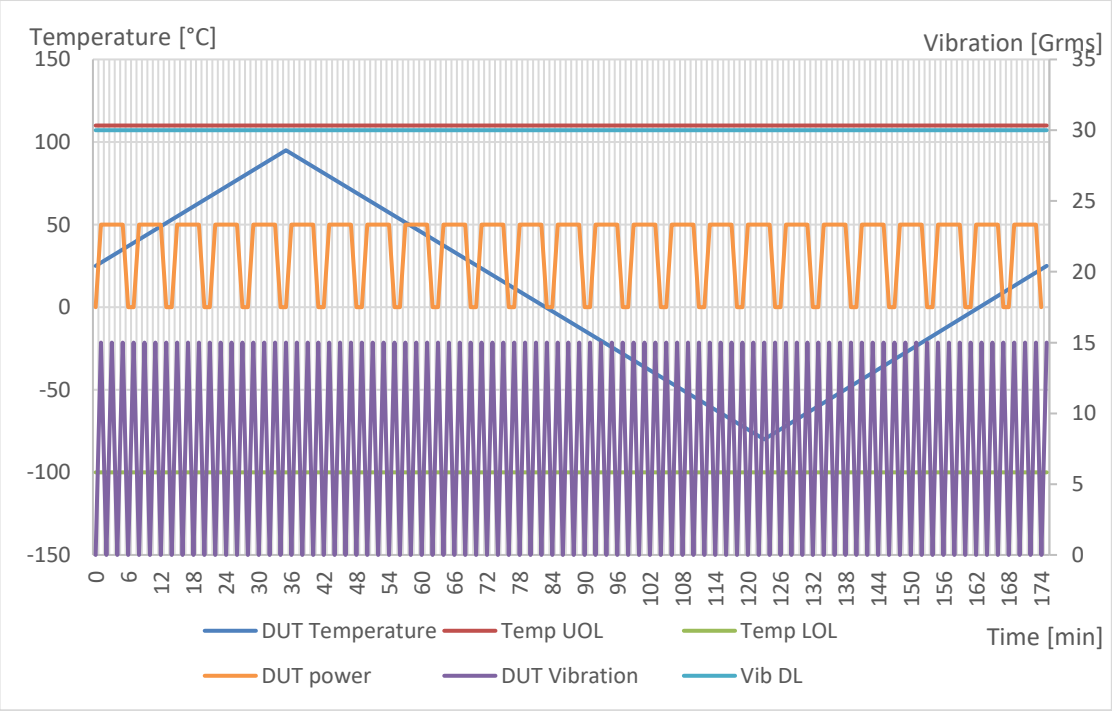

Figure 18. PCBA1 detection screen profile.

Table 22. PCBA1 detection screen specification.

Specification	Value	Note
Temperature cycles	1 complete	Test starting and ending at room temperature.
Temperature ramp	2 °C/min	Slow ramp to allow diagnostics.
Temperature dwell	0 min	
Vibration	Modulated, from 0…15 Grms with period of 2 min. Saw modulating waveform.	Lowest vibration used that is allowed by the equipment.
Power cycling	Continuous cycling, ON time adequate to execute diagnostics with voltage margining.	
Voltage margining	3.0, 3.3, 3.6 V	3 levels on every power cycle, diagnostics run with each.
Time consumption	175 min	

Designed detection screen is in Figure 18. DUT powering state is graphed as a dimensionless ON-OFF square wave, HIGH state = DUT powered and LOW state = DUT unpowered. Logic voltage margining should be performed on every power cycle with nominal-min-max values. Following specification is in Table 22.

PCBA2 HASS profile

For PCBA2 1-phase screen is developed given the constraints in vibration tolerance. The profile is presented below. For more information on the levels, refer to Section 8.3.2.

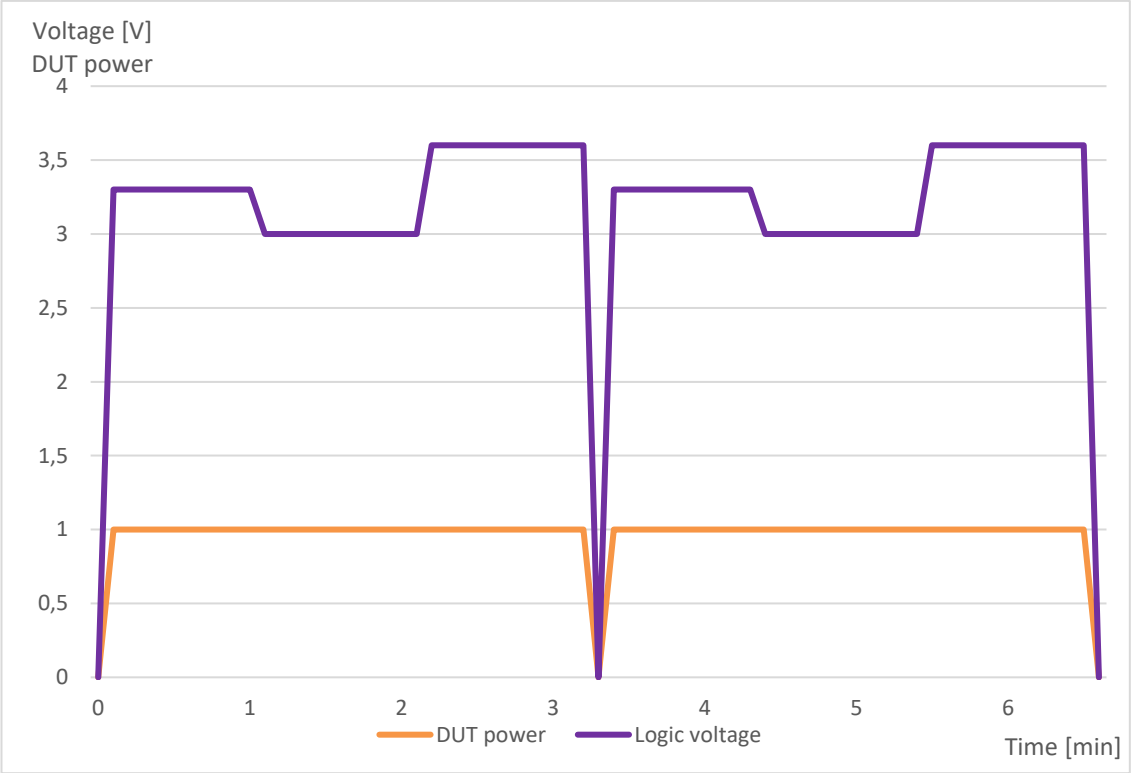

Figure 19. PCBA2 detection screen profile.

Designed detection screen is in Figure 19. DUT powering state is graphed as a dimensionless ON-OFF square wave, HIGH state = DUT powered and LOW state = DUT unpowered. Following specification is in Table 23.

Table 23. PCBA2 detection screen specification.

Specification	Value	Note
Power cycling	Continuous cycling, ON time adequate to execute diagnostics with voltage margining.	
Voltage margining	3.0, 3.3, 3.6 V	3 levels on every power cycle, diagnostics run with each.
Time consumption	6,6 min	

System screening profile

For System level a 1-phase screen is developed, as the principal objective is to screen for cabling issues. It is possible that combined temperature cycling would be even more effective. As there is no HALT data available on the System, the screen profile is highly experimental and will need feedback from conducted tests. The profile is presented below. For more information on the levels, refer to Section 8.3.20.

Designed detection screen is in Figure 20. Following specification is in Table 24.

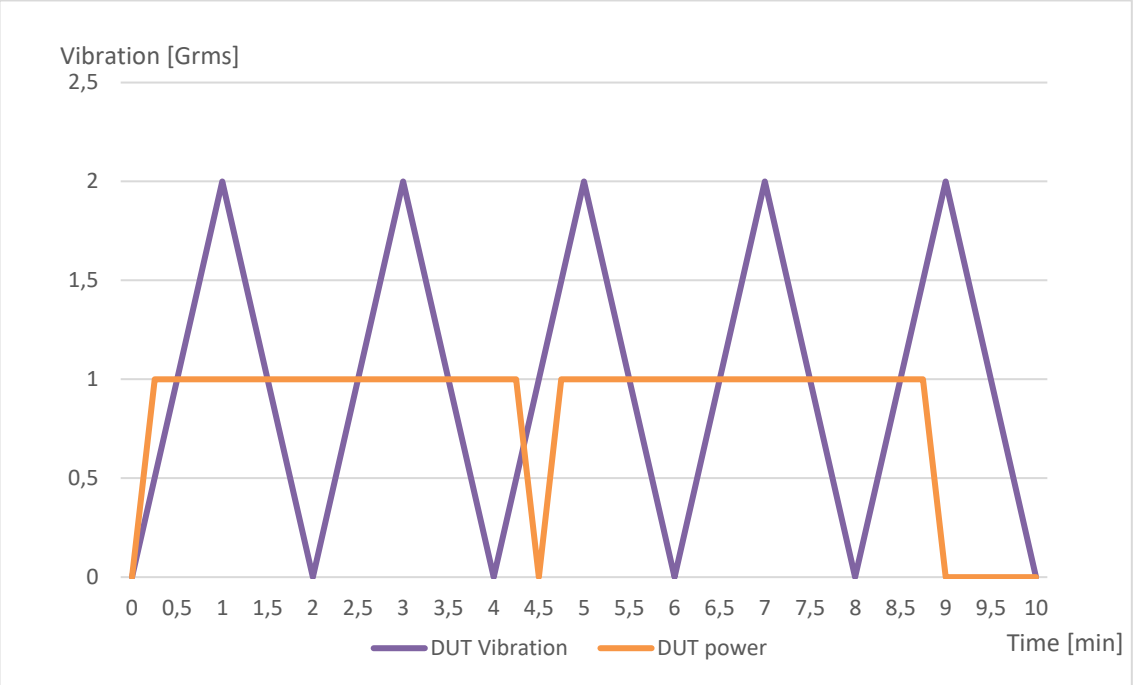

Figure 20. System level detection screen profile.

Table 24. System level detection screen specification.

Specification	Value	Note
Vibration	Modulated, from 0…2 Grms with period of 2 min. Saw modulating waveform.	Lowest vibration used that is allowed by the equipment.
Power cycling	Continuous cycling, ON time adequate to execute diagnostics.	
Time consumption	10 min	

Comparison of current and proposed testing

Illustrative comparisons for current and proposed production testing activities are provided below in Table 25 (for PCBA level) and Table 26 (system level). These should not be taken as accurate values, as HASS profiles are specified without knowledge of details of testing system. Test chamber and diagnostic system properties have major effect on duration of testing.

Table 25. Comparison of PCBA production testing activities.

PCBA production testing process	Duration	Coverage	Potential benefits
Current (Section 8.2.6)	< 3 min + setup time	Good (analyses pending)	N/A
Proposed	> 3 hours + setup time at the highest. Depending on product.	Extended. Depending on product.	Detection of faulty units not currently observable. Possibility to improve reliability by fixing issues found.

Table 26. Comparison of System level production testing activities.

System production testing process	Duration	Coverage	Potential benefits
Current (Section 08.2.6)	< 2 min + setup time	Basic functions tested.	N/A
Proposed	10 min + setup time.	Potential of extension.	Detection of faulty units not currently observable. Possibility to improve reliability by fixing issues found.

Especially for PCBAs, study is needed if the current production testing outlined in Section 8.2.6 can be replaced by stress testing, at least to some extent. Coverage analyses for current testing and planned stress screening are required for decision.

8.3.5 Next steps

Topics in this chapter are not discussed within the scope of this study. However, short discussion of the logical next steps is presented to further clarify the big picture.

Test setup specification

Following must be noted when specifying the setup and equipment adequate to perform HASS:

1. Amount of products to be screened and consequent space and equipment requirements at manufacturing plants.
    a. 100 % or sample HASS?
    b. What is the throughput requirement at PCBA supplier (PCBAs) and System assembly plant? How many samples max needed to be screened simultaneously?
    c. Is there sufficient real estate for required equipment at the locations? What actions needed?
    d. How and where is the failure analysis performed, is the required competence and capacity available?
2. Specification of tester equipment.

   a. For PCBAs, use environment may be simulated by production tester, at least to some extent. Different fixturing and connections are required though, as test points and bed-of-nails fixturing are assumed unusable during vibration.
   b. For System, can the current production tester do or is a more complete simulator needed to run the system?
3. Fault detection capability is critical issue. With insufficient detection, stress screening may lead to disastrous reliability drops.
   a. Special tester software and/or special board software needed to be able to efficiently and quickly monitor all possible nets on PCBA under test. Test coverage must be analyzed in detail as detection of precipitated faults is absolutely vital.
   b. Test coverage of System level must be analyzed and evaluated. Possibly more comprehensive testing cycle and/or setup must be developed.

Business case evaluation

When the test setup specification is ready, the cost of testing can be calculated. The gained benefit is more difficult to quantify to make a business case. The ongoing cost of testing may be relatively high compared to the existing, as can be seen in Section 8.3.4. The decision on implementing the screen must be based on business case calculation taking into account the actual cost of testing and especially the potential costs of *not testing*. Field return rates and associated costs should be considered, as these could be significantly lowered by enhanced screening.

Optimized HASS implementation requires re-evaluation of the complete testing strategy of the products in question. All levels of current testing and achieved coverage should be analyzed to avoid performing "double" testing at different production phases. Potentially some of the existing tests can be replaced by stress screening at the end of the process. Still, cost created by a faulty product is the lowest when it is caught as early as possible.

Screen piloting and tuning

If screening is implemented, the designed profiles must be verified and adjusted by proof of screen (POS). Please see more on POS in Chapter 6.4.3. By these actions it can be verified that screening does not damage good units.

Note: Vibration adjustment for screening will require comprehensive HALT-type verification testing, because DUT amplitude spectral density properties are not documented in prior HALT reports. This means that no information on actual DUT vibration accelerations is available, so the results cannot be used as proof of safety with any other test setup or fixture. The documented values are vibration table setpoints that do not represent any meaningful absolute values of DUT levels.

8.4 Conclusion of case study

A case system was studied to demonstrate the HASS process development in practice. Existing documents were consulted to find the current state of the reliability of the system. The failed unit analysis reports were examined closely to gather all available information on the particular failure modes observed. The current production testing specifications were also reviewed and the absence of any stress screening was noted. By analysis of this information it was concluded that there are no significant issues with the reliability of the case system. No single failure mode was dominating in the returns. This means that reliability improvement through HASS will require a high sampling rate to get a good view on the weakest points and opportunities of improvement. However, if the current failure rate is satisfactory, also a relatively small sample HASS may be appropriate to monitor the ongoing production quality.

The FRCA extent on the failed units was found to be less than thorough in many cases as the physical phenomenon causing the failure was left unclear. For these reasons a proven set of stress stimuli was proposed to provide a starting point for screening the products. It should then be modified to fit the product under test even better as the experience begins to accumulate on the findings.

Main conclusions of the case study are presented below. Refer also to the conclusions of the theoretical part in Chapter 7 and Table 4 as these are valid for the case study as well.

1. FRCA process is a potential and cost-effective source of reliability improvements.

Major benefits may be obtainable by enhancing the depth of FRCA in RMA. This is a way to enable reliability improvements without implementing any new production testing. In the case of returned material, stress testing is conducted naturally during manufacturing, delivery and field use. Relevance of faults is obvious. FRCA should also be performed not only on PCBAs but all parts of the system should they fail.

Stress screening facilities may be very useful also for the needs of FRCA if available to improve the abilities to diagnose NDF units.

2. HALT data is valuable and a prerequisite for HASS.

HASS method is very product specific and relies on HALT results. In this study 2 HASS profile proposals are given for PCBA products that have been through HALT. For System level screening, HASS cannot be applied due to lack of HALT data. Regardless of the proposed screening profile for System level, it is very much possible that better investment would be comprehensive HALT of the System. This way, the robustness properties of the system could be found in the R&D and a proper HASS specification developed.

3. All failures cannot be screened, but many can.

In this study, certain causes of failures and returns are identified that cannot be completely prevented by stress screening. These are caused by events after the product leaves the factory. Examples include erroneous handling and installation of products causing damage by ESD or misconnections as well as operating errors of equipment. The first group can be affected by stress screening in the sense that it creates more robust products against even excessive stresses. Operating errors and consequent NDF returns cannot be prevented by stress screening. However, improved failure analysis may improve the confidence in drawing conclusions of such products truly being undamaged.

9 CONCLUSION

The applicability of highly accelerated stress screening (HASS) to improve the reliability and quality of a manufactured electrical system was studied. The theoretical background of electrical product reliability and failure was outlined. Properties and requirements of HASS were explained and the mechanism allowing product reliability improvement was described. Guidelines on using HASS process were provided. FRCA and CA processes were found to be the most important part of reliability improvement. The suitability of HASS for a particular product depends on the product properties and objectives of reliability and quality. The report and the referred literature can be used as a reference when planning to apply accelerated screening methods to any product. It provides answers to the common questions and concerns around accelerated stress screening.

HASS process was then applied in a case study on an electrical system produced by a manufacturer to assist in implementation of improved production testing. The failure history and analyses were reviewed and HALT results were summarized. The present production testing specifications were also reviewed for comparison. An initial HASS profile was designed for a PCBA product. The profile will require proofing and adjustment in practice. However, for the rest of the products studied it was found that HASS cannot be applied due to product properties and lack of HALT information. Potential for improvement was found in FRCA process in some cases. The ability of HASS to improve product reliability and quality and the value of HALT data were recognized. The results can help in evaluation of the testing strategies of the case products and planning and implementing product and production quality improvements. The application procedure used can also be modified to suit any other product of the manufacturer.

Further research is needed on the software and hardware requirements of the tester. Critical test coverage analyses should be carried out on all products before the tester specification is approved. Coverage analyses of the current production testing are in the delivery and those should be used as a reference when specifying a screening test setup. Current PCBA testers cannot be used with HASS as it is because bed-of-nails fixturing is not compatible with vibration testing. However, the system tester may be applicable.

Suitable chambers, shaker equipment and fixturing to transfer the test stresses on products are also to be specified before the piloting can begin.

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