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Prescaler for a Phase Locked Oscillator

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The main goal of this project was to design a test circuit for a prescaler to be used in a phase locked oscillator. Phase locked oscillator operates on the principle of PLL. Phase locked loop (PLL) refers to a control system which generates an output signal with respect to the input signal phase and feedback. The circuit is constantly adjusted so that the frequency of the output signal is locked to that of input. The PLL has become an integral part of modern day communication systems and is widely implemented in radio communication, mobile phones and GPS systems. One of the main components of a PLL oscillator is the prescaler circuit.

To implement the prescaler circuit a PCB was designed using KiCad, an open source circuit design software and printed. A 1.1 GHz prescaler was used for low power frequency division.

The main function of a prescaler is to perform frequency division on the input signal. The prescaler designed for this thesis study can perform frequency division by a number of factors, i.e. 10, 20, 40 and 80. This division factor can be controlled by high or low signal in three pins placed on the PCB. Upon completion, a PCB that could perform the aforementioned divisions was created and then tested at different frequencies under the operating frequency range of the prescaler, to verify that the desired results would be achieved.

Different measurements were performed to determine the ideal/best operating conditions for the PLL oscillator where the designed prescaler circuit would be implemented. A PLL oscillator has a wide range of applications in terms of signal synchronization and it can be implemented in numerous modern communication and radio devices with output frequencies that range from fraction of hertz to gigahertz. With further improvements in design and assembly process, a prescaler which could yield better results circuit can be obtained.

Keywords	PLL, PCB, Pre-Scaler, KiCad

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List of Abbreviations

AC	Alternating Current
ADPLL	All Digital Phase Locked Loop
APLL	Analog Phase Locked Loop
dB	Decibels
DC	Direct Current
DPLL	Digital Phase Locked Loop
GHz	Gigahertz
GPS	Global Positioning System
LF	Low Frequency
MHz	Megahertz
NPLL	Neuronal Phase Locked Loop
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
RF	Radio Frequency
SMA	SubMiniature version A
SMD	Surface Mount Device
SPLL	Software Phase Locked Loop
VCO	Voltage Controlled Oscillator
XOR	Exclusive OR

1 Introduction

This thesis project was carried out to design a PCB where a pre scaler circuit for frequency division of the input signal would be implemented. Thus designed prescaler circuit would be used as a component of a phase locked loop oscillator system. A prototype PCB with the required components was created and the functionality of the board was tested at different frequencies upon completion. In addition to this, the functionality of a phase locked loop was also tested with the prescaler as a block of it.

Phase locked loop is one of the most important methods used in modern day electronics and communication system, and the implementation of a prescaler to it broadens its application significantly. One of the main example of such is a Phase Locked Oscillator. Phase locked oscillators use the principle of PLL to drive a voltage controlled oscillator (VCO) to generate a signal with stable frequency. The output of phase locked oscillator is the output of the VCO that is operating in the PLL. In this sense, using just a VCO instead of a phase locked oscillator might sound similar but phase locked loop enables VCO to generate frequency that is much more stable and precise.

The output of a voltage controlled oscillator, operating individually or in standalone mode, is not stable. Different external factors like temperature, noise, etc. affect the output of VCO thus making the output signal unstable in terms of the frequency. Therefore, to generate signals with absolute precise and stable frequency, a phase locked loop can be used where a local or reference oscillator can be used to ensure that the VCO oscillates at a stable frequency. If there is a change in the frequency of VCO, due to some external or internal factors, the phase locked loop adjusts accordingly to stabilize the output. Further, a prescaler enables to design a phase locked oscillator which can generate a significantly high frequency signal using a local oscillator oscillating at a lower frequency. In this case, the relation between the reference signal and the output signal is dependent on the properties of the prescaler.

Phase locked loops and its operating principle in brief have been discussed later in the text.

2 Oscillators

Oscillators are an integral part of the modern day electronic systems. Basically, an oscillator is anything that produces oscillation. Oscillation refers to any back and forth motion in a regular pattern or rhythm. In terms of electronics, the oscillations that are significant is simply this back and forth movement of voltage. An oscillator is an electronic circuit that produces periodic oscillating signals, usually a sine or a square wave.

An oscillator accepts DC voltage and generates a periodic wave of desired frequency, as shown in the block diagram in figure 1.

Figure 1. A basic block diagram showing oscillator's principle.

Irrespective of their type, all oscillators have a common principle based on which they operate. In an oscillator, a very sensitive amplifier is used to generate an output which is then fed back to the input terminal, thus creating a feedback loop system. Positive feedback loop system is a situation where part of the output signal is applied to the input by adding the feedback and input signal so that they are in the same phase as the initial input signal. The feedback is also responsible for recovering the losses, thereby sustaining the oscillation to some extent. The total closed loop gain of a positive feedback loop is greater than the open loop gain.

Let's consider the following circuit block in figure 2 where an input voltage Vin is initially applied to the amplifier.

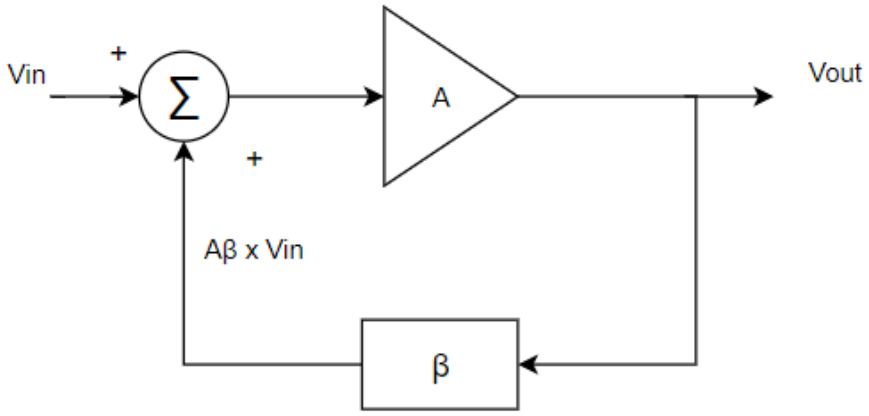

Figure 2. A basic oscillator feedback circuit.

If A is the gain of the amplifier then the voltage at the output of the amplifier is,

$$Vout = A \times Vin \tag{1}$$

This output voltage is then fed back to the amplifier through a feedback loop. If β is the feedback fraction or feedback ratio then the output of the feedback loop is,

$$Vf = \beta \times Vout = A\beta \times Vin \tag{2}$$

The term Aβ is referred to as closed loop gain of the amplifier and this closed loop gain determines the pattern of oscillation and thus the nature of the output signal.

- If the closed loop gain, $A\beta < 1$ then the signal is damped or decreasing i.e. the amplitude of the signal is decreasing and the oscillation eventually dies out.

- If the closed loop gain, $A\beta > 1$, then the oscillation is increasing, i.e. the amplitude is increasing and the oscillation is unstable. The resulting output is a distorted oscillation, which might produce a square or a saw-tooth or any other random waveform.

- If the closed loop gain, $A\beta = 1$, the oscillation is constant and continuous. The amplitude of the generated signal is constant and stable. The closed loop gain of the loop being 1 suggests that the gain of the loop is matched by the losses on the feedback.

The three conditions described above result in waveforms which have been shown in figure 3 below.

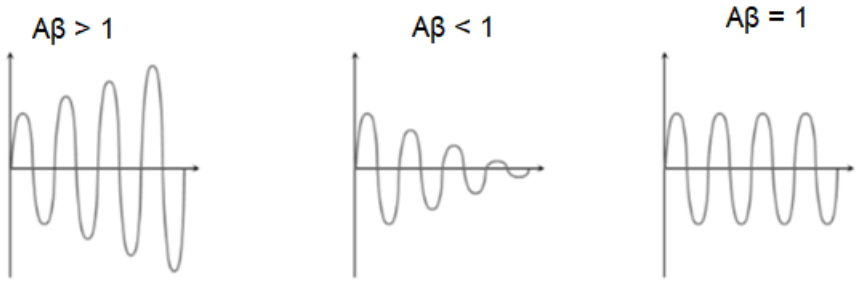

Figure 3. From left to right: increasing oscillation, damped oscillation and a stable oscillation, modified from “Oscillators: What Are They?”.[1]

In order to operate properly, an electronic oscillator must satisfy the Barkhausen Criterion, according to which the closed loop gain of the oscillator should be unity and the phase shift between the input and the feedback input should be a multiple of 360 degrees.

In terms of the signal they produce, oscillators can be classified into following two categories:

- Linear or Harmonic oscillators, which produce a sine wave with constant amplitude and frequency

- Non-linear or relaxation oscillators, which produce non sinusoidal output like square waves, saw-tooth wave etc.

Linear oscillators can further be classified into different categories in terms of their output frequency, RF oscillators and LF oscillators. RF oscillators are oscillators that produce frequency in the range of 100MHz-1000 MHz or above, whereas LF oscillators are this oscillators that produce signals with frequency less than 30 MHz.

Besides these, an oscillator can also be categorized on the basis of their frequency control mechanism, which have been briefly stated below.

- LC oscillators: As suggested by name, LC oscillators have an inductor and a capacitor in parallel, which is also called tank circuit. The frequency of oscillation depends inversely upon the value of the inductance and capacitance of the inductor and capacitor respectively. LC oscillators are mainly used in to generate RF signals. The signal generated by LC oscillators are steady in terms of the shape and frequency of the signal provided that the capacitor and inductor are ideal, i.e. with ohmic resistance zero.

- RC oscillators: RC oscillator use resistors and capacitors with an amplifier that produces a phase shift of 180 degrees. The RC element is used in the feedback loop to produce a phase difference in such a way that eventually, the signal fed back to the input has a phase shift of 360 degrees, which would basically be similar to a phase shift of zero degrees. RC oscillators are commonly used to generate low frequency signals.

- Crystal oscillators: Crystal oscillators produce electric signal by using mechanical vibration of crystal of a piezoelectric material. Thus produced electric signal is highly precise in terms of frequency stability. When voltage is applied, the crystals are distorted. When the voltage is removed, signals are generated as the crystals try to return to their original shape. Crystal oscillators have a fixed frequency which is determined by the physical properties of the crystal. [2]

Other than these classifications, oscillator can also be classified on the basis of the frequency as fixed frequency oscillators or variable/tuneable frequency oscillators.

Oscillators have a wide range of application in the modern day and are used in a lot of electronic devices like computers, clocks, metal detectors, microcontrollers, music synthesizers, radio communication etc. They are used in wireless transmitters and receivers to generate and collect real time signals. Oscillators can also be used to generate waveforms in power systems. Hence, it can be said that they are an integral block of any present electronic devices.

3 Introduction to Phase Locked Loop

A phase-locked loop (PLL) is a closed-loop frequency-control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator [3].

PLL is a specific type of an electronic feedback system which operate by continuously changing a voltage or current-driven oscillator in order to match (or lock into) the input signal phase and frequency. In order to produce the desired output signal, PLL can add, multiply, divide and/or mix various frequencies. PLLs usually consist of the following components:

- voltage driven oscillator VCO,
- error comparator/detector,
- loop filter,
- prescaler feedback counter.

These basic blocks that form a PLL have been shown in the figure 4 below.

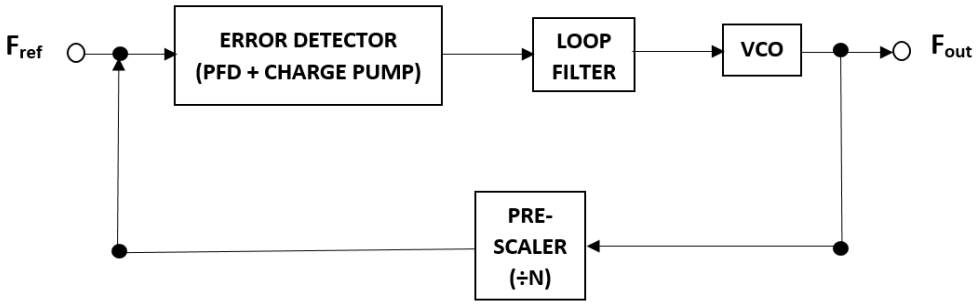

Figure 4. Blocks of a basic PLL, modified from MT-086: Fundamentals of Phase Locked Loops (PLLs). [4]

The output frequency can be expressed in terms of the reference frequency as:

$$F_{out} = N \times F_{ref}, \quad (3)$$

Where Fref is the reference frequency and is the frequency of one of the two inputs applied to the error detector.

PLLs are used for producing, stabilizing, modulating, demodulating, filtering or restoring signals from a "noisy," disrupted communication stream. They are used widely in the field of cellular communication, radio technology and other general electronic items, ranging from mobile phones to radio broadcasters, TVs and wireless routers to walkie-talkie radio stations so on. In digital data transmission, phase locked loops are usually used more frequently than in analog transmission.

A PLL operates in one of the three following operating modes: free running mode, capture mode and tracking mode.

- A PLL is considered to be in free running mode before any input is applied to it. At this stage, the output of the error detector and the loop filter is zero and VCO runs at free-running frequency.

- When an input is applied, an error generated control voltage is generated which, as an input at VCO, causes change in the output frequency of VCO. At this stage where there is change in the VCO frequency, a PLL is said to be in a capture mode.

- When the PLL is locked, it is said to be in tracking mode.

3.1 Parts of PLL

As mentioned earlier there are four basic blocks or parts in a PLL system. They have been discussed briefly in the sub headings below.

3.1.1 Error Detector/Comparator

The error detector consists of a phase frequency detector (PFD) and a charge pump. The key phenomenon for operation of a PLL is the phase difference between two signals and as implied by its name, the phase detector block in a PLL performs this comparison.

The two input signals are the reference signal with frequency F_{ref} and the feedback signal with frequency F_{out}. An error voltage, which is directly proportional to the difference between the phases of the two signals is generated by the phase detector. This error-generated-voltage can then be used to regulate the frequency of the PLL. Preferably, the two signals should be very identical to each other i.e. the phase difference between them should be very small.

The charge pump is responsible for feeding or drawing current to or from the loop filter depending upon the state of the signal fed to it by the PFD. The signals generated by the PFD are either an up signal or a down signal. The state of these signals depend upon the phase (leading/lagging) of the feedback signal. The VCO operates at a higher frequency if the state of control signal is ‘up’ and vice versa. The charge pump drives the current to the loop filter if it receives an ‘up’ signal and it draws the current from the loop filter if it receives a ‘down’ signal. [3]

3.1.2 Voltage Controlled Oscillator.

Voltage driven oscillator or Voltage controlled oscillator (VCO) is an important part of a phase locked and loop. The VCO block generates an RF signal which, usually, is the output of the phase locked loop. The output of the voltage controlled oscillator can either be a sine waved signal or squared wave signal depending upon the need. The frequency of thus generated signal depends on the input voltage applied at the oscillator. The relation between the applied voltage and output signal in a voltage controlled oscillator is linear, i.e. if the applied voltage increases, the output frequency increases and vice versa.

3.1.3 Loop Filter

Loop filter is a compensating element which provides loop stability. Loop filter produces a control voltage based on the signal received by the charge pump and allows it to pass through to the VCO. This control voltage, which is applied to the VCO, is used to determine the level (high/low) of frequency at which the VCO needs to operate. The frequency and phase of the VCO and the feedback clock is dependent upon this control voltage. The control voltage generated by the loop filter increases upon the application of current

to it and decreases if current is drawn from it. The voltage controlled oscillator's frequency increases when the current is driven to loop filter and decreases when the current is driven from it. Loop filter, generally, is a low pass passive RC filter.

Loop filter has two main functions:

- to filter the unnecessary high frequency components of the frequencies at the phase detector which affect the VCO control input, and
- to govern the loop stability.

The balance between noise and frequency can be achieved by selecting accurate bandwidth, type and order of the loop filter. Loop filter also determines the properties of PLL like capture range, lock range and the bandwidth of the PLL.

3.1.3.1 Lock Range

A PLL lock range is the range of frequencies at which the PLL is able to track the frequency of the input signal and remain locked. The free running frequency of the VCO has to lie in the lock range of the PLL. The PLL will not achieve locked state if the frequency of the input signal is outside its lock range.

3.1.3.2 Capture Range

Capture range of a PLL is the frequency range where the PLL obtains lock. Capture range is very narrow in comparison to the lock range and always lies in the lock range. The VCO free running frequency lies in the capture range as well. The basic concept of capture range and lock range have been shown in the figure 5 below.

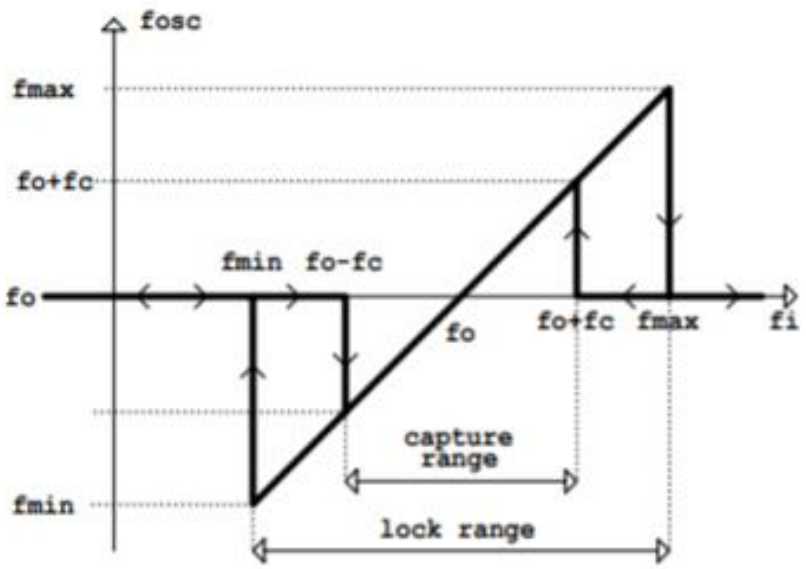

Figure 5. Capture range and lock range of a PLL, copied from CMOS 4046 Phase-Locked Loop. [5]

In the aforementioned figure 4,

- fo is the free running frequency,
- 2fc is the capture range with lower and upper limits fo-fc and fo+fc respectively,
- and, fmax-fmin on the fi axis is the lock range of the PLL.

3.1.3.3 Loop Filter Bandwidth

As it has already been mentioned, the loop filter plays a major role in determining the loop bandwidth of the PLL. The cutoff frequency of the loop filter determines the PLL bandwidth. The lower the cutoff frequency of the loop filter, the lower the PLL bandwidth and vice versa. Higher bandwidth ensures faster response of PLL for output frequency adjustment but at higher bandwidth a PLL is harder to control.

3.1.4 Prescaler Counter

A prescaler is an electronic counter circuit that is used to decrease the frequency of a high frequency signal by performing an integer division on the input frequency. In other words, prescaler is a frequency divider circuit. Prescalers are of great significance as they can be used to generate different low frequency signals from a single frequency source. Standard prescaler performs frequency division by a fixed factor N, whereas a dual modulus prescaler has a programmable/adjustable frequency division factor. A dual-modulus prescaler is a counter whose division ratio can be switched from one value to another by an external control signal [3].

In case of a phase locked loop, the output of the prescaler should be very close to the reference input signal to achieve a lock.

3.2 Types of PLL

Depending upon the types of components used as the building blocks, a PLL can be of three different types: analogue or linear PLL (LPLL), digital PLL (DPLL), all-digital PLL (ADPLL), software PLL (SPLL) and neuronal PLL (NPLL).

3.2.1 Analogue PLL

A PLL is said to be linear PLL if all the components, i.e. the phase detector, the loop filter and VCO are analog components and the multiplier used is a linear element. The loop filter can be active or passive. It is also denoted as APLL. Generally, an analogue PLL consists of a mixer in the loop, which is used to generate a small frequency shift to the feedback input frequency by application of an external signal to it. A basic operational block diagram of an analogue PLL has been shown in the figure 6 below.

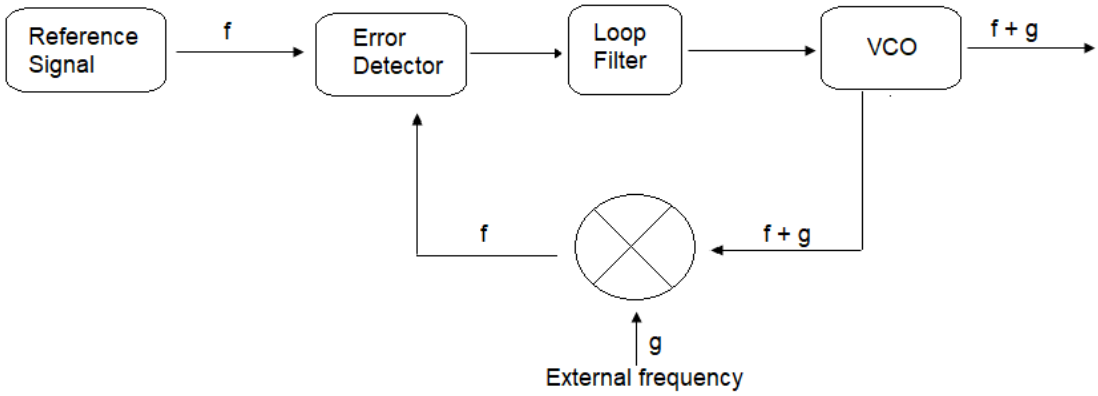

Figure 6. Block diagram of an APLL, modified from PLL Frequency Synthesizer Tutorial. [6]

3.2.2 Digital PLL

A digital PLL (DPLL) is basically, just an upgraded APLL with a digital phase detector. All other components other than the phase detector are analog components. Digital gates like XOR gate, edge triggered JK flip flop are generally used as the phase detector in DPLL. A DPLL may also have a digital frequency divider. A basic operational block diagram of a digital PLL has been shown in the figure 7 below.

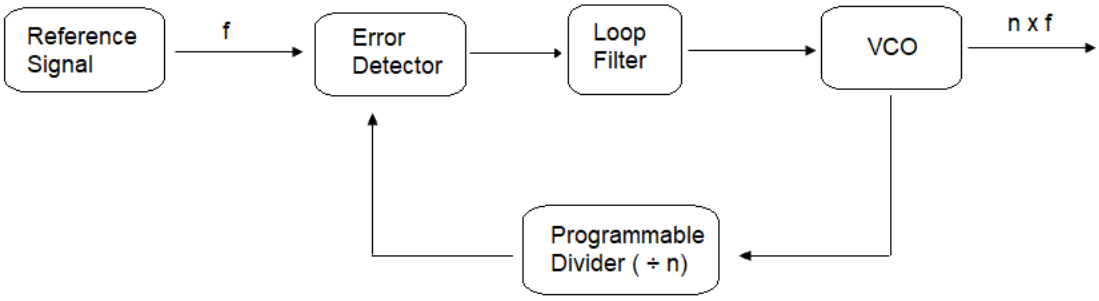

Figure 7. Block diagram of a DPLL, modified from PLL Frequency Synthesizer Tutorial. [6]

3.2.3 All-Digital PLL

An all-digital PLL is a PLL which consists of digital components only. It is exclusively built without any passive or linear components. An ADPLL usually consists of a NCO which is a numerically controlled oscillator. An ADPLL, thus locks the frequency and phase of the NCO to the phase and frequency of the reference signal.

3.2.4 Software PLL

A software PLL (SPLL) is a PLL developed in the software domain where the blocks are deployed in terms of software that than the actual hardware.

3.2.5 Neuronal PLL

A neuronal PLL consists of blocks which consists of neurons. “The simplest embodiment of the NPLL includes a phase detector (that is, a neuronal plausible version of an ideal coincidence detector) and a controllable local oscillator that are connected in a negative feedback loop”. [7]

3.3 Operating Principle of a PLL

A reference frequency F_{ref} is applied to the PLL, which creates some error voltage that drives the voltage controlled oscillator. The frequency of this output signal varies as the error voltage changes. This output of the voltage controlled oscillator is partially fed back to the PLL and this VCO output which goes through the prescaler circuit acts as a second input for the error detector. The error detector produces an error voltage which is equal to the difference between the two signals: reference signal and the feedback signal. When the reference signal and feedback signal have equal frequency the PLL is considered to be locked. Hence, it can be said that when a phase lock loop is locked:

- the reference signal and feedback signal have same frequency and a very small phase difference,
- the error voltage generated by the error detector is constant, the difference between the two input signals at the error detector is zero.

Once the loop is locked, then the PLL adjusts itself to any change in the input frequency F_{ref} in its lock range. If the input F_{ref} is increased or decreased slightly, the error detector generates an error voltage accordingly which is fed to the loop filter. As a result, the loop filter changes the tuning voltage for the VCO, thus changing the VCO output frequency which eventually changes the feedback frequency. This feedback frequency adjustment

phenomenon keeps the loop locked, as long as the applied frequency is within the lock range of PLL.

Mathematically, if F_{ref} is the applied reference frequency, F_{out} is the frequency of output signal generated by VCO, and if N is the frequency division factor of the prescaler then the frequency of the two input signals at the error detector is F_{ref} and F_{out}/N.

If e(s) is the error voltage, then,

$$e(s) = F_{ref} - F_{out}/N \tag{4}$$

When the PLL is locked, e(s) = 0. [8]

$$F_{ref} - F_{out}/N = 0 \tag{5}$$

$$F_{ref} = F_{out}/N \tag{6}$$

$$\mathbf{F_{out} = N \times F_{ref}} \tag{7}$$

4 MC12080dg Prescaler

The module used to implement the prescaler circuit for this thesis study is the MC12080 dg module which performs low power frequency division by four specific division factors: 10, 20, 40 and 80. The frequency division factors are controlled by the state of three control signals SW1 SW2 and SW3. This frequency range for operation of the module is 100 MHz to 1.1 GHz. The different division factors and the corresponding state of the control signals have been shown in the table 1 below.

Table 1. Control signal states and their corresponding division factors, copied from MC12080 1.1 GHz Prescaler. [9]

SW1	SW2	SW3	N
L	L	L	80
L	L	H	40
L	H	L	40
L	H	H	20
H	L	L	40
H	L	H	20
H	H	L	20
H	H	H	10

In table 1, L refers to low and H refers to high. N is the frequency division factor. Control signals are high when a DC voltage equal to Vcc i.e. 5V is applied to the control pins and low when they are left open.

5 Observations and Measurements

To achieve the goals, firstly a schematic and its corresponding layout were created in KiCad. KiCad is a free design software which is used for electronic circuit design. It is equipped with tools for creating schematics and implementing them to PCB layout design. The schematic for the pre scaler circuit has been shown in the figure 8 below.

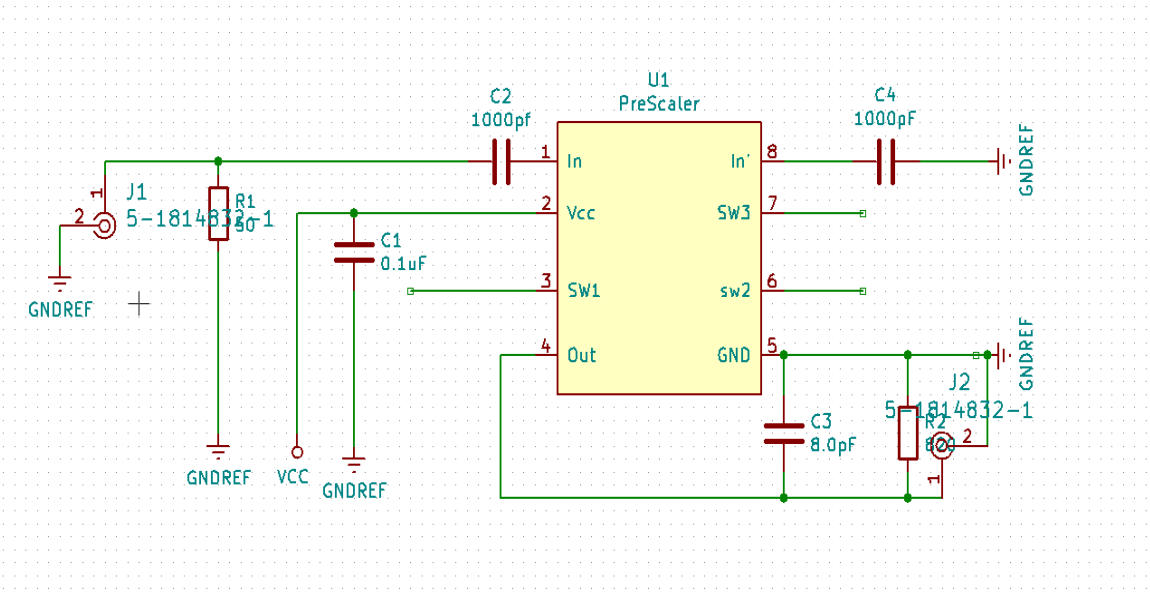

Figure 8. Schematic for prescaler circuit

The aforementioned schematic was then implemented as a layout, which has been shown in the figure 9 below. The footprints for the coaxial SMA male connectors and the MC12080DG module were downloaded and modified from online library.

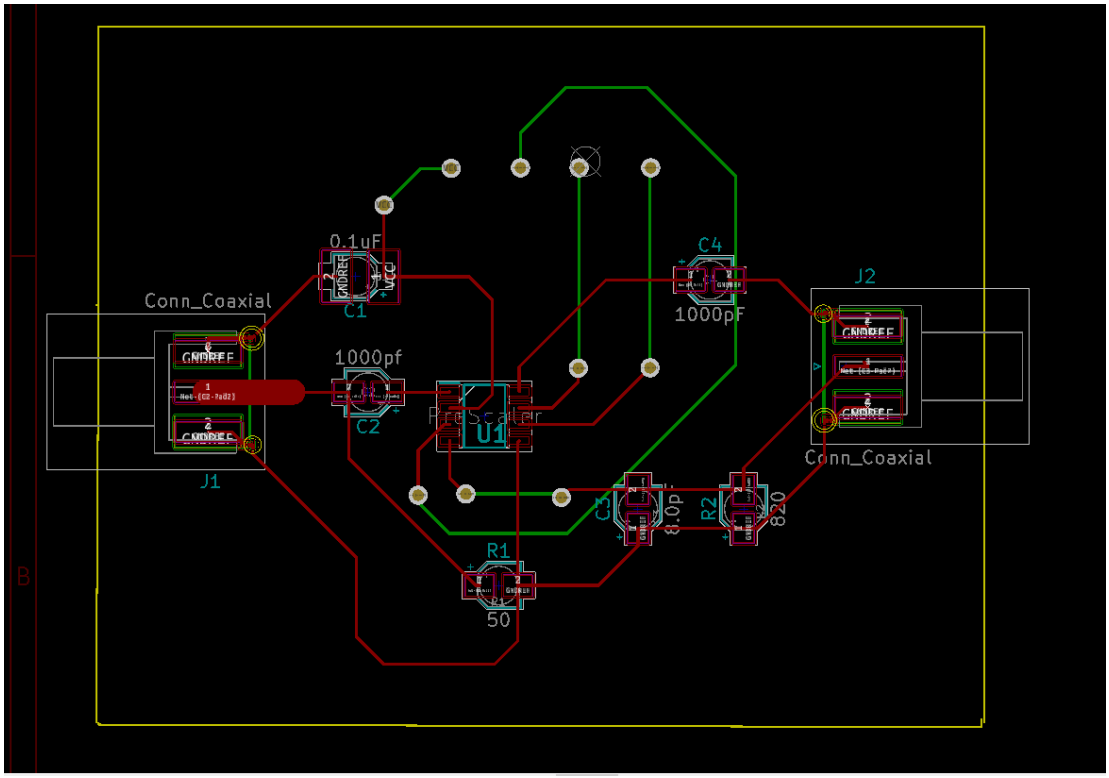

Figure 9. PCB layout for prescaler circuit

The designed layout was then printed into a board using the milling machine at Metropolia UAS and the corresponding components were soldered to the board. The components used for the implementation were resistors, capacitors, SMA connectors and a MC12080dg prescaler. All the components used in the prescaler were SMD components. The final outcome resulted in a PCB which is shown in the figure 10 below.

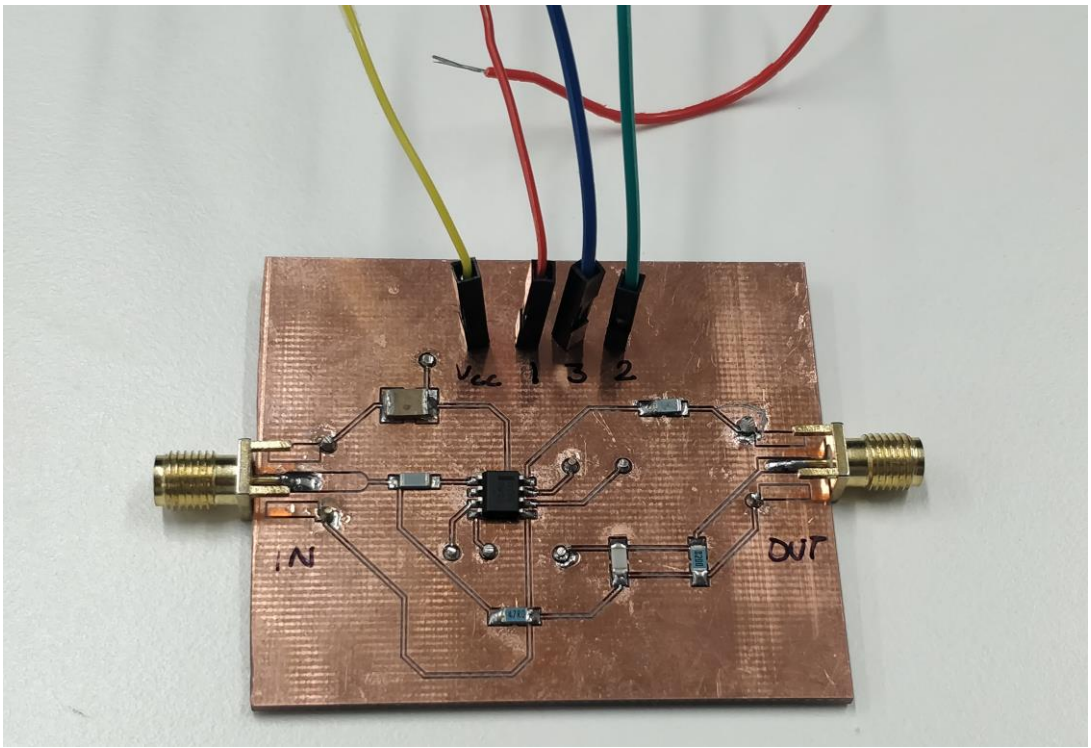

Figure 10. Prototype for the prescaler.

The signal is fed through the SMA connector labelled ‘in’ and the output signal is obtained from the SMA connector labelled ‘Out’. A DC supply voltage V_{cc} = 5 Volts is applied through the pin marked V_{cc}. The frequency division factor is determined by the state of the control signals 1, 2 and 3. Control signals are either high or low. Control signals are high when a DC voltage of 5V is applied to the control pins and low when they are left open.

The objective of this thesis study is to verify the functionality of the designed prescaler circuit and compare the obtained results to the theory and analyze various measurement values to validate the ideal operating range of the prescaler in a PLL oscillator.

To test the functionality of the prescaler PCB designed, it was tested at different frequencies. Other than the frequency division, various other measurements were done to analyze different properties of the prescaler. These measurements were done to analyze the following:

- output of the prescaler at different output frequencies.

- power loss/attenuation at different input frequencies at different division factors
- power loss/attenuation at different input power levels, and
- functionality of the PLL with the prescaler PCB.

5.1 Measurement Setup

The measurements were carried out in the electronics lab at Metropolia UAS. HP's 8648B synthesized RF signal generator was used to generate the input signal that was fed to the prescaler circuit. The output of the prescaler was analyzed using a HP E4411B spectrum analyzer. The basic block diagram of the measurement setup has been shown in the figure 11 below.

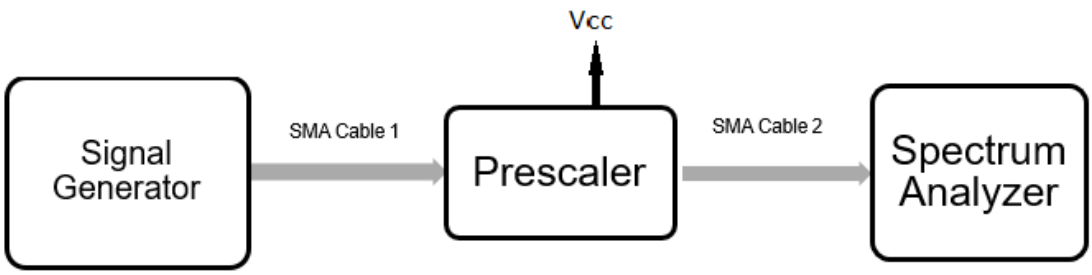

Figure 11. Block diagram of measurement setup

First the signal generator and the spectrum analyzer were connected with each other using two SMA cables and a connector to note the error in the measurements. The error was calculated for different read range presets at the output and were corrected accordingly while the measurements were carried out with the prescaler connected. The actual measurement setup for the measurements has been shown in appendix 1. Table 2 shows the error values at different frequency range at the spectrum analyzer.

Table 2. Reading error at spectrum analyzer.

Read Range	Error (dBm)
0-500 MHz	4.6
0-100 MHz	6.6
0-50 MHz	7.6

5.2 Prescaler Output Frequency

As stated earlier, the output frequency of the prescaler depends upon the input frequency and the division factors which is determined by the control signals SW1, SW2 and SW3. A supply voltage V_{CC} = 4.8 voltage was applied to the prescaler circuit. The same voltage value was used for the control signals when they were in 'High' state. The prescaler can have the same division factors for different configurations of the control signal's states. An input signal with an input frequency, F_{in} = 1000 MHz was applied and the output frequency for different division factors (N) at corresponding configuration of the control signals were measured. The frequency for the first second and third harmonics were also measured. The result of this has been shown in the table 3 that follows.

Table 3. Verification of frequency division

SW1	SW2	SW3	N	F_{in} (in MHz)	F_{out} (in MHz)	Frequency at Harmonics		
						1st	2nd	3rd
L	L	L	80	1000	13	25.3	38	43.4
L	L	H	40	1000	25	50	75	100
L	H	L	40	1000	25	50	75	100
L	H	H	20	1000	50	100	150	200
H	L	L	40	1000	25	50	75	100
H	L	H	20	1000	50	100	150	200
H	H	L	20	1000	50	100	150	200
H	H	H	10	1000	100	200	300	400

It can be clearly seen that the input frequency is N times the output frequency in almost all the cases. The prescaler module used in the PCB was stated to have an operating range between 100-1100 MHz (i.e. 0.1-1.1 GHz). The circuit was tested with input frequencies higher than the range of the prescaler module and the result has been shown in the table 4 below. The frequency division for N = 40 has also been shown in appendix 2.

Table 4. Output at higher frequencies

N	F_{in} (in MHz)	F_{out} ((in MHz)
10	1200	120
	1300	128
	1400	128
	1500	138
20	1200	60
	1300	64
	1400	64
	1500	64
40	1200	30
	1300	34
	1400	34
	1500	34
80	1200	15
	1300	16.3
	1400	17.3
	1500	15.8

The results from table 4 show that the prescaler circuit functions properly up to 1.2 GHz but doesn't function as desired at frequencies higher than that.

5.3 Power Loss as a Function of Frequency.

The power loss for the prescaler circuit was calculated at different frequencies and different division factors. To perform this measurement, the input power was set to 0 dBm and the output at different input frequencies was noted. The spectrum analyzer used had an error of +4.6 dBm for read preset range 0-500 MHz and +6.6 dBm for 0-100 MHz at output which was subtracted from all the readings accordingly for correction.

The frequency division factor was set to 10 and input frequencies ranging from 100-1000 MHz was applied. The power loss at different frequencies for division factor, N =10 has been show in figure 12 below.

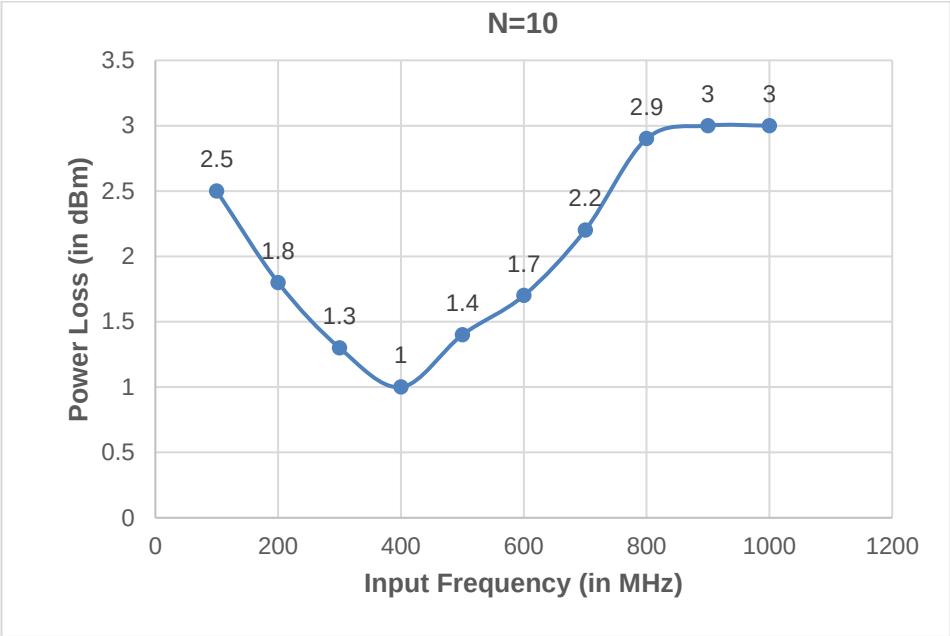

Figure 12. Observed power loss at 100-100 MHz for N=10

It can be seen that the power loss decreased as the input frequency was increased from 100-400 MHz, and it increased at 400-900 MHz and was almost constant at higher frequencies. The division factor was then set to 20, using all configurations for the control signal and figure 13 shows the power loss at different frequencies.

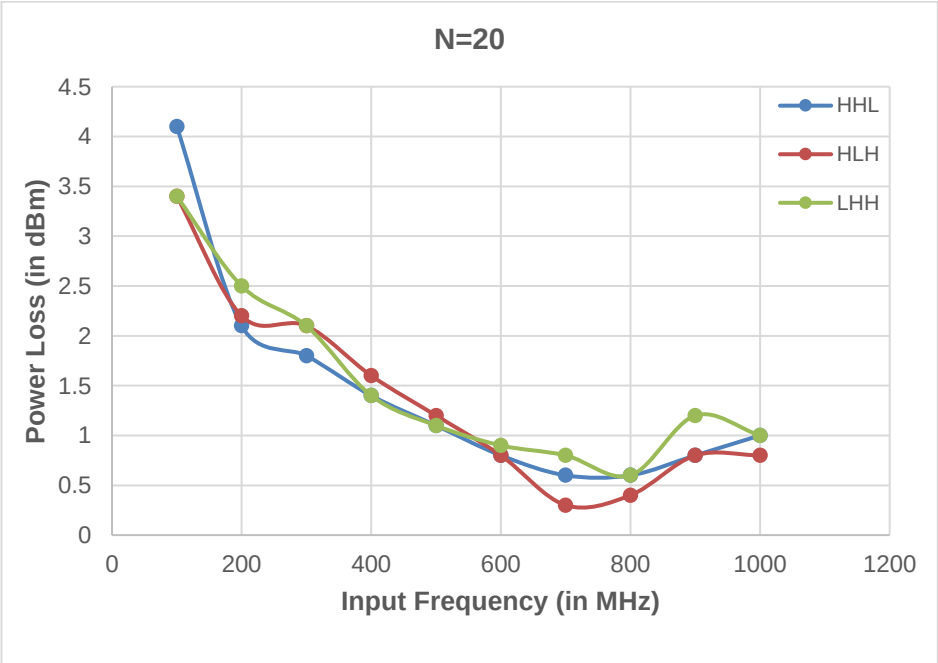

Figure 13. Observed power loss at 100-1000 MHz for N=20

The letters HHL, HLH and LHH denote the state of the control signals, since N =20 can be achieved for all these state of the signals. For example HHL is the state while the state of control signals SW1 and SW2 is high, and SW3 is low. It was observed that the power loss was much higher at lower frequencies and were lower and almost constant at higher frequencies. Slight variations were observed for different configurations for control signals' states.

The division factor was then set to 40, using all configurations for the control signal which has been shown in figure 14 below.

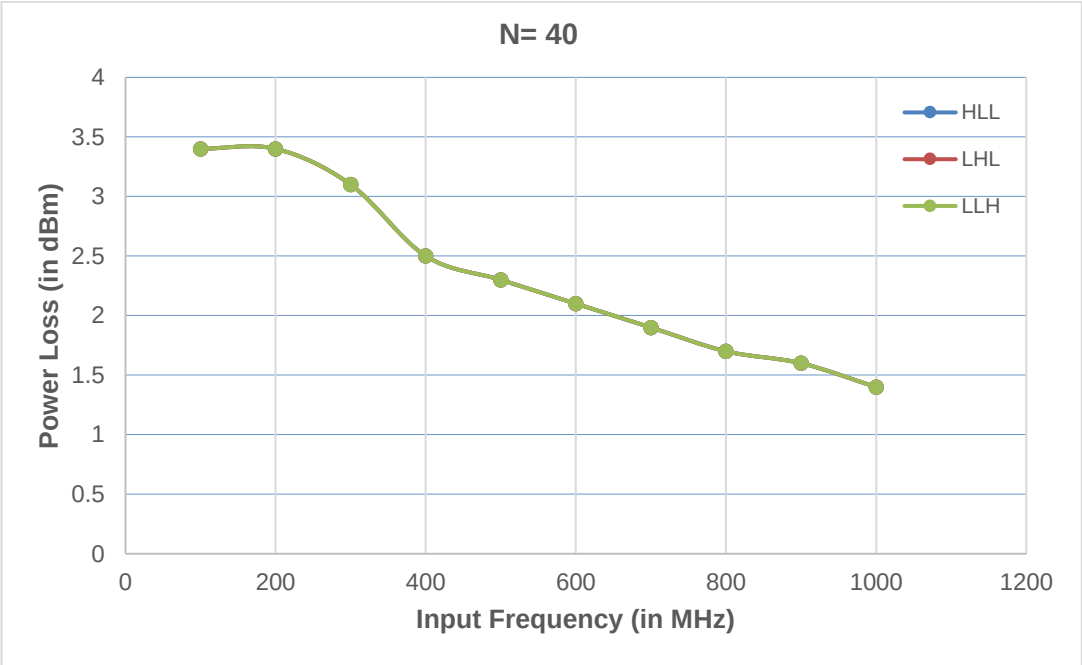

Figure 14. Observed power loss at 100-1000 MHz for N=40

It can clearly be seen that the power loss at N=40 was exactly the same for all configurations of the control signal states. The power loss for the prescaler circuit was found to be higher at lower frequencies and lower at higher frequencies.

The division factor was then set to 80 and the power loss obtained at frequencies 100-100 MHz has been shown in figure 15 that follows.

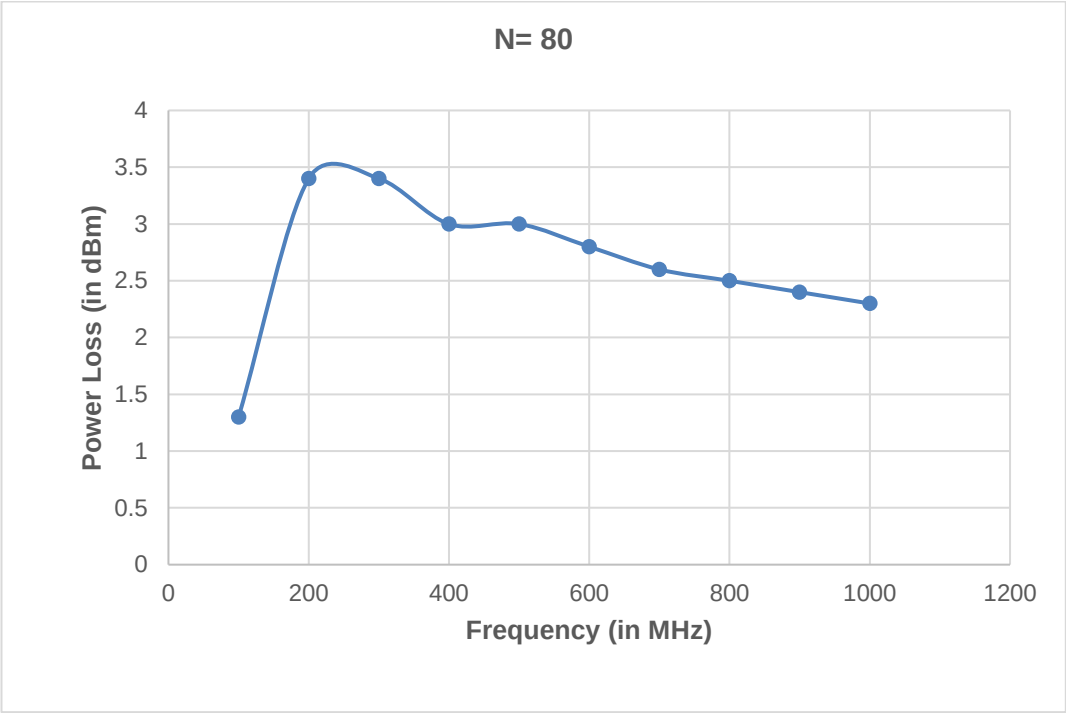

Figure 15. Observed power loss at 100-1000 MHz for N=80

It can be observed that the power loss at N=80 was higher at lower frequencies and lower at higher frequencies, the power loss at 100 MHz being an exception.

5.4 Power Loss as a Function of Input Power

The feasible input power that can be applied to the prescaler circuit depends upon whether the input power falls under the operating window of the MC12080DG module at the frequency division factor being used. Thus the maximum and minimum power level of the input signal to be applied to the prescaler have to be within the operating window of the MC12080 module for the prescaler to function properly. Figure 16 below, provides an insight on the operating window of the MC12080 for division factor, N = 10.

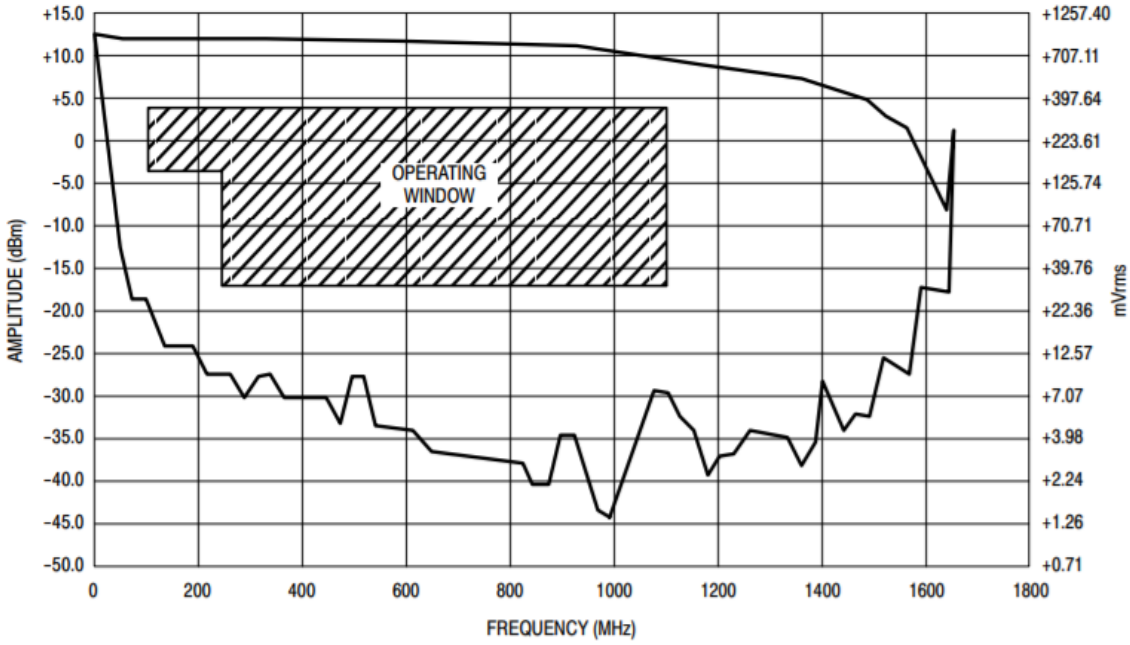

Figure 16. Input signal frequency versus input signal amplitude of MC12080 at division factor N=10, copied from MC12080 1.1 GHz Prescaler. [9]

The power loss of the prescaler circuit was measured at different input power level and different division factors keeping the input frequency constant. These measurements were done at three different input frequencies, F_{in} = 100 MHz, 500 MHz and 1000 MHz, for division factors N = 20, 40, 60 and 80. To study the behavior of the prescaler, input power, outside the ideal operating window was also applied to the prescaler circuit. Necessary error corrections were done for these measurements, using exactly the same error correction values that were used for the power loss calculation.

Figure 17 shows the graphical representation of the attenuation as a function of the input power at N=10.

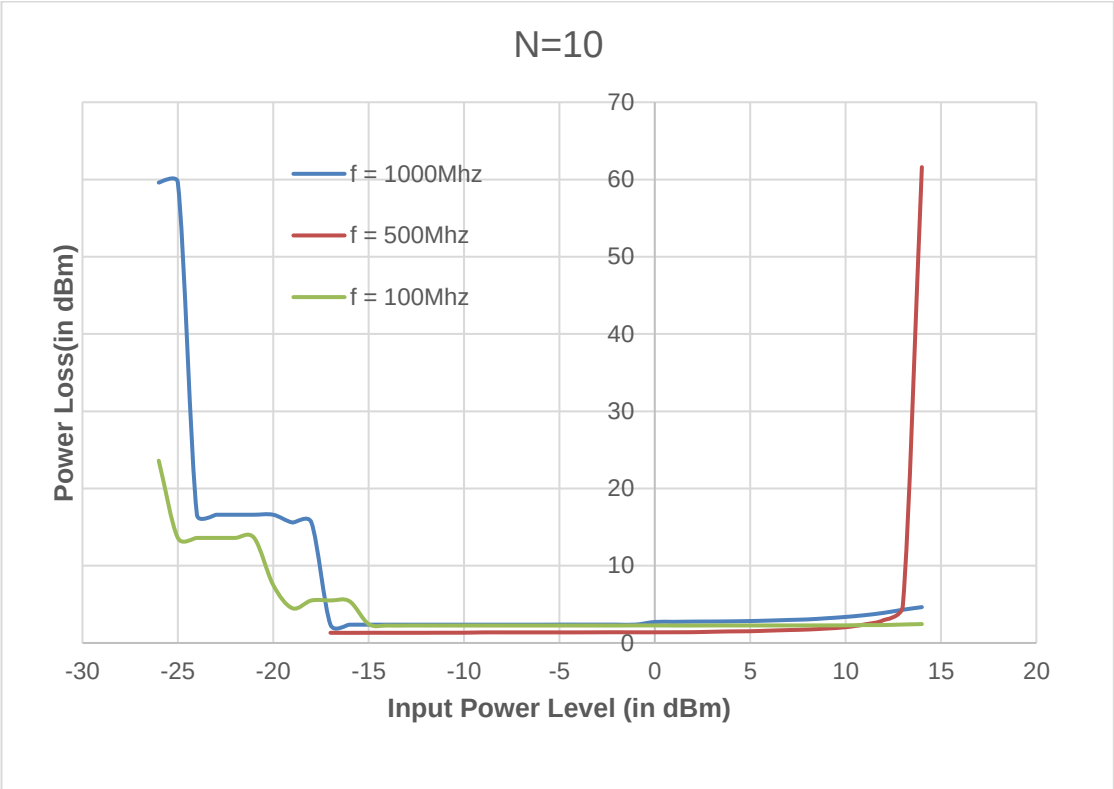

Figure 17. Attenuation as a function of input power level at N=10.

It was seen from aforementioned figure 10 that the power loss is almost constant for the frequencies 1000 MHz, 500 MHz and 100 MHz for input power range -15 to +13 dBm and outside these ranges the power loss increases significantly, thereby suggesting that the ideal operating range for the prescaler at division factor, N=10 would be between -15 and +13 dBm.

Likewise, the attenuation at different input power level at N=20 has been shown in figure 18 below.

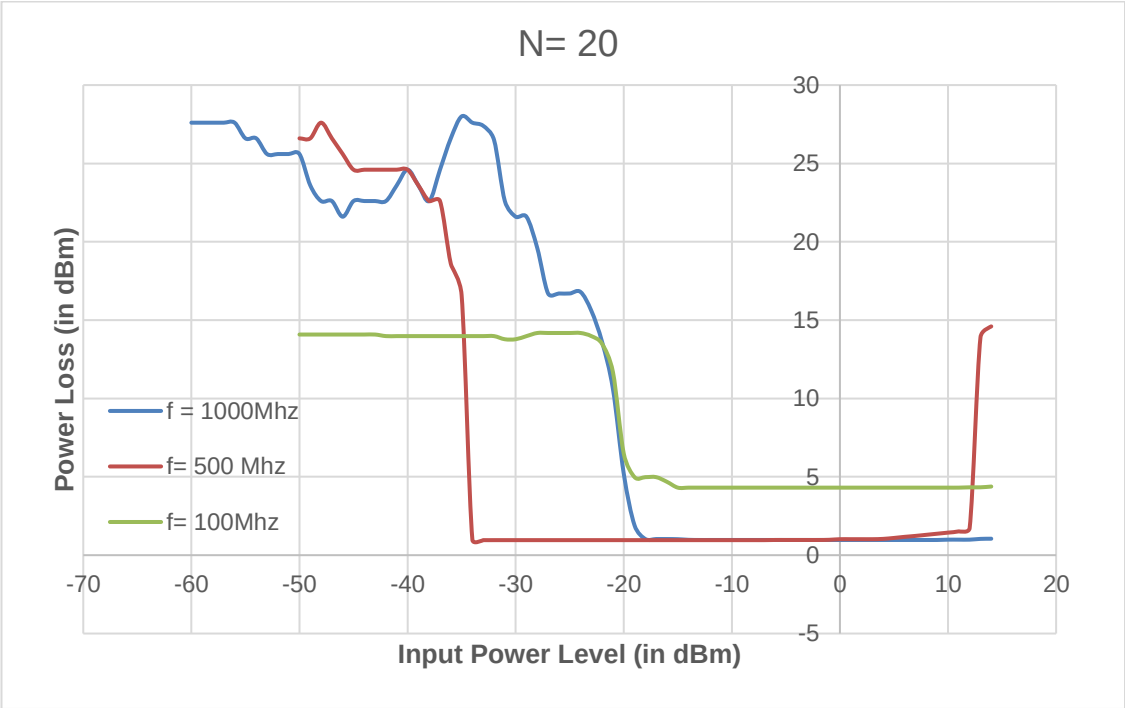

Figure 18. Attenuation as a function of input power level at N=20.

As seen in figure 17, the attenuation at output was constant for input power range -40 to 12 dBm at 500 MHz and for 100 MHz and 1000 MHz, the power loss was constant at the range of -20 to 14 dBm. The attenuation was found to be higher at 100 MHz than at higher frequencies, 500 MHz and 1000 MHz.

Similarly the attenuation for different input power levels at N= 40 has been shown in figure 19 below.

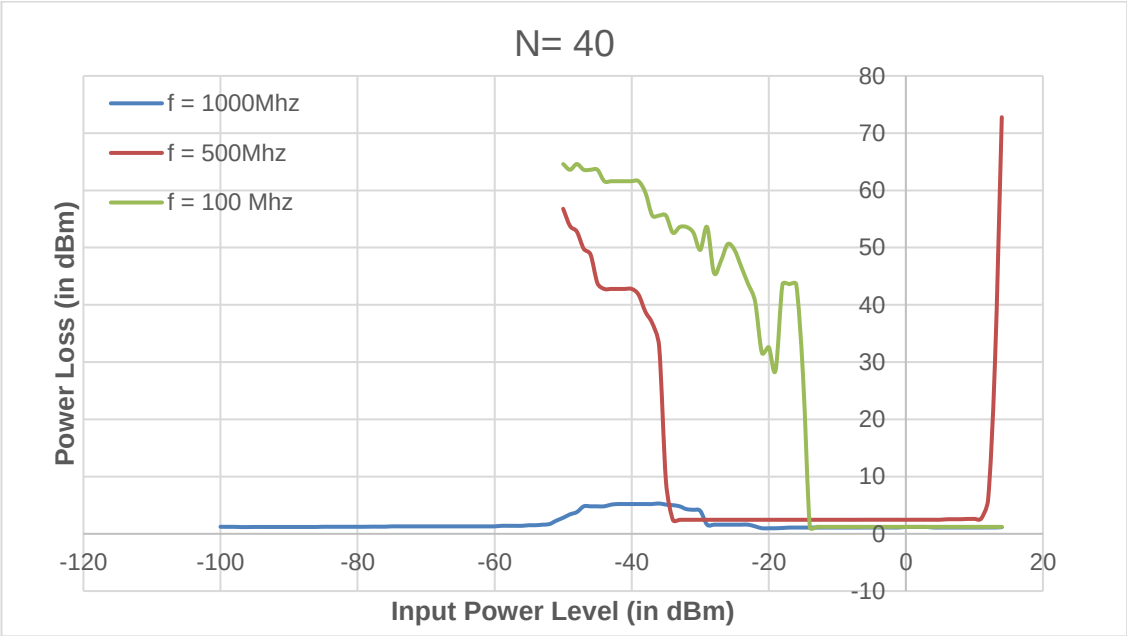

Figure 19. Attenuation as a function of input power level at N=40.

It can be clearly seen that the attenuation was constant for all input power levels between -100 to 14 dBm for an input signal with frequency 1000 MHz. However, at 500 MHz, the attenuation was found to be constant only between -33 to 11 dBm. And finally at 100 MHz, constant attenuation was achieved only for a small range between -13 dBm and 14 dBm.

Finally, the attenuation at N = 80 was noted, the graphical representation of which has been shown in figure 20 that follows.

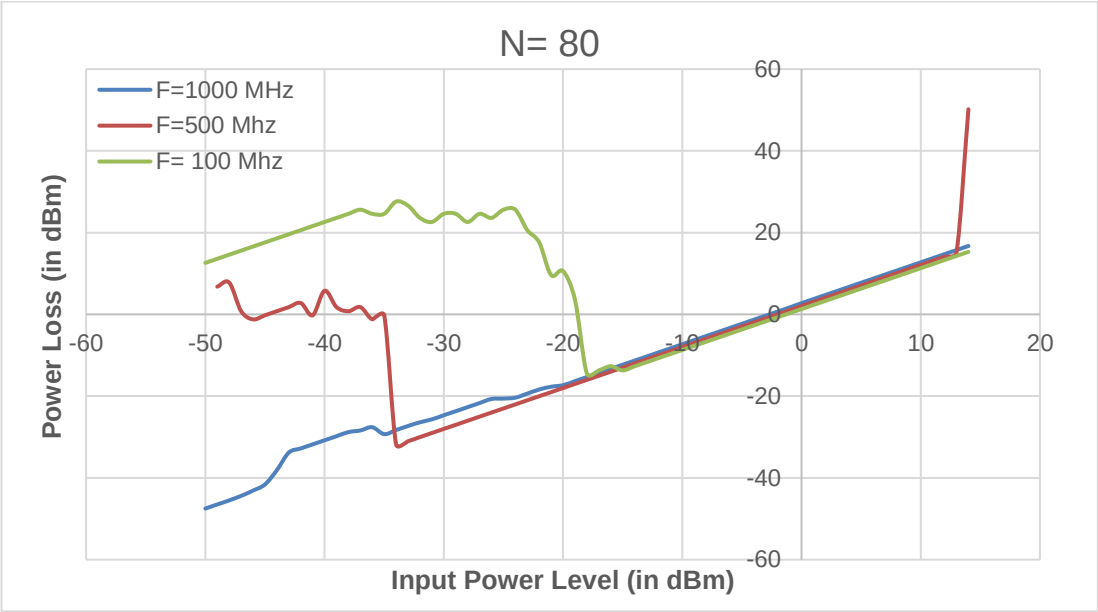

Figure 20. Attenuation as a function of input power level at N=80.

As can be seen in figure 19, the prescaler circuit showed an abnormal behaviour at lower input power levels at N= 80 by amplifying the input signal. At 1000 MHz, the input signal was amplified between -50 and -2 dBm after which the attenuation increased linearly between -2 and 14 dBm. At an input frequency of 500 MHz, this abnormal behaviour of amplification was shown between -47 to -4 dBm, after which the attenuation increase linearly. However at lower frequency of 100 MHz, the signal underwent amplification for a smaller range of input power, -18 to -2 dBm. For all three input signals, the attenuation characteristics of the prescaler circuit was similar for the input power range of -2 to 14 dBm, thus suggesting that at N= 80, the operating window in terms of input power level lies in the range of -2 to 14 dBm.

5.5 Prescaler in Phase Locked Loop

Finally, the prescaler PCB was used as a part of a phase locked loop. This was to check if the phase locked loop would then collectively function with the prescaler PCB that was created during this project. A block diagram of the implementation has been shown in figure 21 below.

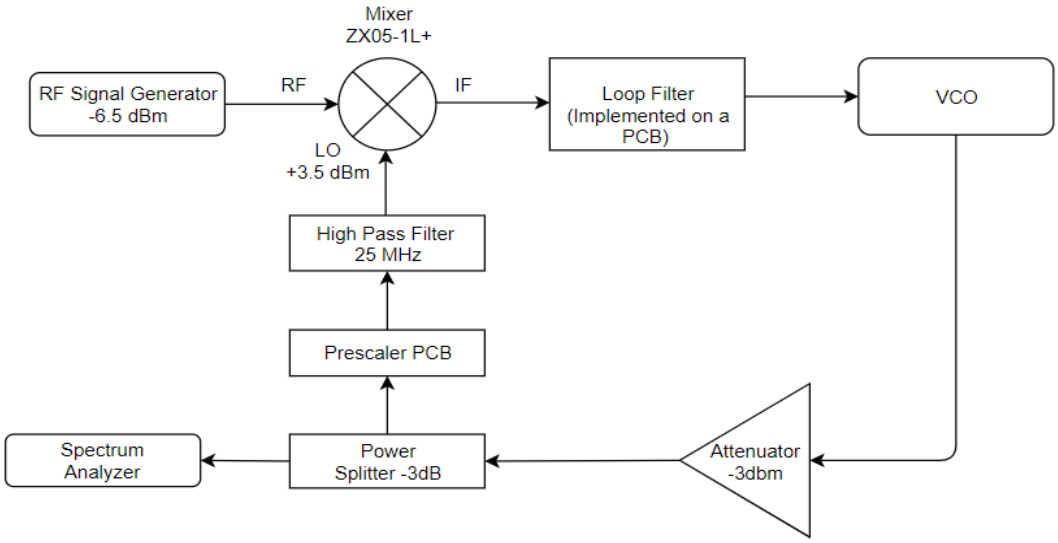

Figure 21. Block diagram of circuit to test the functionality of the phase locked loop together with the designed PCB.

Each component blocks were connected and tested sequentially to verify the functionality of each component and to discover errors, if any. While performing these tests, a DC power supply was used to supply the tuning voltage and VCC for the voltage controlled oscillator. The VCO used was ZX95-1300+ from Mini Circuits. The relationship between the tuning voltage and output frequency of a ZX95-1300+ voltage controlled oscillator has been shown in figure 22 below.

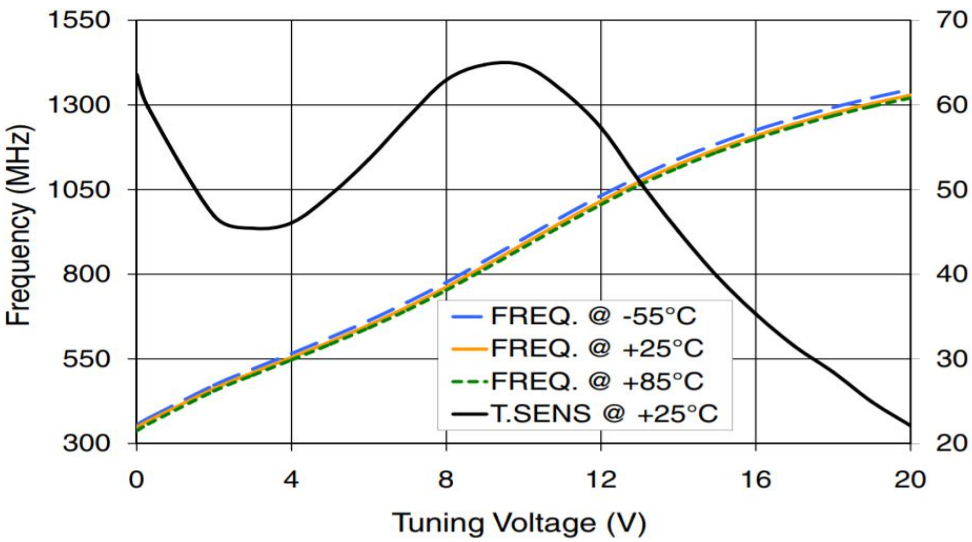

Figure 22. Frequency as a function of tuning voltage in ZX95-1300+ VCO, copied from Voltage Controlled Oscillator - Mini Circuits datasheet. [10]

To generate a frequency of around 1000 MHz, tuning voltage V = 12 V and supply voltage VCC = 5 Volts were applied to the VCO. The tests were performed on the following order:

1. First, the output of VCO was measured with the spectrum analyzer to measure and verify the output frequency. The output frequency was found to be f = 1020 MHz.

2. This output was then connected to the prescaler PCB whose division factor was set to N = 40. The output of the prescaler was then measured using the spectrum analyzer and was found to be 25.6 MHz.

3. This output of the prescaler, i.e. 25.6 MHz, and a 25 MHz signal generated from the RF signal generator were then connected to the inputs of the mixer whose output was terminated using a 50 Ohms terminator. Surprisingly, there was a significant rise in current consumption of the circuit from 43 mA to 200 mA when the mixer was connected. This error was due to the presence of unwanted DC component (approximately 4 volts) at the output of the prescaler which was the input for the mixer.

4. To remove this unwanted DC component, a high pass filter with cut off frequency of 25 MHz was introduced at the output of the prescaler, thus only allowing signal with frequency higher than or equal to 25 MHz pass through to the mixer. The introduction of this high pass filter stabilized the current consumption to 43 mA.

5. Finally, the loop filter was introduced to the loop and the output of this loop filter was used to tune the VCO. The loop used in the test used an inverted buffer as a result of which a negative voltage (V_{cc} = -15 Volts) was applied at the VCC of the loop filter. When the loop was not locked, the output of the loop filter was adjusted using the trimmer on the PCB so as to get the required tuning voltage for the VCO, which was around 12 Volts. The loop filter PCB introduced in the loop has been shown in appendix 3. [11]

The reference frequency was set to 25 MHz and the output of the VCO was fed back through the prescaler. The output of the VCO was analyzed with the spectrum analyzer.

The input frequency was gradually increased by a factor of 100 KHz and at the output corresponding amplification as a factor of 40 could be clearly seen, as N was set to 40. Figure 23 shows the variation of the output frequency with respect to the reference frequency.

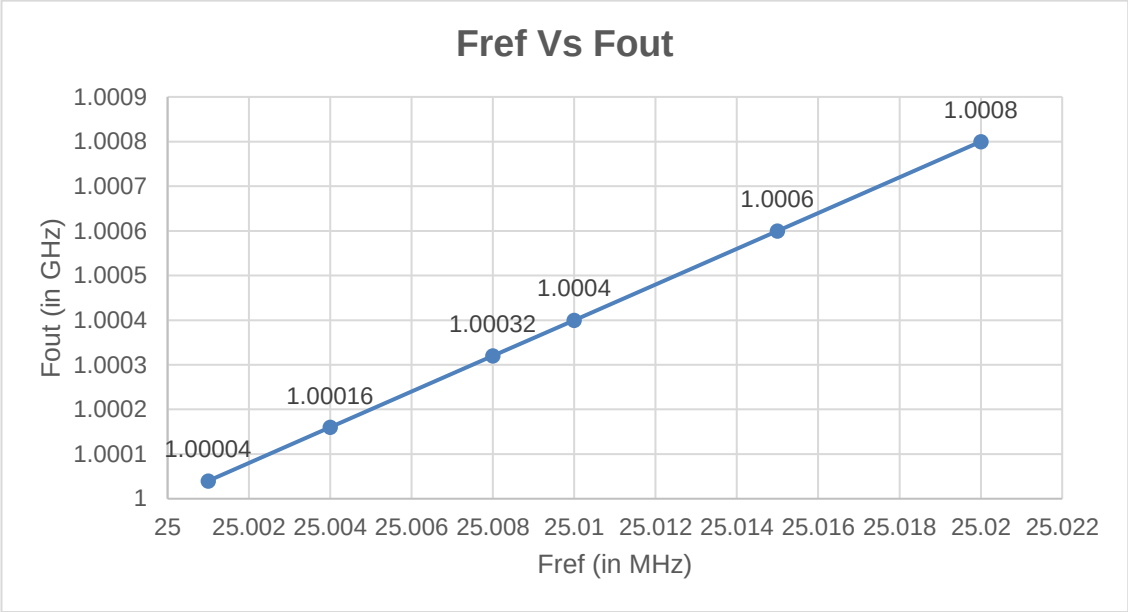

Figure 23. Output frequency vs reference frequency at PLL lock.

Similar process was followed to test the PLL at another reference frequency, 28.5 MHz. For this the trimmer was adjusted so that the loop filter generated 14.39 Volts to tune the VCO to generate 1140 MHz signal. The PLL locked at this frequency too. The input and output when the PLL is locked has been shown in appendix 4.

6 Discussion and Conclusion

On completion of this project, a fully functioning prescaler PCB was designed and successfully implemented with other components to form a phase locked loop. The prescaler was able to perform frequency division by all the factors which were set as a target during the beginning of the project. With its implementation, a phase locked loop which locked at two different frequencies 25 MHz and 28.5 MHz was created. Because of the programmable nature of the prescaler, or in other words, because of the four different division factors of the PLL, a wide range of frequencies can be generated at the output. This

PLL can also be used to generate high frequency signals from low reference frequencies, thus offering plenty of applications. In other words, a phase locked oscillator which oscillates at a higher frequency with reference to a lower frequency local oscillator can be designed based on this implementation.

However, there is still room for improvement for the design of the prescaler and overall PLL. Because of the presence of the DC component at output, a high pass filter with offset 25 MHz had to be introduced. This limits the range of the reference frequency that can be applied as this PLL block with the high pass filter cannot be used at frequencies lower than 25 MHz without changing the high pass filter. Thus various analysis have to be done to find an appropriate high pass filter or the PCB should be designed with a DC blocking module which will still allow the PLL and the prescaler to operate at lower frequencies. In addition to this, the lock range and capture range of the PLL needs to be determined as well.

Another possible concern could be the range of the prescaler. The range of the prescaler is 100 MHz to 1.1 GHz, even 1.2 GHz as the prescaler functioned properly till this frequency. It should be tested, if it is possible to design a prescaler PCB which involves a module whose range can be higher than 1.1 GHz or even more. Then the VCO can be used to generate higher frequency signals that can be fed to the prescaler. This will enable to operate the PLL at higher reference input frequencies.

Hence, it can be concluded that in spite of the room for improvement, the designed prescaler PCB functioned properly and was successfully implemented to create a well-functioning phase locked loop and a phase locked oscillator.

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Measurement Setup

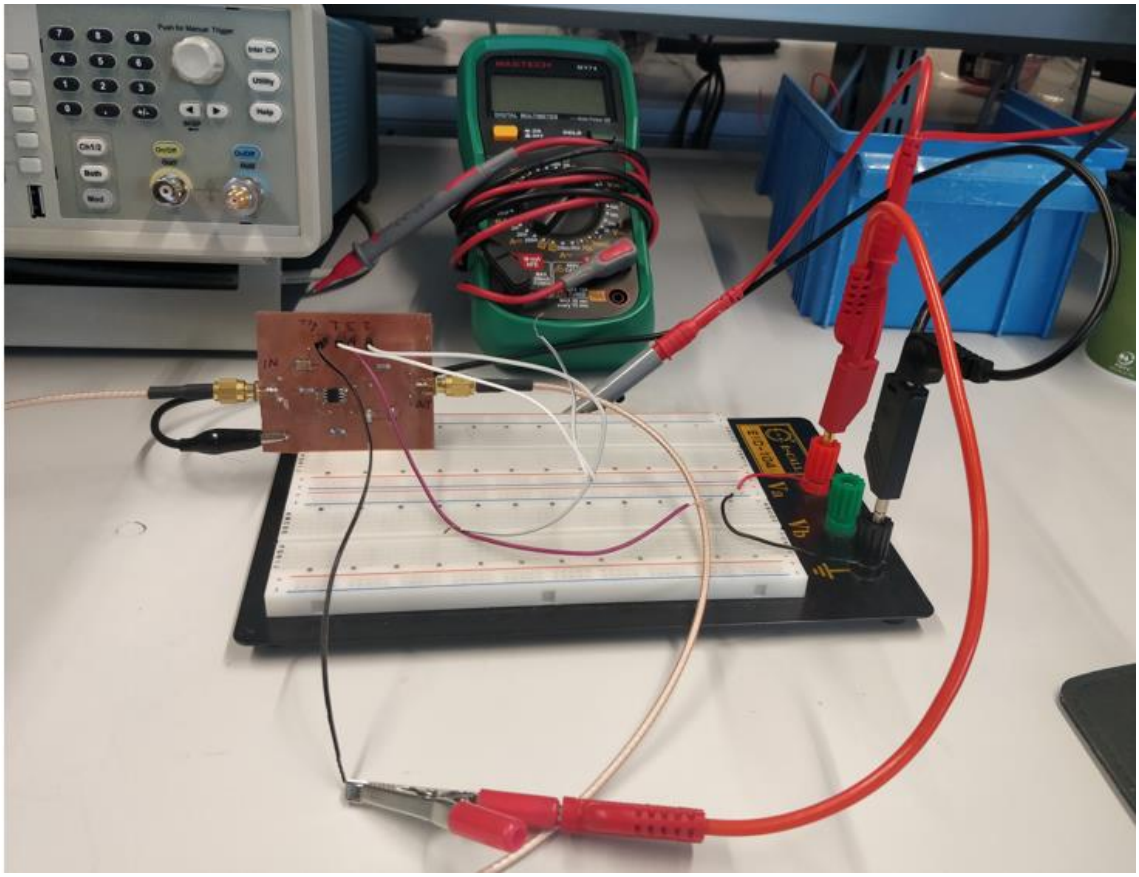

Figure 24. Measurement setup for testing prescaler circuit.

Verification of frequency division

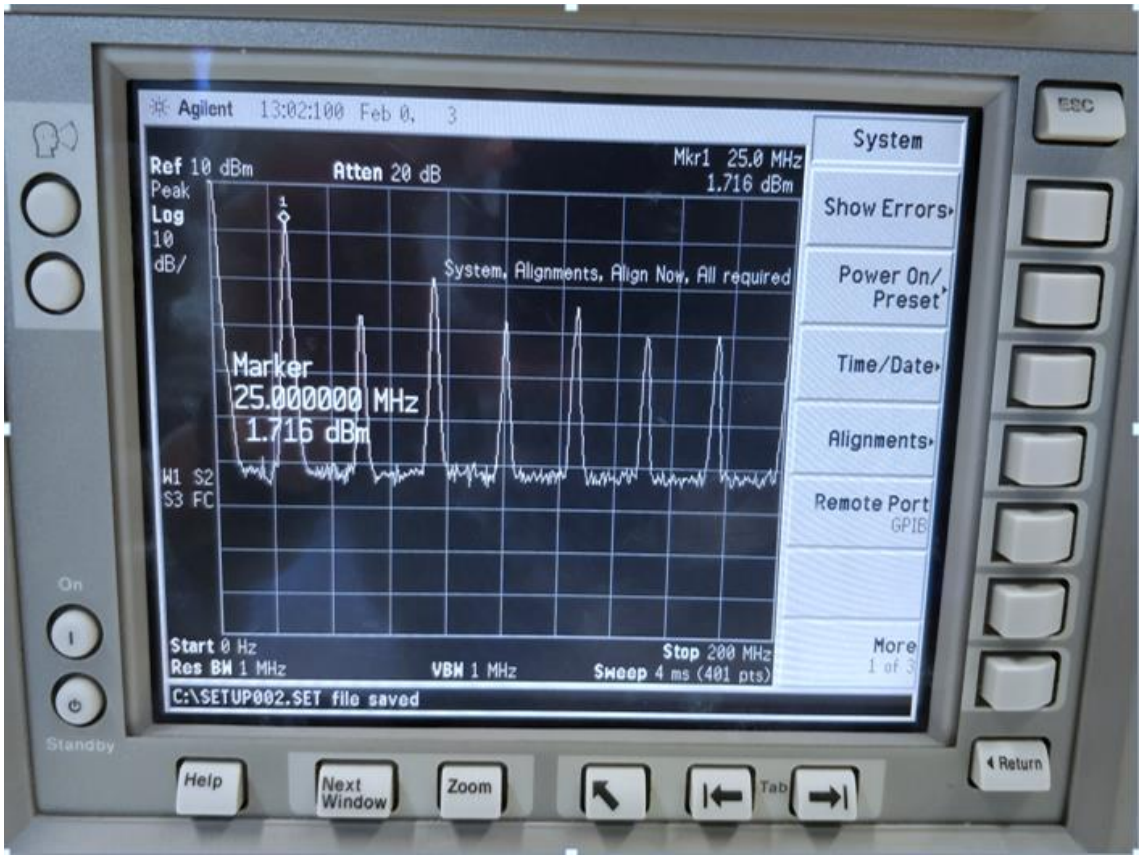

Figure 25. Frequency division and different harmonics of the output signal at N=40.

Loop filter

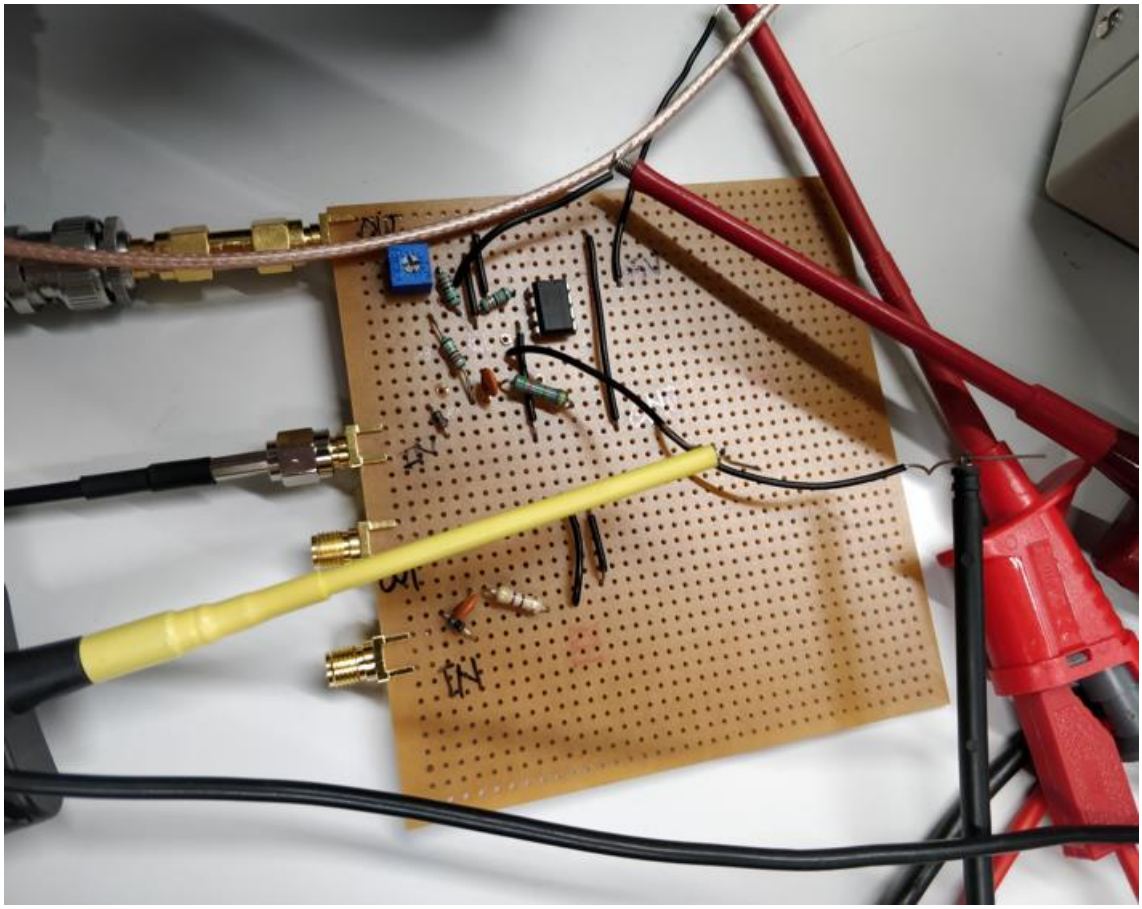

Figure 26. Loop filter used in the PLL, copied from The Impact of Loop Filter in Phase Locked Loop. [11]

Loop locked state at 25.013 MHz

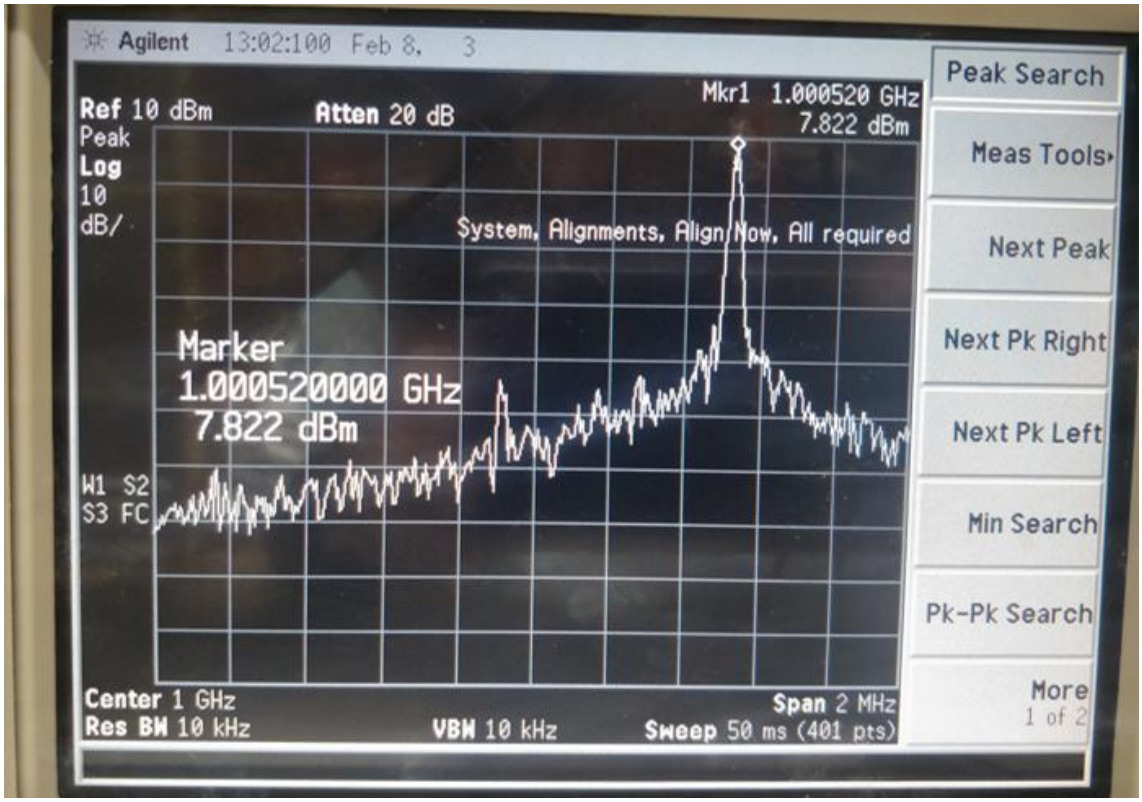

Figure 27. Output in locked state.