



Andre Pruunsild

Module Tester First Pass Yield Improvement

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Abstract

Author: Andre Pruunsild
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Anssi Ikonen, Head of Degree Programme

Production testing is a vital part in development and testing automation directly affects the efficiency and coverage of the testing and the accuracy of the test results. High first pass yield (FPY) of testing implies that the quality of test equipment and production methods are excellent, and this project aimed to improve the testing equipment to raise the FPY and so the quality of testers in the case company.

In order to make the testing equipment more reliable, a method needs to be developed to analyse the results and locate the issues with the testing equipment or other components of the development process. In this final year project available methods were used, and some new ones were created to simplify the analysis process and increase the accuracy of testing process.

Since the production testing consists of various hardware and software components, it was found that depending on the case, different parts may have problems. These problems were successfully addressed.

The improvement of the test equipment was found to be an infinite process and the results further confirm that tester's development helps to reduce the amount of wasted recourses of the case company.

Keywords: FPY, testing, LabView, tester, TestStand

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Appendix 1: DRO module report example

List of Abbreviations

CPS:	Central Processing Unit with Serial Links
DAQ:	Data acquisition system
DMM:	Digital Multimeter
DRO:	Digital Relay Output module
DUT:	Device Under Test
EMD:	Electrical Middle Distance
FPY:	First Pass Yield
GPS:	Global Positioning System
Ltd.:	Limited
MVB:	Multifunction Vehicle Bus
NI:	National Instruments
PC:	Personal computer
PoE:	Power over Ethernet
SCC:	Serial Communication Controller
USB:	Universal Serial Bus
UUT:	Unit Under Test
VI:	Virtual Instrument

1 Introduction

Many modern hardware and software development companies are using automated testing at least partially to benefit from efficiency, higher test coverage and effectiveness. Automated testing is crucial in decreasing development costs, which makes constant improvement of automated testing process important. An excellent way to evaluate testing effectiveness is test first pass yield (FPY), which, through detailed reporting, can reveal troubled parts of testing equipment or software. This final year project focused on the test FPY of the case company.

The case company is EKE-Electronics Ltd., whose strategy is focused on providing technologies for efficient train manufacturing and operations. Although product testing and testing process development is fundamental in the case company, not all the currently produced modules' test first pass meets the company's standards. Current module tester results are influenced primarily by the module under test itself; the user testing the module and the module tester with the test programs. Improvement of FPY and finding the weaknesses in module testers is crucial in improving the effectiveness of product development in the case company.

The purpose of this project was to identify the issues in the module testers and attempt to increase the reliability of the module testers. The goal was for the module testers to evaluate the modules always in the same way, thus increasing the test first pass yield. This thesis describes the actions taken to increase the module testers' capability and to raise the test FPY of products, that are perfectly functional.

2 Product Development

This chapter handles the questions about product development and electronics testing. It also examines the test results statistics, application of first pass yield tactics and expected results of increasing the test FPY.

2.1 Product Development Process

There are different approaches to develop products and companies implement the suitable method. Product development processes define the operations and outcomes that are needed to be completed at particular points in the product development. Planning, scheduling, and checking the development is done by using the processes and they are usually represented by a broadly described tasks. In the 1980s, a few studies were completed only to find that the heads of companies believed the success is hiding in new products, especially developing innovative solutions, and using the companies' internal resources effectively for new product growth. In a study by Hopkins [1], 63 percent of managers felt that their new product success rate was "disappointing" or "unacceptably low" [2]. This encouraged specialists to introduce a system for product development process and by the 1990s, different systems emerged.

One of these systems is a stage-gate system, which was introduced by Robert Cooper in 1990. The research by Cooper [2] showed, that new products need to be developed instead of extensions and incremental improvements of old ones.

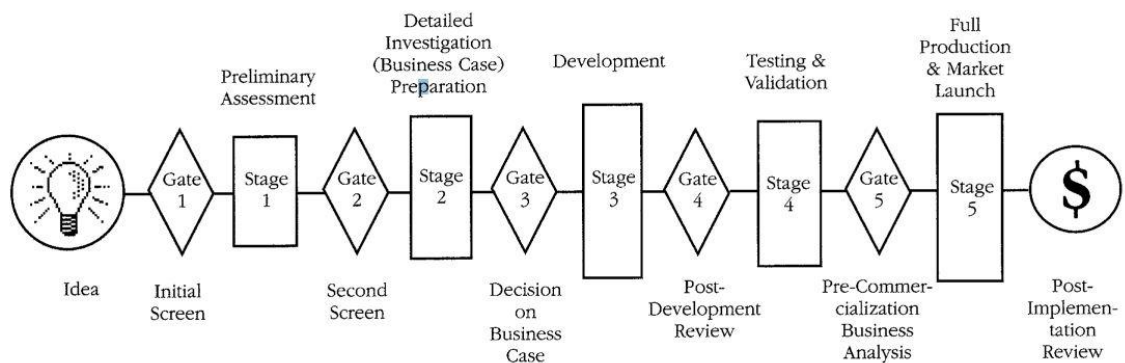
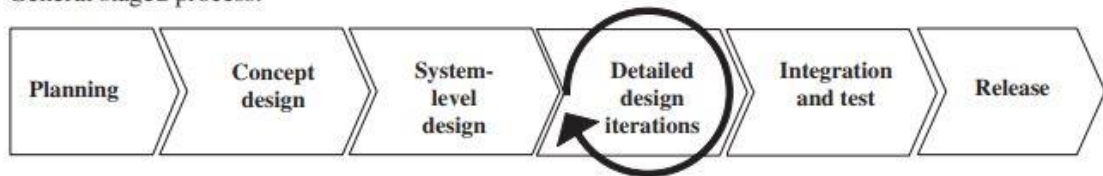


Figure 1. Robert Cooper's Stage-Gate System. [2,2]

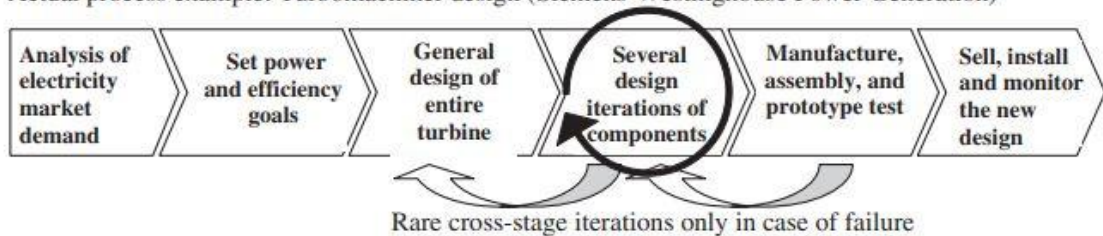
A major electrical/electronics corporation recently undertook a study of the innovation process within its roughly 50 operating divisions. The results were conclusive: Only a handful of the divisions had implemented stage-gate systems, but those few were achieving a much higher level of new product performance than those divisions that lacked a formal game plan. [2,2.] Cooper

implied that by using stage-gate system, product development becomes a process and like any other process, it can be managed, and this is done by applying process-management methodologies to this innovation process. Stage-gate system can be divided into a number of stages or work stations as can be seen in figure 1. Between these are quality control steps or gates. This workflow shows that the stages are where the actual work in the product is done, and gates are for analysing the quality. Staged processes are suitable in product developments when the product definitions are stable, product cycles use well-known technologies and have high quality standard. This is often the case for product updates according to D. Unger and S. Eppinger [3]. Once a stage is complete, it is generally difficult or expensive to go back. However, companies sometimes must revisit design issues from previous stages. [3,3.]

General staged process:



Actual process example: Turbomachiner design (Siemens-Westinghouse Power Generation)



Defining characteristics:

- **Reviews:** Strict, checklist-style design reviews before a new stage can begin
- **Iterations:** Iterations within some stages are normal, but cross-phase iterations are an unusual sign of trouble
- Freezes most design specifications early to avoid rework and design changes

Figure 2. Staged product development processes. [3,3]

Unger and Eppinger [3] analysed the process and practice of Siemens-Westinghouse Power Generation and found that in the company, the staged process is adjusted for cross-phase (in contrary to internal) iteration of serious problems or failure. This is illustrated in figure 2. These steps to the previous

stage are uncommon, but possible. The first part of figure 2 shows the general nature of staged development process in contrast to the second part which presents stepping backwards. Staged processes might leave companies open to market risk, for example if a product is developed with perfect design specifications but it is found out from prototypes or market research that these specifications missed did not meet evolving market demands. This design problem is discovered near the end of the process which makes corrections complicated or impossible. The issues with staged product development processes lead companies to develop other strategies. One of these is a spiral process model (figure 3 (b)) which in contrast to the staged process is flexible and anticipates feedback. The spiral process includes a series of planned iterations that provide feedback and stretch over multiple phases of development process.

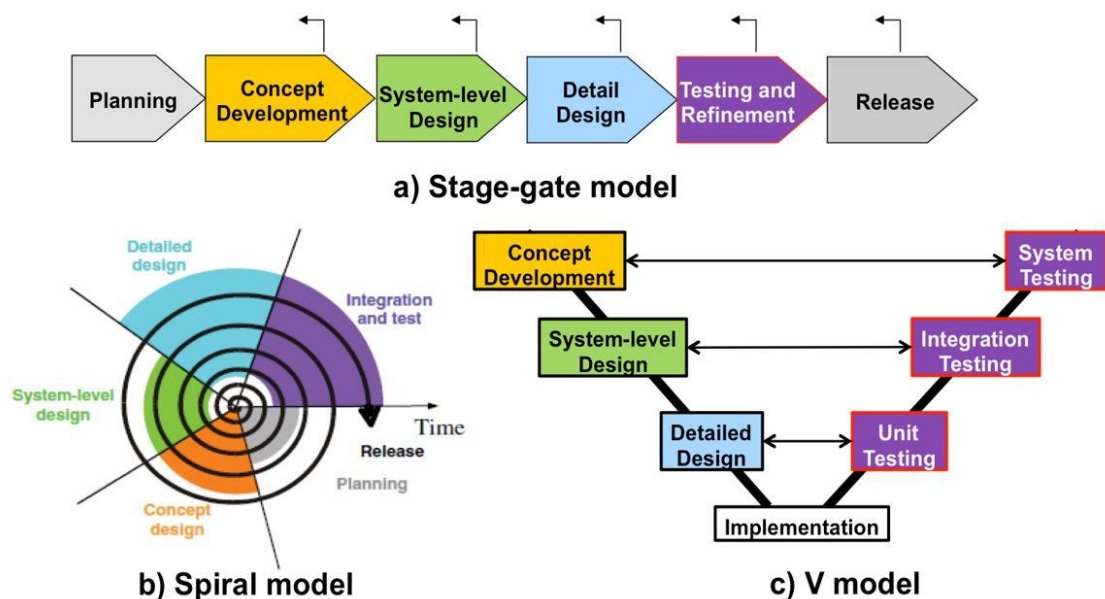


Figure 3. Models of product development process. [4,2]

Unger and Eppinger [3,4] explain that the spiral process model repeats the steps, including concept development, system level design, detailed design, and integration and testing. It is clearly less problematic and expensive to rework the design which lowers the development time and cost. The spiral model holds several disadvantages. For example, its complexity requires considerable management attention, it can lead to delays in developing

complex subsystems and it can just be too complicated for projects that could use a simple staged process.

Figure 3 shows another model of product development process, the V model [5,2] (figure 3 (c)). The figure of the V model displays the connection between each step of the product development and its linked phase of testing. Design and testing are both ordered activities in time sequence, which complement one another across the 'V'. [4,2.] It is clear even from the shape of the model, that testing is left to the end of the process.

2.2 Product Testing

Product testing, also called consumer testing or comparative testing, is a process of measuring the properties or performance of products [6]. The purpose of the testing is to locate as many inaccuracies of a product as possible as early in the development or construction stage as possible. Testing process should always advance simultaneously with all the product development stages so that defects and errors would be discovered early, therefore avoiding doing same work repeatedly. In most cases, very exact functional and technical specifications are used in product testing, testing without these is impossible since it would be unknown how the product should function.

Even though testing is emphasized to be an important part of product development by research and actual work done by companies, in intellectual literature testing is considered to have specific techniques that only detail the methods, practices and equipment for tests or how to set up or improve a test. In design research, an example of this is Engel's book [7], which is considered to be the first book to focus specifically on engineering systems. According to Engel [7,4], the engineering systems of the manufacturing industry consist of a range of components, machines, technologies, and people instead of simple separate products. Engel [7] discusses the importance and methods of systems' verification, validation, and testing, seeking to answer questions like what should be tested, how should one test, when should one test, and, when should one stop testing?

Automation is a process or procedure that uses a program of instructions with a control system that executes the instructions instead of using human assistance. Automation is the application of mechanical, electronic, and computer-based systems to operate and to control manufacturing. [8,75-78.] Automated testing uses scripted sequences that are executed by testing tools. The testing may be semi-automatic, where a user is involved during some part of the testing process (in the case company this is the case with module tests that require reconnecting cables and adapters).

Two types of automated hardware testing are used: product validation and manufacturing test. The purpose of product validation is to determine that the design of the product meets its requirements. This type of testing is executed in an early stage of design development, cycling through various provocations like input voltage limits or load limits and environmental aspects like temperature and humidity, to determine how the design will function when the product is commercialised. These devices are often handled to the point of failure and are not intended to be put on market. In contrast, manufacturing test is used to verify that the device passes a subset of key specifications before it is shipped out of the factory, it is often the closing step of the manufacturing process. This thesis discusses the latter form of product testing.

2.3 First Pass Yield

First pass yield is an important analysis tool of production and testing. FPY presents the quality and efficiency of the process and quantity of loss or ineffective work. However, it does not display information about the inactive time of the process or schedule of the production or testing. In addition, FPY offers a great overview of work that is done more than once for example due to a mistake in the process or poor quality of the supply. This figure specifically expresses the proportion of finished devices that pass inspection during product testing, which means that the higher the FPY, the more reliable and consistent is the process. FPY is usually measured for a certain period or output, such as batch or order.

The first pass yield calculation is defined as the quantity of modules passed on the first test attempt divided by the total quantity of modules tested. The figure is usually displayed as a percentage. For example, if 100 modules are tested and 96 of them pass the testing on the first try, the FPY is 96%. The remaining four must be tested again which results in wasted time.

2.4 First Pass Yield Improvement

There are different reasons for a module to fail testing, this final year project considered only the testing process's portion of these. First, maintaining a practical statistics overview is essential to keep up with test results and problematic elements of testing. Second, having clear boundaries of FPY which note the spot at which an action needs to be taken are needed. Third, a plan of processes that are required to be handled must be established. This project aimed to provide all these improvement points for the case company's module testing.

3 Module Tester's Introduction

This chapter will describe the module testers used in the case company. In addition to the hardware side of the module tester, the software of the tests is also explored.

3.1 Module Tester's Physical Components

The case company's module tester is composed of multiple elements which are all essential to secure a successful testing procedure. Figure 4 displays a typical automated test system.



Figure 4. An example of a test system. [9]

First, there is a rack where the DUT and master module are inserted. The rack for modules can also hold other components needed for testing, for example a slot address adapter that was also used in this final year project. Second, to execute the analysis, there are different output devices that are used in the module tester to simulate various conditions the module is intended to experience. These instruments include a relay matrix, analog output and electronic load, among others. Third, power supply is present. Finally, there is a PC that holds all the programs used for testing. The PC is also used to send and receive commands to the module under test or the master module thus acting as a measuring device since expected test results are stored on the computer or in databases. A block diagram of the module tester used in the case company is displayed in figure 5.

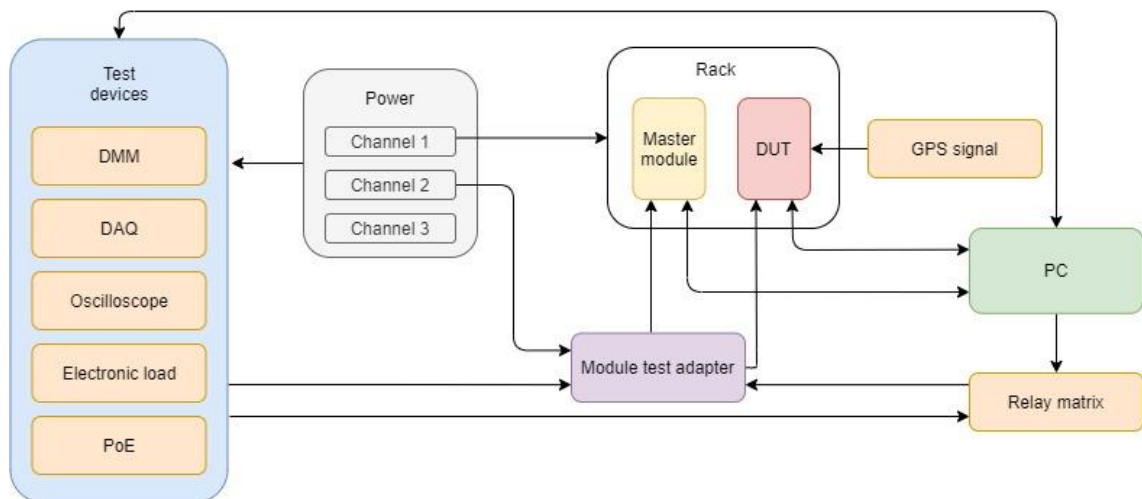


Figure 5. Case company's module tester's structure.

Module test adapter is needed to analyse needed characteristics of the module since each tested module has different functionalities and physical aspects, i.e., connectors. Master module is a device in the system that is able to view and communicate with DUT even without direct connection between the user and DUT. A system ready to be delivered to the customer uses this capability to function properly and efficiently and for this reason a master module is needed when testing modules. The testing process also includes different cables to be used. There are some modules that support GPS functionality, for this reason a GPS antenna can be connected to the DUT.

There are devices on the module tester that are used with every module's test, these include power, rack with master module and PC. These are essential to confirm the basic functionality of every module that has been developed by the case company. However, in most instances, also other components of the module tester are used.

3.2 TestStand Sequences

NI TestStand is a sequencing software that enables developers to create test applications. An example of a test sequence is displayed in figure 6.

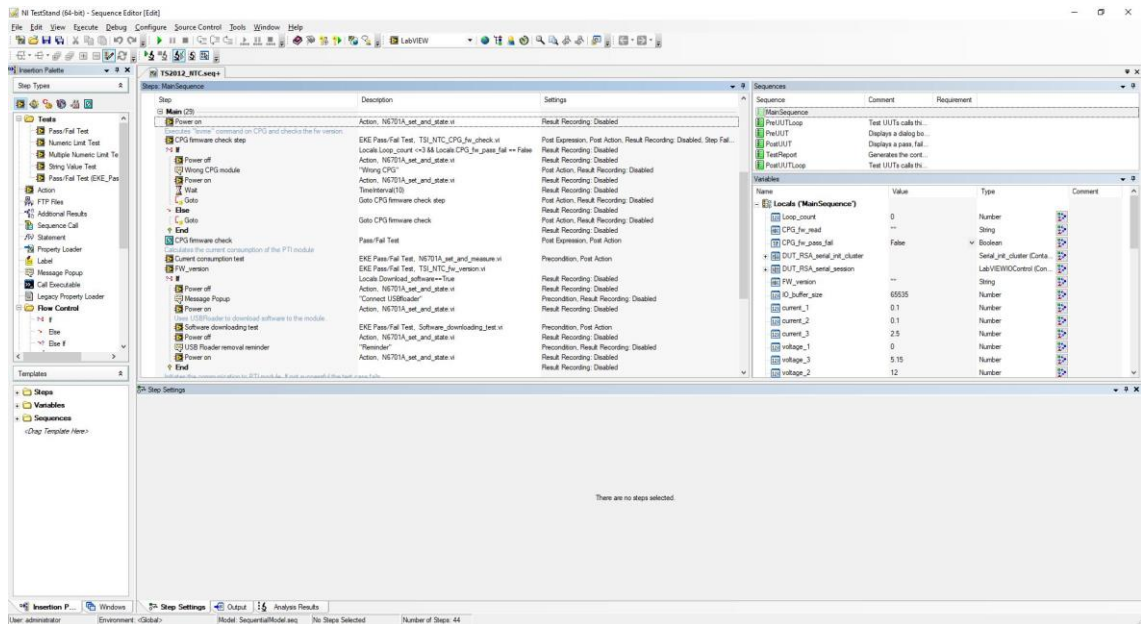


Figure 6. A TestStand sequence composed of different steps.

TestStand sequences consist of steps that are easy to implement into entire automatic tests. These steps can be any logic or action functions, which in turn can be programmed to operate in predefined way. TestStand has built-in functionality to adjust speed and use parallelism, in the case company, the database logging and reporting functions are implemented. The program provides connectivity to other systems and code modules that are used to build the sequence can be written in any programming language. In the case company's current module tester, these action steps are written using LabVIEW.

3.3 LabVIEW Programs

LabVIEW is a graphical programming software that enables users to design programs, or VIs in LabVIEW. The visualization aspect of LabVIEW makes it a lot simpler to design needed applications than regular text-based programming languages. LabVIEW uses class library interface with different functions which have inputs and outputs. The user drops these functions and wires inputs to outputs to determine the functionality. Figure 7 displays an example of a LabVIEW code.

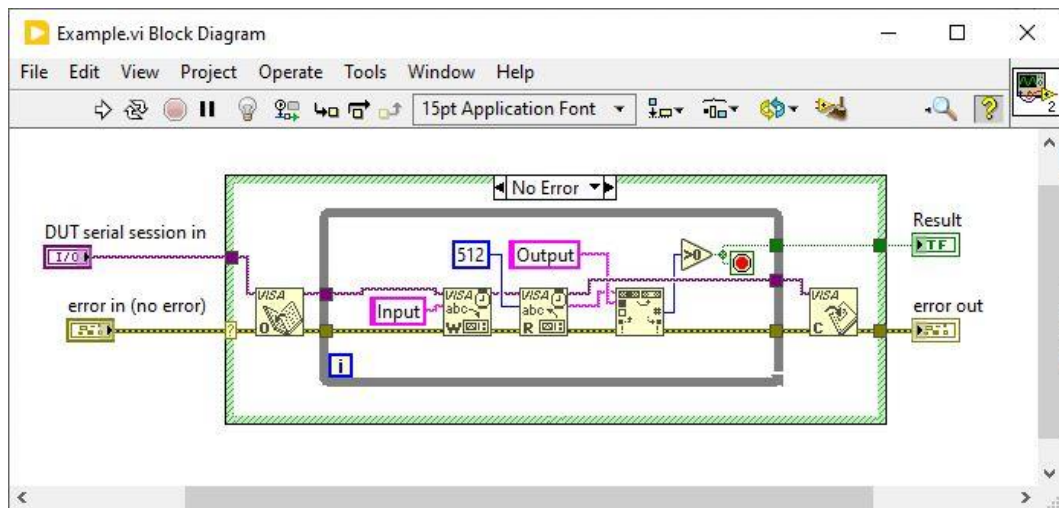


Figure 7. An example of a LabVIEW program.

LabVIEW is used in the case company as a way to communicate with the DUT or the master module of the module tester. In most cases, a serial connection is opened to the device under test, or the master module and commands are sent to and received from the module using programs that have been created using LabVIEW. Thanks to its versatility, LabVIEW is used to connect the module and module tester's output devices in a parallel manner to test different features, it is possible to control the module tester's devices using the drivers that come with LabVIEW and to meet all the testing criteria the DUT has received.

Since the test sequences are composed of LabVIEW programs, these programs determine if the step is passed or failed. This procedure of confirming or rejecting any values or answers given by the DUT are analysed in the LabVIEW program and therefore there must be an action in the program that compares the result received from the DUT to the expected result. In the case company, these expected results are recorded in databases and are imported to the specific LabVIEW program using the sequence of each individual module.

4 Module Test Analysis

This chapter describes the statistics of the first-time module test results. The criteria for selecting the modules to improve the FPY is also defined in this chapter.

4.1 Test result Statistics

In the case company, as in any modern hardware development company, the test results are collected into a report, which includes different information depending on the device under test. The report shows the results of different test steps in the sequence, usually including more information than just pass or fail status of the test, as shown in appendix 1. To pass the test, a module needs to pass all the steps in the test, failure of a test step causes failure of the whole test. The reports are specific for every module and are identified by module's serial number. Production testers' module test reports are uploaded to a cloud-based hosting service, and a statistics generator tool is used to view the first pass yield of each module. An example of the statistics is displayed in figure 8.

Production testers statistics for DRO2342A

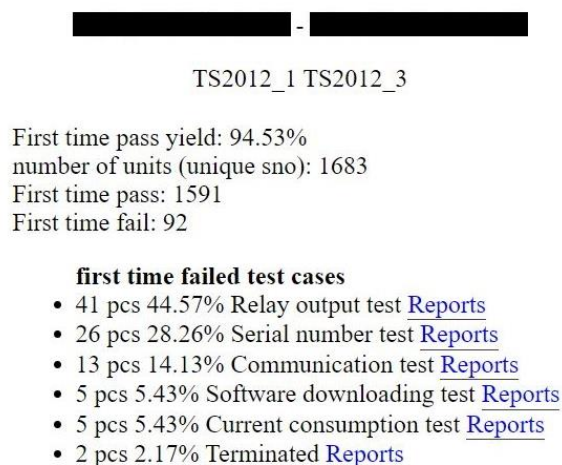


Figure 8. Production testers statistics for DRO module

The statistics tool also generates a Pareto Chart of the module's FPY. An example of the chart can be seen in figure 9. This chart displays data from

figure 8 and presents the frequency of failure of the test case (left vertical axis) and cumulative percentage of the total number of occurrences (right vertical axis), latter showing the percentage of pass test result received if issues on the left would be resolved.

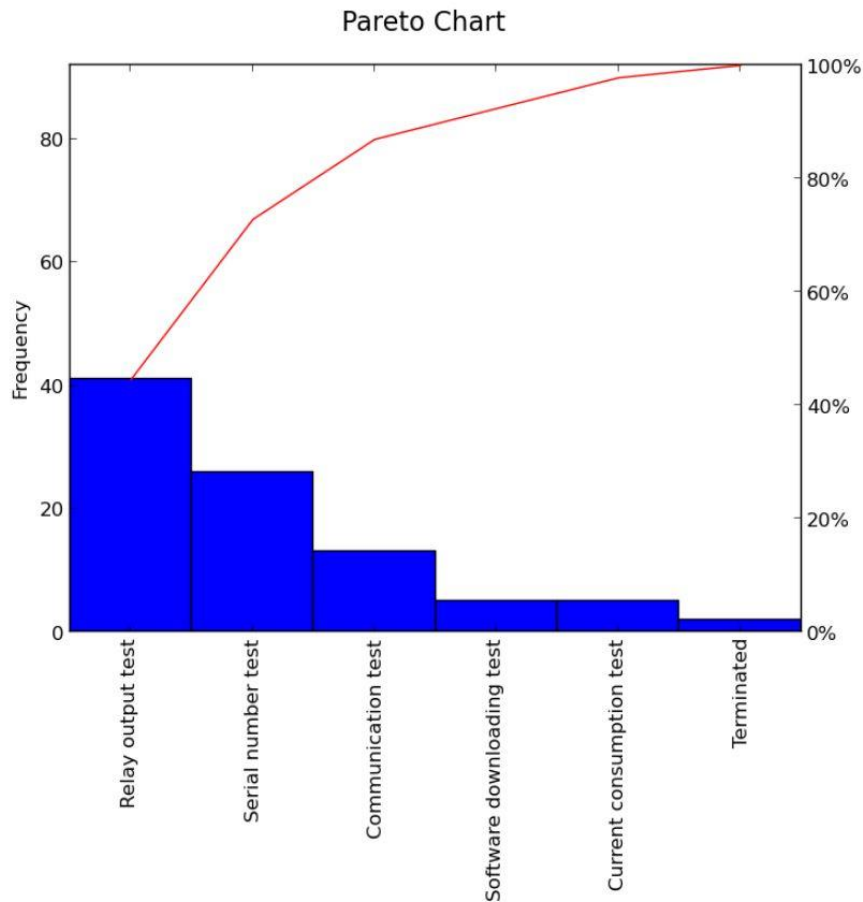


Figure 9. Pareto chart of DRO module's production testers statistics

The chart only displays the failed test results and the percentage of each test case that has been the reason for failure. This DRO module testing statistics cover a predefined period of testing and reveal that FPY for this module in this time interval is 94.53%. The statistics expose all the test cases that have caused the failure of the test sequence and define, which cases need to be revised to raise the FPY.

4.2 Module Selection

This final year project analyses the module test result statistics of the predefined period, which will not be disclosed on the uploaded version of the thesis. To get as objective results as possible, only modules, that had at least 100 units tested with first pass yield lower than 95% from this period, were selected to the project. Also, from all the test results, the test cases were observed: out of first-time failed test results, all the test cases that contributed with more than ten percent to these results were included in the project. This means that taking DRO module test statistics (figure 8) into account, Relay output test, Serial number test and Communication test cases were chosen to be improved. Overall, during that period, 56 different modules were tested, and tens of thousands of tests were conducted. There were several modules that fulfilled the criteria to be included and two of these were determined to be held in the project.

5 Process of Improving the Tests

This chapter inspects the test results as well as includes the description of different methods that are available to be used to improve the module testers' reliability thus increasing testing first pass yield and it also describes the practices applied in this project.

5.1 Test Results Analysis

In order to improve the tests, the results need to be examined. Determining problematic parts in the test is based on the statistical analysis, which can be conducted in several steps. First, it is important to establish, which tests are the most critical failures and prioritize these. The greater amount of time spent on testing failed modules, the more important it is to improve the module test. This can be expressed as the largest amount of modules times the highest probability to fail the test equals largest loss to the company. Higher priority should also be on the tests, which if passed, would present the most advantage and those with less benefits could be worked with later. This prioritising enables

to employ limited resources efficiently and balance the workload between developers and test personnel. Second, identifying if the cause of the test failure is the module tester with test programs, the production process, or the design of the product. Different approaches are suitable for different problems. In case the module tester is at fault, the tests with the module tester need to be modified, production mistakes require better construction guidance and if the product design is responsible, a new version of the device needs to be developed.

5.2 Methods of Improvement

Since the purpose was to improve the reliability of the module testers hence raising the test FPY, different approaches of improvement were taken into consideration. As it was already mentioned, this project focuses on resolving the testing issues that have been caused by the module tester. These issues include physical test equipment for example measurement cables and adapters or malfunctioning measure devices. However, test software is required to be analysed and improved if needed as well. The decision, which component needs to be reworked was based on the results of examination of the test reports.

First, physical practices to improve testing FPY include reconstructing or replacing the test equipment. It is clear that testing equipment can be the cause for the failure of the test. The measurements read from the device under test can be affected by worn out cables or measuring devices that are not properly functioning. Since testers can be composed of multiple different components and numerous measurement devices can be in use, detecting the cause of malfunctioning device can be problematic. For this project, measuring devices were analysed and testing cables were produced.

Second, the user might be the cause of failure in some instances. The tests require different measurement equipment to be connected to the module tester and if this is done incorrectly, the TestStand sequence fails. A procedure to counteract this behaviour was required to be developed and this was to add a

second or more chances to run a step in the sequence displaying a notification to the user. This notification was to describe the encountered issue and a solution, also a picture with guidance to connect the test system or DUT to the module tester was decided to be added where needed. An example of a notification is displayed in figure 10.

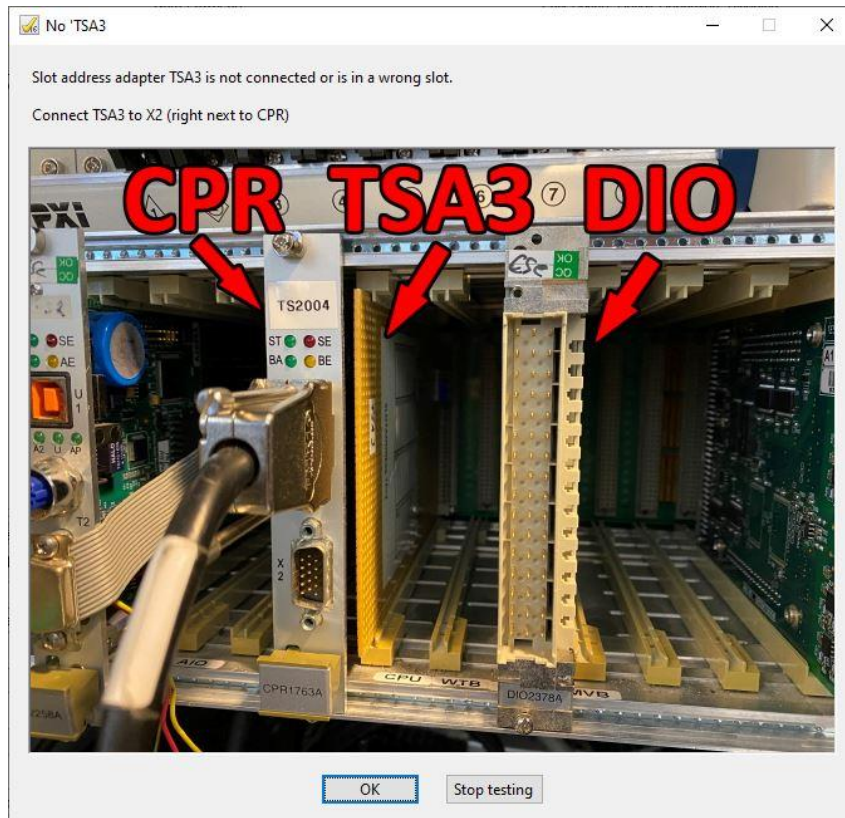


Figure 10. A notification aiding user to make the connections correctly.

The purpose of the notification was to eliminate the feature of the sequence that will cause the immediate failure of the test if the user has inaccurately connected the test equipment. In most cases, the power of the module tester was turned off after the failure of the step, before displaying the notification to the user. This behaviour was implemented to allow the user to replace the test equipment or to adjust the testing setup otherwise. The power of the module tester was turned on should the user have chosen to continue the test with repeating the last failed step. These improvements to the sequence were created to be run several times, should the problem remain or should another problem occur during the test step.

Furthermore, the parts of the whole test i.e., LabVIEW programs, could have been improved. The improvement was thought to have been conducted in several different ways, depending on the test step. Tests usually include communication with the DUT whether directly or using the module tester's master module. This communication commonly involves sending commands and receiving answers from the module and these answers could potentially be long and complicated, making the module delay the answer. If a problem of this nature was discovered during the analysis process, a further testing was concluded. A measure to react to this issue was to add a delay before receiving a response from the module.

Further, more terminals of the LabVIEW programs may have been added. These terminals could be used whether as inputs or outputs and they could significantly improve information flow using the TestStand sequence. Debugging the test using TestStand is far simpler than LabVIEW, this advantage greatly reduces the debugging time. Using the output terminals is also an asset since they can be used to display read out messages from the testing modules to the user. Also, creating an entirely new program was considered as an option. The reasons for a new program could include an updated module that has caused a change in the module's behaviour so that different outcomes of the test could be possible, ones that were not imaginable in the past. The advantage of an entirely new test step includes the fact that the test developer is acquainted with the program, therefore improving, and debugging becomes less complicated.

Finally, analysing the test limits and adjusting these was considered to be an option to improve FPY. Devices under test are supposed to behave in a defined manner and testing the modules include set limits that the results of the test are supposed to land in. The modules are being updated from time to time and with every update, the behaviour of the module changes, which can easily affect the results of the tests. The limits that these results are required to comply with, need to be inspected with every upgrade and updated according to the development testing results. It is also possible that the production method of the

module has changed, and this affects the behaviour of the DUT. All of this must be considered when creating the limits for the test results.

5.3 Improvement Process

The case company's current module tester manages the statistics of testing by creating reports of the test results and uploading them to the cloud. The statistics are generated from uploaded results, which present the first pass yield. This final year project included creating a file which is used to overview these statistics and simplifies the process of improving the test FPY by covering recent information of module testing results and FPY. This document was saved in the company's document managing system and it needs to be updated regularly to notice any change in the results and problematic elements in testing process or module design. For the updating process to be as effortless as possible, a task was created in the company's work management tool, which notifies the statistics handlers to update the data in a period that is adjusted according to the needs.

The specifications to respond were already described in paragraph 4.2: if module test FPY falls under 95%, problematic test cases will be examined. The process of inspecting the statistics is displayed in figure 11.

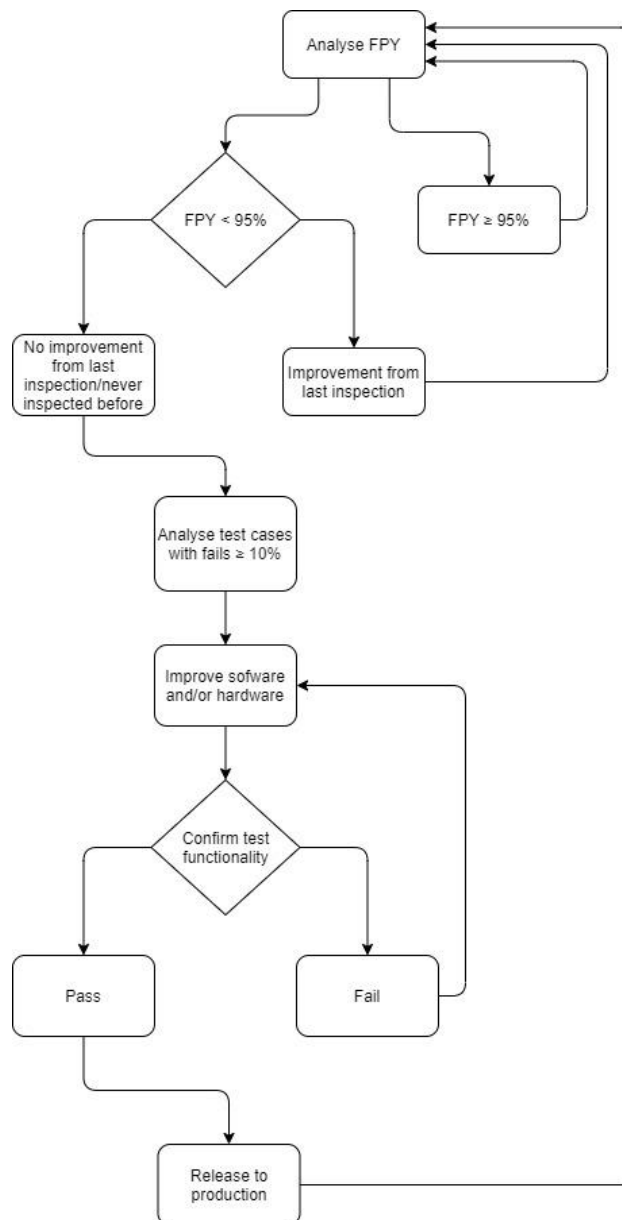


Figure 11. Process of improving module test FPY

The minimum number of units needed to have been tested on given period will be determined on a case-by-case basis, obviously if only one module has been tested and failed on the first try, it could possibly be a problem with the module itself and not with the module tester.

5.4 Procedures to Improve the Test Results

To clarify the work structure, the test result improvement operations are arranged by modules in the following chapter.

5.4.1 MVB Module

First, the Multifunction vehicle bus (MVB) module's test results were analysed. Number of MVB modules tested was 4621 in the period, making it the third most tested module in the time. The FPY of the testing was 87.84% and the detailed results of testing can be seen in figure 12.

Production testers statistics for MVB1820B

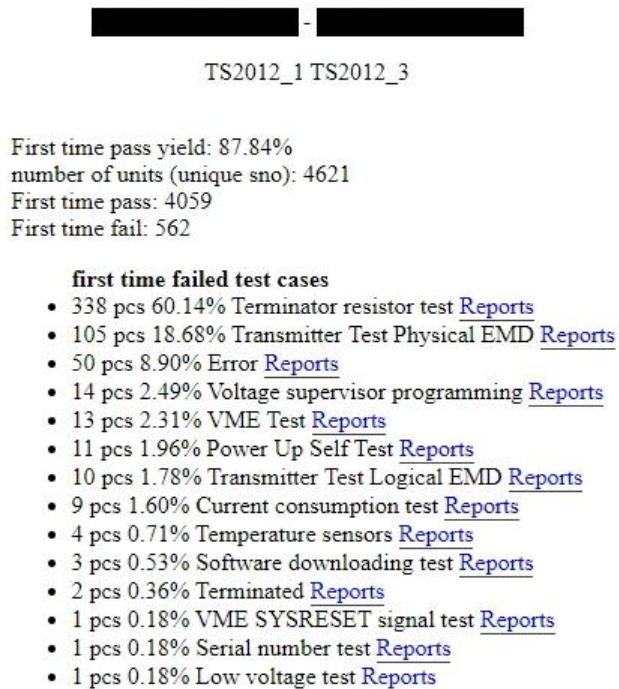


Figure 12. Production testers' statistics for MVB module

Two cases of MVB module test had larger than ten percent contribution to all the failed test steps. First, the Terminator resistor test demonstrates a high failure occurrence compared to other test steps. This test case utilises the tester's matrix switch module to measure the module's electrical middle distance (EMD) termination resistor's resistances. Additionally, it is requested to connect two measuring cables and a terminal resistor measure adapter to the connectors on the module. The measurements are taken between four different pairs of pins on the module's connectors and have limited values and receiving a result outside these values results in failure of the test. Investigating the

reports for this module reveals that there are several reasons for the failure. Some reports disclose that the module has received measurements between some pins, but not all of them. This situation is presented in an extract from a report in figure 13.

Terminator resistor test	
Status:	Failed
Module Time:	2.1401245
Limits: 117;120;117;120;117;120;117;120	
Measured value:	
x1 pin 8-9 117.984 PASS	
x1 pin 6-7 NaN FAIL	
x2 pin 8-9 118.179 PASS	
x2 pin 6-7 117.433 PASS	

Figure 13. Example of MVB module's Terminator resistor test step failure

Additionally, there are several reports showing, that the module receives all the measurement, but one or more of them are out of limits, as illustrated in figure 14.

Terminator resistor test	
Status:	Failed
Module Time:	2.1295406
Limits: 117;120;117;120;117;120;117;120	
Measured value:	
x1 pin 8-9 120.783 FAIL	
x1 pin 6-7 117.831 PASS	
x2 pin 8-9 118.106 PASS	
x2 pin 6-7 117.400 PASS	

Figure 14. Example of MVB module's Terminator resistor test step failure

These two situations might indicate that the issue lays in the module's build quality and the module needs to be examined and reconstructed before testing again but it could also indicate that the resistance is affected by the measurement cables or other equipment. A good solution to improve the test would be to measure voltage instead of easily affected resistance. This procedure involves extended analysis of the measuring equipment and rebuilding the program and will be completed outside this project.

In addition to these instances, there are 38 reports indicating that the module has not received a reading from any of the pins. This situation is illustrated in figure 15.

Terminator resistor test	
Status:	Failed
Module Time:	2.2945099
Limits:	117;120;117;120;117;120;117;120
Measured value:	
x1 pin 8-9	NaN FAIL
x1 pin 6-7	NaN FAIL
x2 pin 8-9	NaN FAIL
x2 pin 6-7	NaN FAIL

Figure 15. Example of MVB module's Terminator resistor test step failure

Clearly this example implies, that the reason for failure is possibly an incorrect connection by the user or damaged measurement cables or adapter. Testing cables and adapters are updated regularly, and the case company's module tester's maintenance plan reveals, that new and tested cables and adapter for MVB module test have been brought into use during the inspected period. Nevertheless, inspecting the test sequence for MVB module test shows, that the user is required to attach this equipment correctly, since improper connection results in immediate failure of the test. Figure 16 displays the test sequence for MVB module's terminator resistor test. It unveils, that immediately after the pass/fail test step, another not related step follows.

Main (26)	
Terminator resistor test	EKE Pass/Fail Test, MVB3275_Terminator resistor test.vi
Adapter removal popup	"Remove TSC15 adapter reminder"
Calculates the combined current consumption of the tester CPG and DUT	
Current consumption test	EKE Pass/Fail Test, N6701A_set_and_measure_2.vi
Power off	Action, N6701A_set_and_state.vi

Figure 16. Example of MVB module's test sequence

As a result, the user does not have a chance to correct the connection and the failure of the module test is reported. This module is tested again resulting in wasted time thus wasted resources for the case company. To overcome this situation, a few steps were added to the sequence: an if statement was added

with an increasing variable followed by a reminder for the user to make sure the connection is correct. Next, a Goto step was added that reruns the Terminator resistor test step after the pop-up. After the if statement ends, another step was added to decide if the test was passed. These edits to the sequence can be seen in figure 17.

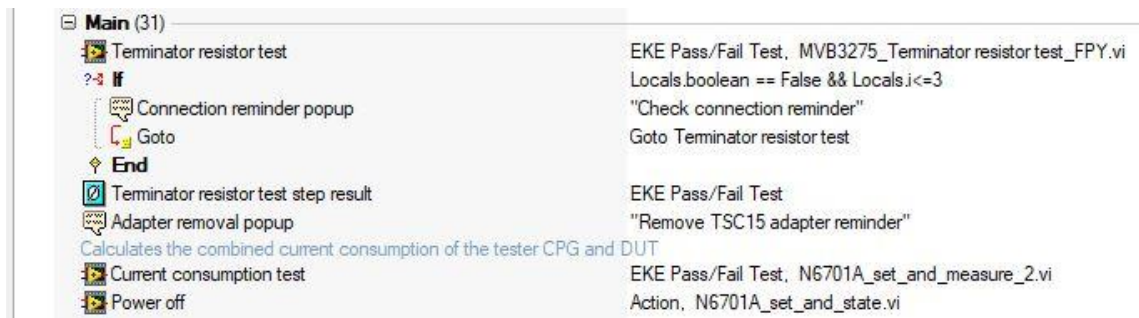


Figure 17. Example of MVB module's test sequence after editing

These changes to the sequence cause the test to prompt the user to confirm the correct connection. This can be done up to three times before the result of the test is decided.

Another test step that had high failure percentage was Transmitter test using physical EMD. This test measures the transmitter signal levels to determine whether the physical characteristics of the transmission lines are functional. Similar to the previous test, module tester's matrix switch module is used; however, the measurements are conducted using module tester's oscilloscope (these components can be viewed from the block diagram of the module tester in figure 5). The test connects required channels using the switch, gives command to DUT and reads a measurement from the oscilloscope. MVB modules' test reports indicate that the reading is always received, but it does not always lay within the limits. In every failed report, one or more channels report too low voltages. An example of a failed Transmitter test with physical EMD test step is displayed in figure 18.

Transmitter Test Physical EMD	
Status:	Failed
Module Time:	5.9442037
Limits: 2000;3300;1500;2900	
Channel A: 2162 mV PASS	
Channel A with load: 1749 mV PASS	
Channel B: 2243 mV PASS	
Channel B with load: 995 mV FAIL	

Figure 18. Example of MVB module's Transmitter test with physical EMD step failure

There can be several reasons for this, for example the transmitter or the oscilloscope could be accurate enough or the cables could interfere with the signals. However, further investigation reveals, that the test personnel has always immediately after failing this test step, tested the module again. Extracts of two different reports can be seen in figure 19. Because the serial number on both of these reports is the same, the module under test has been the same.

UUT Report			UUT Report		
• Station ID:	TS2012_3		• Station ID:	TS2012_3	
• Module ID	MVB1820-B00		• Module ID	MVB1820-B00	
• Serial Number:	619328		• Serial Number:	619328	
• Date:	6. heinäkuuta 2020		• Date:	6. heinäkuuta 2020	
• Time:	8:11:19		• Time:	8:13:37	
• Operator:	JLa		• Operator:	JLa	
• Execution Time:	98.1792788 seconds		• Execution Time:	160.8122128 seconds	
• Number of Results:	10		• Number of Results:	13	
• UUT Result:	Failed		• UUT Result:	Passed	
• Failure Chain:					
Step	Sequence	Sequence File			
Transmitter Test Physical EMD	MainSequence	TS2012_MVB1820B_v2.seq			

Figure 19. Two reports from the same MVB module

These reports have been generated a few minutes apart, which implies that any adjustments to the DUT were not carried out. The module has failed the test step on the first attempt but passed on the second and this occurrence applies to all the randomly selected module reports. This problem was investigated further. Test step was modified so that the delay time between the transmitter's signal change and module's command to read the change can be adjusted and the test was run 100 times with different 0 to 0.5 second periods of delay. The results indicate that the module failed the test for only a few times with very short delays. Half a second is enough for the module to adjust to the signal change and correct reading can be received by the oscilloscope and the step was modified accordingly.

5.4.2 CPS Module

Next, combined number of 4975 Central Processing Unit with Serial Links (CPS) modules were tested during the period, CPS module consist of A and B modifications, difference being that A mod includes a USB port. CPS represents the second most tested module. The details of test statistics for this module can be viewed in figure 20. CPS module combined calculated test FPY was 93.29% and five test steps had over ten percent first time failed part of all the first time failed test steps.

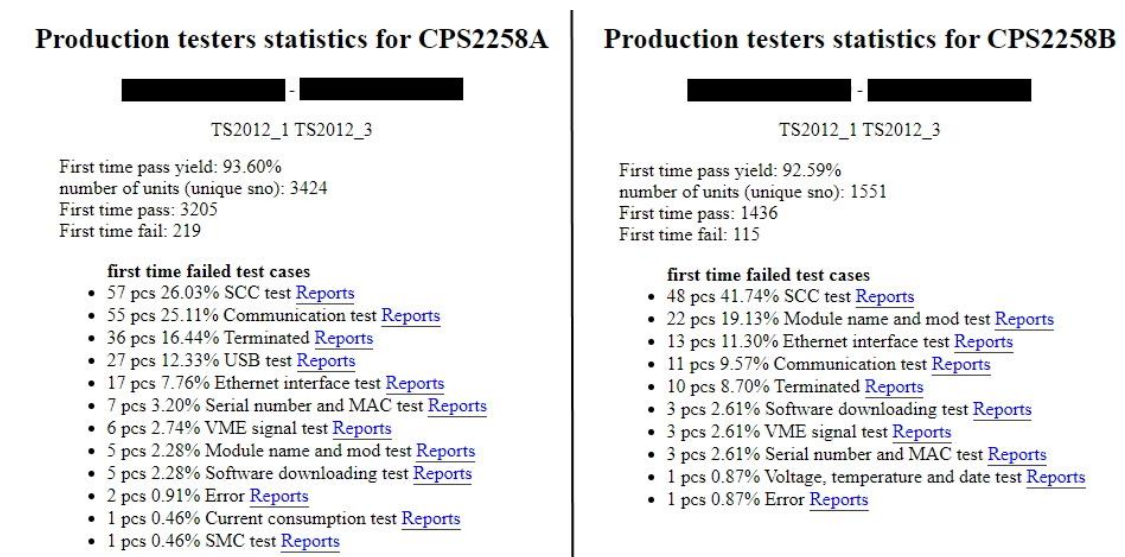


Figure 20. CPS module's test result statistics

First, the Serial communication controller (SCC) test contributes to about a third of the failed test results. The functionality of SCC one, three and four are tested using a test cable between module tester's master module and DUT. During the test, data is sent from DUT to master module one SCC at a time via the SCC cable and the master module replies to the DUT. To succeed in the test, the received data must be correct. Inspecting the reports reveals that in all the instances the data sent back by the DUT was incomplete. Since this information moves from module to module via a cable, it might deteriorate the data in the way or affect the travel speed. As with the MVB module's Transmitter test, a delay of half a second was added before reading the answer from DUT and it was again tested 100 times without the delay. Three different CPS modules

were used but none of these were unsuccessful during the test. CPS module's SCC test will be further examined.

Second, the Communication test was inspected. The communication test also requires the module tester's master module to be connected. A file is created on the DUT and after that it is confirmed that the master module is functional. Inspection of the failed reports revealed that the master module does not boot completely, and this situation was simulated on the test equipment. It was discovered that in these instances, the file on the DUT is not created successfully. In some instances, the test did not identify the DUT, so it was not known if the serial cable was connected to the DUT or if DUT was connected to the module tester at all. Research in the reports revealed that the module was always tested again after Communication test failure without altering the module under test. Example of this is seen in figure 21.

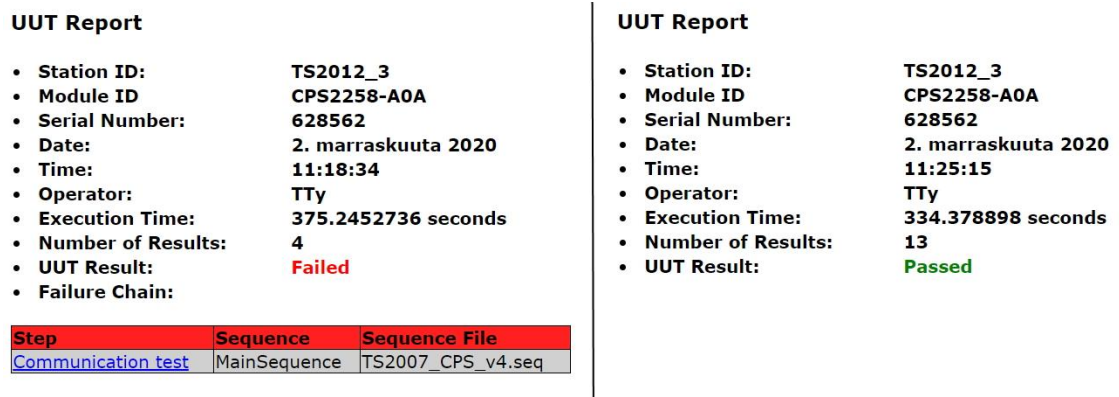


Figure 21. Example of the same CPS module tested twice

This indicates that the connection was revised and the test was run again. All these instances, when DUT had connection problems were corrected using a case structure in the LabVIEW program and a notification in the sequence, allowing the user to correct the issue and attempt the test again.

Third, the reports of modules that failed the Module name and mod test indicate that DUT is not responding to the commands. The test establishes a connection with DUT and checks, that correct module information is written on it. The

reports did not reveal the reason for these issues to occur, but simulating the test indicated a problem that Communication test did not review. CPS module test requires the DUT to be connected to a certain slot for it to function properly. In the Communication test a file is created on DUT and if it is inserted to a wrong slot, the file will make the DUT unresponsive. To combat this issue, Communication test was modified to confirm, that DUT is functioning properly after creating the file.

Next, the Ethernet interface test requires an ethernet cable to be connected between DUT and master module. All the failed reports had identical print and it can be seen in figure 22.

Ethernet interface test	
Status:	Failed
Module Time:	9.4505414
Limits: 1500	
Parameters: 21729297	
ETH0 tester CPG-->DUT transfer rate: 0,00kB/s	
ETH0 DUT-->tester CPG transfer rate: 0,00kB/s	
ifconfig eth0 10.0.0.2	
~ # □[6nftpput -u root -p root 10.0.0.2 ethtestfile /var/opt/ethtestfile	
ftpput: cannot connect to remote host (10.0.0.2): No route to host	
~ # □[6n	

Figure 22. CPS module Ethernet test failure report

This read from the master module clearly indicates that there is no connection established between the modules and the reason for this is most probably a malfunctioning or missing cable. This issue was treated similarly as the USB test problem. USB test requires an USB flash drive to be connected to the DUT's port and measurement cables to the digital multimeter of the module tester. A voltage is measured from the port and after that a file is moved from the drive to DUT and back and its movement is being confirmed. Reports indicate that in all cases, after failed test attempt the module was tested again almost immediately with a positive result, which implies that the connection was corrected rather than the module being malfunctioning. In most cases there was an issue with the measured voltage being too low and in some cases the USB stick was not found. CPS module Ethernet interface test and USB test received a notification to the sequence in case the connection was found improper.

6 Results of the Improvements

In this chapter, a test result statistics comparison between the initial reports and altered tests' reports is examined. The period of the analysis is predefined.

6.1 MVB Module

First the MVB module's test results were compared. In figure 23, the reports' details from period before and after editing of the test sequence can be seen.

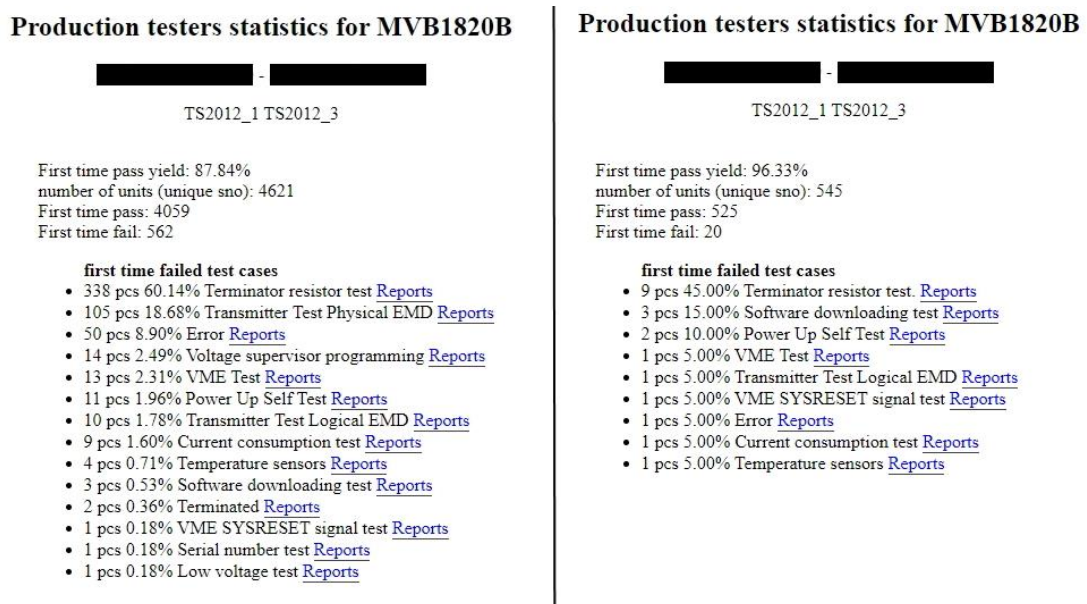


Figure 23. MVB module test statistics comparison

Similar to the original results conclusion, there are first test failed instances of the Terminator resistor test. This implies that the test case needs more extensive analysis and development of MVB test will continue. However, the percentage of the failure has decreased which indicates that the revised test sequence might have been helpful for the test personnel. This can be observed when passed MVB module test reports from period after the test modification are examined. The test took about 130 to 170 seconds to complete before editing the sequence and this time does not change if the connection is correct, but it raises considerably if the user is given a chance to correct the connection

error since making these corrections would take some time. An extract from a report before and after the modification with a passed test result is presented in figure 24.

UUT Report		UUT Report	
• Station ID:	TS2012_3	• Station ID:	TS2012_3
• Module ID	MVB1820-B00	• Module ID	MVB1820-B00
• Serial Number:	609496	• Serial Number:	636729
• Date:	9. maaliskuuta 2020	• Date:	25. toukokuuta 2021
• Time:	12:42:01	• Time:	5:48:19
• Operator:	MLa	• Operator:	TTy
• Execution Time:	167.692132 seconds	• Execution Time:	371.5354472 seconds
• Number of Results:	13	• Number of Results:	12
• UUT Result:	Passed	• UUT Result:	Passed

Figure 24. MVB test time before and after the modifications

Although the time it took the user to complete the test is longer than before, it must be remembered that the time is still shorter than receiving the failing test result and starting the test over. Figure 24 is an example of how the FPY of MVB test was raised when it was concluded that an error by user has caused the failure of the test.

Another revised MVB test case is Transmitter test using physical EMD. In contrast to the previous step, figure 23 indicates that this test has not been the reason for any failed result of MVB module test during the period. This might imply that the build quality of modules has been excellent. The comparison between the reports before and after the edit reveals, that the time it takes to complete Transmitter test using physical EMD test has increased from about six seconds to about seven and a half seconds, which is the result of added delays in the step's program.

6.2 CPS Module

Next, the CPS module test results comparison will be presented. The combined test result statistics for CPS module's A and B modification after the adjustments can be seen in figure 25.

Production testers statistics for CPS2258A

██████████ - ██████████
 TS2012_1 TS2012_3

First time pass yield: 97.08%
 number of units (unique sno): 274
 First time pass: 266
 First time fail: 8

first time failed test cases

- 2 pcs 25.00% Communication test step [Reports](#)
- 2 pcs 25.00% Terminated [Reports](#)
- 2 pcs 25.00% VME signal test [Reports](#)
- 1 pcs 12.50% Voltage, temperature and date test [Reports](#)
- 1 pcs 12.50% SCC test [Reports](#)

Production testers statistics for CPS2258B

██████████ - ██████████
 TS2012_1 TS2012_3

First time pass yield: 98.84%
 number of units (unique sno): 86
 First time pass: 85
 First time fail: 1

first time failed test cases

- 1 pcs 100.00% Software downloading test [Reports](#)

Figure 25. CPS module test result statistics after the adjustments

The number of modules tested using the modified tests is much smaller than before, but still some information can be received from the statistics. First, the Communication test failed two times after the update: the reports indicate, that one of the failures was corrected immediately and the test was run again successfully so the reason for the failure is impossible to identify, and the second module's reports show that the module was tested three times in a short period with failed results and then successfully tested three days later which indicate that the module was malfunctioning and then repaired. The Module name and mod test's issue was linked to the Communication test and tested modules have not failed due to that test case.

Low volume of tested modules after the modifications might be the reason why there are no failed test cases of USB and Ethernet interface test. The reports indicate that the testing time of passed tests has not increased considerably. Figure 26 displays the charts showing the passed result testing time of CPS A module before and after the modifications to tests.

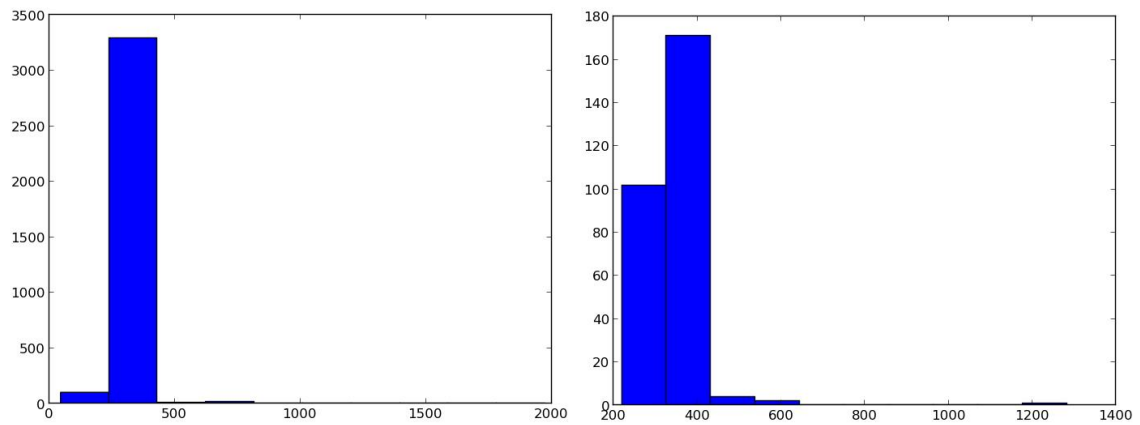


Figure 26. CPS A modification module's pass result testing time before (left) and after the adjustments to the tests

In the charts, the vertical axis indicates the number of successful tests and horizontal shows the time it took to complete the test. It can be seen from the charts that successful test usually lasts less than 400 seconds, but this time has somewhat increased after the adjustments since the user has opportunity to correct the connection and this results in fewer tests conducted.

7 Conclusion

This final year project found that in the case company, the module testers' reliability can and should be improved continuously. The FPY of the module tests is affected by several matters and the impact of these can be decreased by systematic analysis of the test projects and process of improving the module testers. The reports of module tests imply that modifications made during this project have risen the FPY and further development is necessary to create increasingly reliable module testers.

New module tester is being developed in the case company. That next generation tester adopts a completely different system for saving and analysing the module test reports. The reporting statistics is created automatically and can be viewed immediately, thus making the modification of the tests less complicated. The process of analysing the reports needs to be established through experience and followed by the case company, in order to continuously improve the module testers.

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DRO Module Report Example

UUT Report

Station ID: TS2012_2
Module ID: DRO2342-A00
Serial Number: 315321
Date: 4. joulukuuta 2018
Time: 8:06:11
Operator: administrator
Execution Time: 79.0019986 seconds
Number of Results: 5
UUT Result: Passed

Begin Sequence: MainSequence
 (C:\TS2012\TS2007_DRO_3m.seq)

Current consumption test	
Status:	Passed
Module Time:	10.2723725
ch3: Limits: 0.8;1.5 Parameters: 2.5 Current consumption: 1.150821A ch2: Limits: -0.01;0.1 Parameters: 0.1 Current consumption: 0.000226A ch1: Limits: -0.01;0.1 Parameters: 0.1 Current consumption: 0.000392A	
Software downloading test	
Status:	Skipped
Communication test	
Status:	Passed
Module Time:	16.0543052
----- 1 03 DRO - DRO2342A 315321 0 ----- AOM Start 01 >	
Serial number test	
Status:	Passed
Module Time:	0.2022307
sernum w DRO2342A 0 315321 Modules: DRO2342A mod: 0 sernum: 315321 >	
Relay output test	
Status:	Passed
Module Time:	43.4229035
Limits: 5 Parameters: 1-8 Relay 1: Default state NC resistance = 1.645868Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.698692Ohms Relay 2: Default state NC resistance = 1.986113Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.689280Ohms Relay 3: Default state NC resistance = 1.691594Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.688817Ohms Relay 4: Default state NC resistance = 2.367505Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.455918Ohms Relay 5: Default state NC resistance = 1.357831Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.404894Ohms Relay 6: Default state NC resistance = 3.506900Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 3.279761Ohms Relay 7: Default state NC resistance = 1.592787Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.663973Ohms Relay 8: Default state NC resistance = 1.796316Ohms NO resistance = -1.00Ohms Switched state NC resistance = -1.00Ohms NO resistance = 1.831292Ohms	

End Sequence: MainSequence

End UUT Report