SAVONIA

Update for X-Ray Beam Profile Monitor Daughter Card and Firmware

Jussi Kangaskoski

Bachelor's Thesis

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Bachelor's degree (UAS)

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Tiivistelmä

Tässä opinnäytetyössä tehtiin päivitys elektronisuihkun monitorointiin tarkoitettuun laitteeseen ja sen ohjelmistoon. Opinnäytetyö tehtiin Havaijin yliopiston fysiikan osaston Instrumentation Development Laboratory -laboratoriossa.

Monitorointilaitteen päivitys on osa suurempaa kokonaisuutta. Monitorointilaite on osa tutkimusorganisaatio KEK:n hiukkaskiihdytinpäivitystä KEKB:tä Super KEKB:hen. Tuleva hiukkaskiihdytin Super KEKB pystyy 40-kertaiseen luminositeettitasoon aikaisempaan hiukkaskiihdyttimeen verrattuna. KEK toimii Japanin Tsukubassa, jonne on määrä tulla myös uusi Super KEKB -hiukkaskiihdytin. Monitorointilaitteesta päivitettiin tytärkortit. Vahvistinkorttien päivitys ei ollut tarpeellista. SCROD-kortin päivitys ei ollut osa tätä opinnäytetyötä vaan sen hoitivat laboratorion henkilökunta.

Opinnäytetyön tuloksena saatiin päivitetty tytärkortti hiukkaskiihdyttimen monitorointilaitteeseen. Monitorointilaitteen firmware ei tullut valmiiksi, mutta sen kehitykselle on jatkaja ja sitä tehdään parhaillaan.

Avainsanat:
ASIC, STURM, KEK, KEKB, Super KEKB

SAVONIA UNIVERSITY OF APPLIED SCIENCES **THESIS**
Abstract

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Abstract

The purpose of this thesis was to update the electron beam-monitoring device and its firmware. This thesis was made in Instrumentation Development Lab at Physics Department in University of Hawaii at Manoa.

The update of the monitoring device is part of the KEKB particle accelerator upgrade to Super KEKB. Super KEKB will have 40 times greater luminosity than KEKB has. KEK is a high-energy accelerator research organization who owns these colliders. KEK organization is located in Tsukuba, Japan. The monitoring device update focused only on ASIC cards. Amplifier cards did not need update and the update for SCROD was made by the staff of the IDLab. The redesign of the board was made with the PADS design tool and the firmware update with the ISE Xilinx designing tool.

The results of this thesis were successful. The monitoring device is ready for X-ray beam testing. The firmware of the device is incomplete but firmware design will continue.

Keywords:
ASIC, STURM, KEK, KEKB, Super KEKB

PREFACE

This thesis was done for the Instrumentation Development Laboratory in the departament of Physics and Astronomy in University of Hawaii at Manoa, in spring 2012.

I would like to thank the staff of the Instrumentation Development Laboratory for all the guidance and support during my internship and thesis process. Especially I would like to thank Dr. Gary S. Varner, my supervisor, for the possibility to do my thesis in Instrumentation Development Laboratory as well as for all the help he gave me during my exchange period. Special thanks go also to Ari Suopelto, my thesis supervisor, who gave me guidance during the thesis process. I also want to thank Janne Himanen who was my work partner during the whole six months in Hawaii.

Kuopio January 29, 2013

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Jussi Kangaskoski

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SYMBOLS, CONCEPTS AND ABBREVIATIONS

KEK	the High Energy Accelerator Research Organization. KEK is the organization that has the particle accelerator KEKB.
IDLab	Instrumentation development laboratory. Located in University of Hawaii at Manoa. IDLab is the laboratory where this thesis was made.
ASIC	Application Specific Integrated Circuit. Chip built and designed for a specific task. ASIC's behavior cannot be changed by programming.
ADC	Analog to Digital converter. Takes analog input value and converts it into digital voltage.
DAC	Digital to Analog converter. Takes digital input value and converts it into analog voltage.
FPGA	Field Programmable Gate Array. Digital integrated circuit that can be programmed by user.
STURM2	Sampler of Transients for the Uniformly Redundant Mask. ASIC that is deigned to be part of the KEKB particle accelerator upgrade to Super-KEKB
eV	Electron volt. A unit of energy. Often eV is associated with a prefix, i.e. TeV is Tera electron volt and GeV is Giga electron volt.
DCM	Digital Clock Manager. Makes virtual clocks in firmware design.
STURM2	Sampler of Transients for the Uniformly Redundant Mask. ASIC that has specially made for this project
Mils	A unit of measurement used in electronics. One mill equals one thousandth of an inch.
PADS PCB	Design software created by Mentor Graphics. This software is used for circuit board design

SCROD FPGA firmware + PC software to control and readout waveform sam pling ASICs for instrumenting sub detectors in high-energy physics ex periments. Designed in Instrumentation Development Laboratory at Uni versity of Hawaii.

FEL Free Electron Laser. This equipment is used in monitoring devices final hardware testing before it can be used in an actual collider

1 Introduction

KEKB is a particle accelerator owned by a research organization called KEK. KEKB's upgrade to the Super KEKB is now under construction. The X-ray monitoring device for the Super KEKB needs to be redesigned. The design of the monitoring device will be made in Instrumentation Development Laboratory in University of Hawaii at Manoa. The Super KEKB collider will be located in a Tsukuba, Japan.

When an electron beam gets bent in a particle accelerator it will emit an X-ray, which can be monitored. The X-ray will be focused to the fermionics sensor and through a monitoring device it can be monitored and analyzed by a computer. The monitoring device will have a fermionics sensor, amplifier cards, ASIC cards, SCROD and all this will be placed on a motherboard. When the X-ray hits the fermionics sensor the output voltage is only 35 µV when it needs to be at least 10 mV, therefore the signal needs to be amplified. After the amplifiers the signal goes to the STURM2 chip, which will take samples of a voltage caused by the X-ray hitting the sensor. It also holds them until they are transferred to the computer via SCROD.

In this thesis the ASIC card and the firmware of the monitoring device will be updated. The work in the laboratory was made with Janne Himanen, who mostly focused on the motherboard update and the firmware development.

2 KEK

KEK is a high-energy accelerator research organization, which has one of the world's best laboratories in the field of accelerator researching. KEK is increasing people's understanding of the surrounding universe. In the future people will obtain answers to the most compelling questions in nuclear physics, particle physics, life science and materials science. (KEK, 2009)

2.1 Super KEKB

Super KEKB is going to be more efficient than KEKB. It will have 40 times greater luminosity than the older one has. The idea of 'Luminosity' in particle science is diverse the luminosity in stars. It does not show how luminous some matter is but how luminous the collision proceedings are and how efficiently an accelerator produces these events. At first luminosity was meant to get higher by increasing the current. Later it was changed to the nano beam design. Instead of taking high current at the interaction point the nano beam design takes a small beam-size and a large crossing angle. By squeezing beams to the nanometre scale the higher luminosity approaches. Super KEKB was originally designed to be only 20 times greater than KEKB. (KEK, 2009)

The nano beam scheme brings out the best of the interaction mechanism. The beam gets squeezed by a strong magnetic field. Using the nano beam option in Super KEKB has many advantages and the most important of them is that using the nano beam design the particle accelerator is greener. The beam current is only 4 Ampere and otherwise it would be 9.4 Ampere. (KEK, 2009)

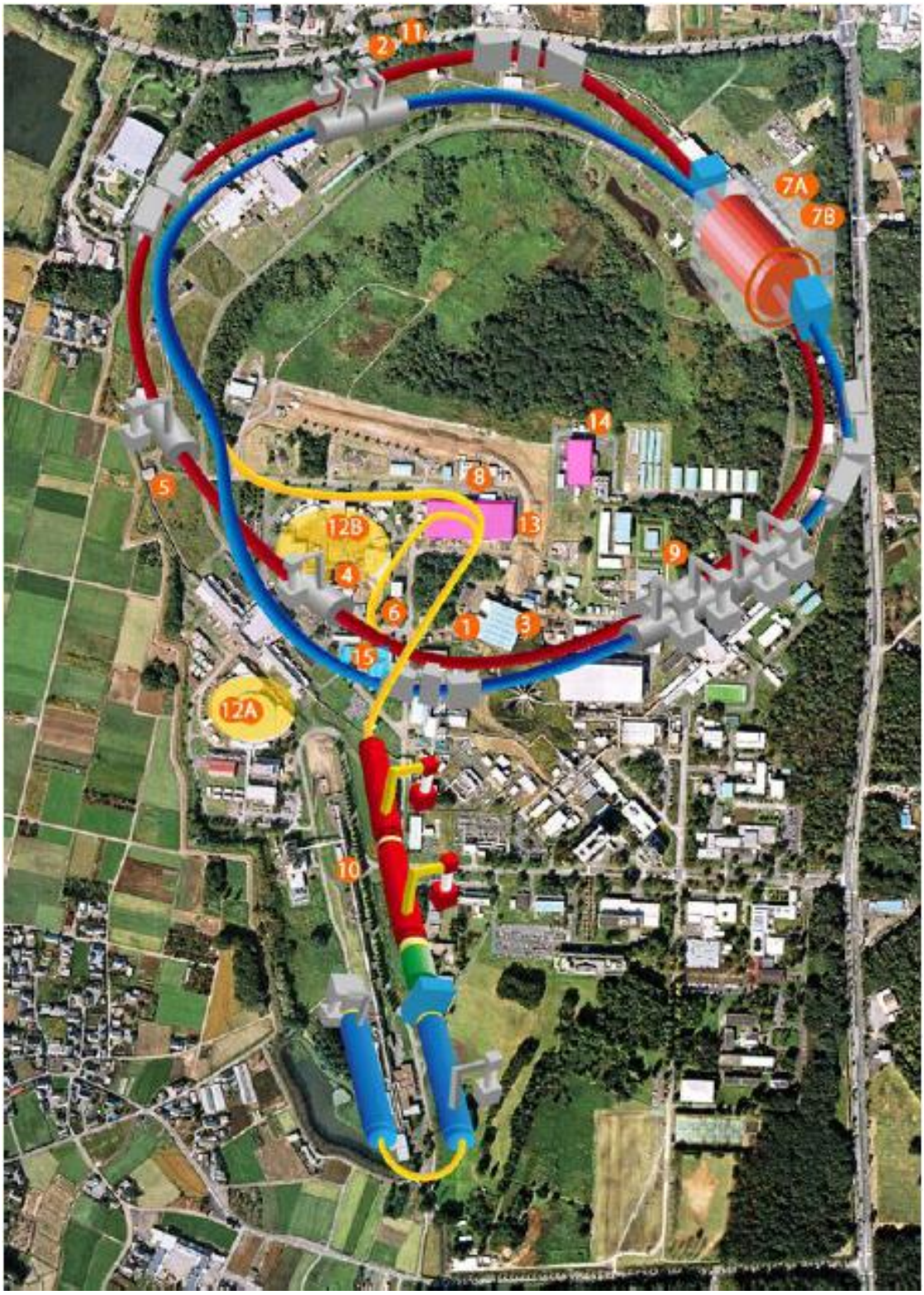

FIGURE 1. KEKB facilities and components (Jussi Malin, 2012)

Figure 1 shows the campus map of Super KEKB. Super KEKB is located in Tsukuba, Japan.

Campus is presented in the list below.

1. Magnets in the arc section. 2. Superconducting accelerating cavities. 3. Movable mask. 4. Normal conducting accelerating cavities (ARES). 5. Transverse kicker. 6. End of the beam transport line. 7A. The Belle detector at KEKB. 7B. A quadrupole superconducting magnet at the point of cllision (QCS). 8. Beam transport line. 9. Wiggler magnets. 10. The injector. 11. Crab cavity. 12A. Photon Factory (PF). 12B. Photon Factory (PF-AR). 13. Accelerator Test Facility (ATF). 14. Superconducting rf Test Facility (STF). 15. KEKB Control room

2.2 STURM2

STURM stands for Sampler of Transients for the Unifomrly Redudant Mask. The STURM2 chip was designed to make a very fast sampling. The design of the chip is in Figure 2. This chip collects and holds the samples from the fermionics sensor and later provides them to the computer via SCROD.

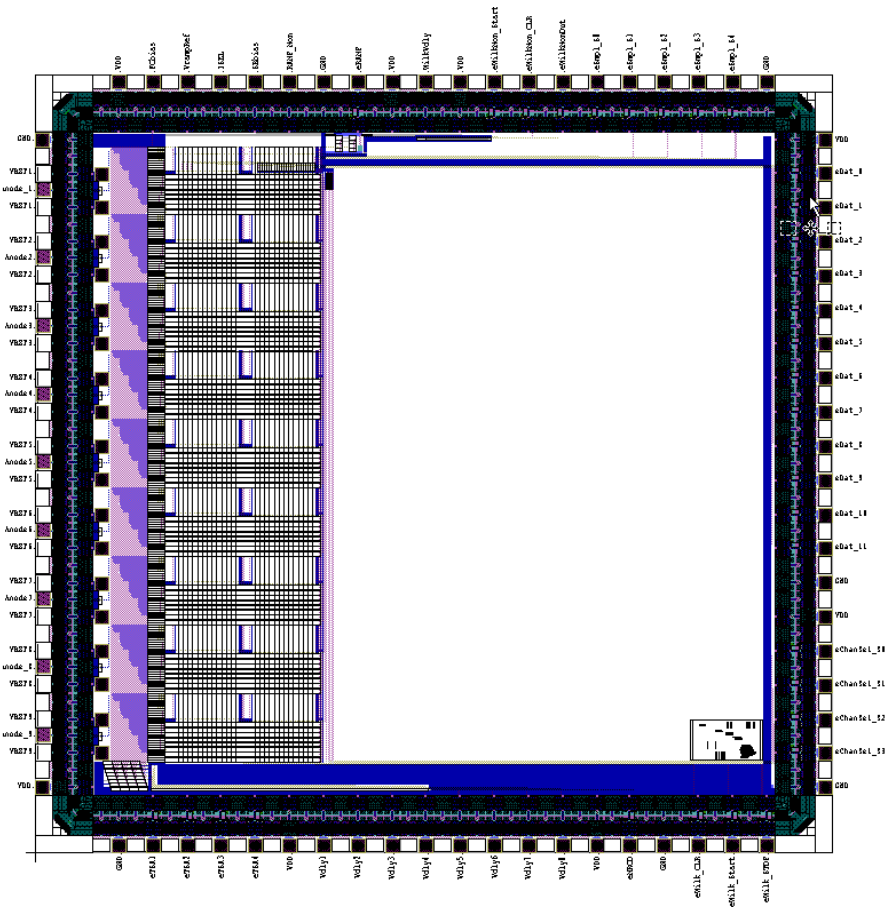

FIGURE 2. STURM2 Design

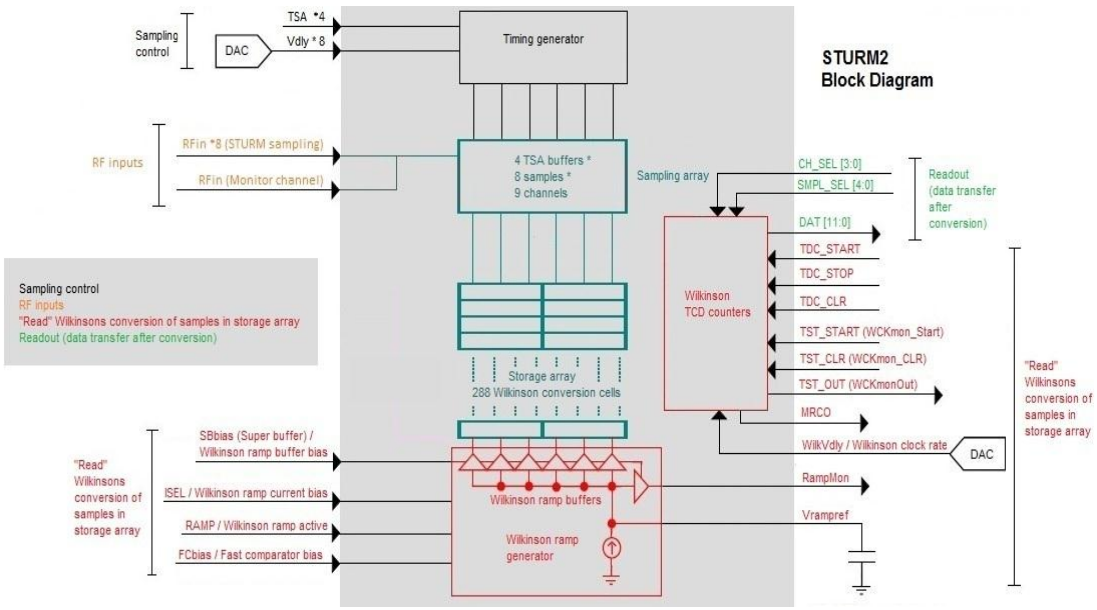

FIGURE 3. STURM2 Block Diagram

As seen in Figure 3 the STURM2 chip has 8+1 channels, eight for the sampling and one for monitoring. STURM2 chip has four TSA sample buffers, which all have eight samples per buffer. The STURM2 chip has 288 Wilkinson conversion cells. The STURM2 chip has one word sample readout (RAM) and 100 kHz sustained readout (orbit). The STURM2 chip has been designed in IDLab at Honolulu, Hawaii by Dr. Gary S. Varner. (Dr. Gary S. Varner, 2009)

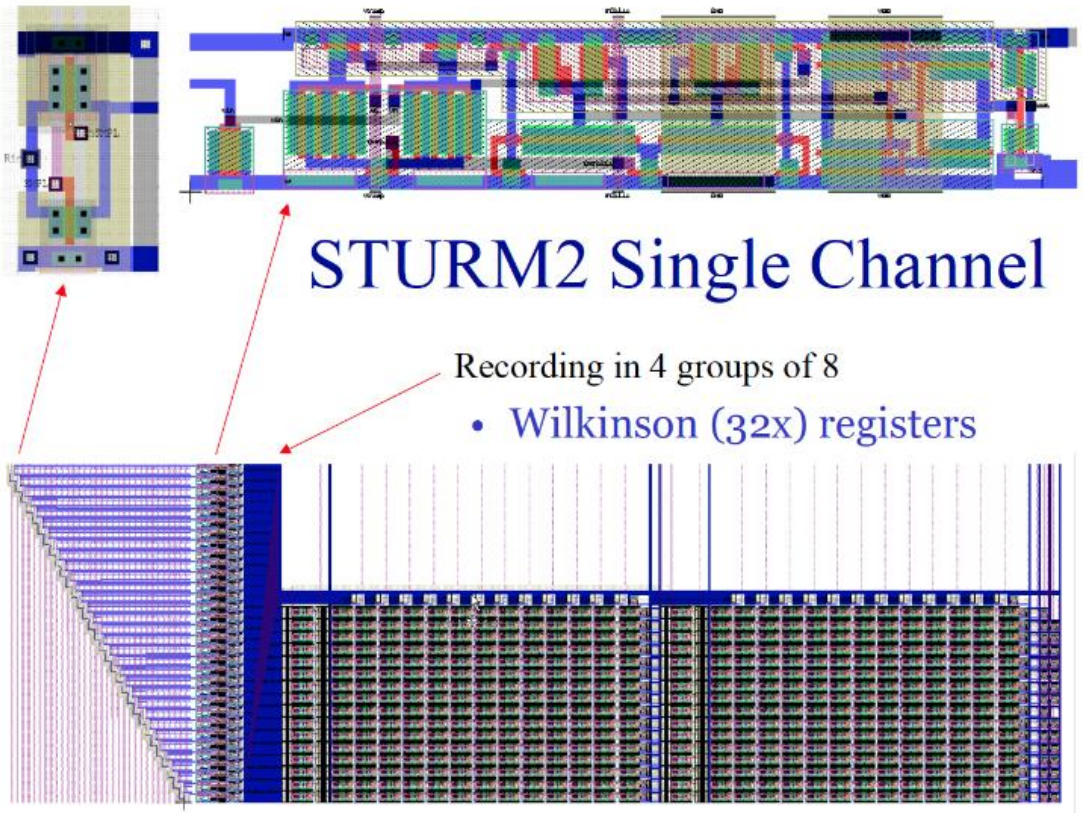

FIGURE 4. One single channel of STURM2

One of the eight channels of the STURM2 chip is shown in Figure 4. One channel has 32 registers and the whole chip has 256 registers. However 288 Wilkinson conversion cells must be used because of an extra channel for monitoring. Figure 5 shows how the timing has been made and also where the 32x register comes from. (Dr. Gary S. Varner, 2009)

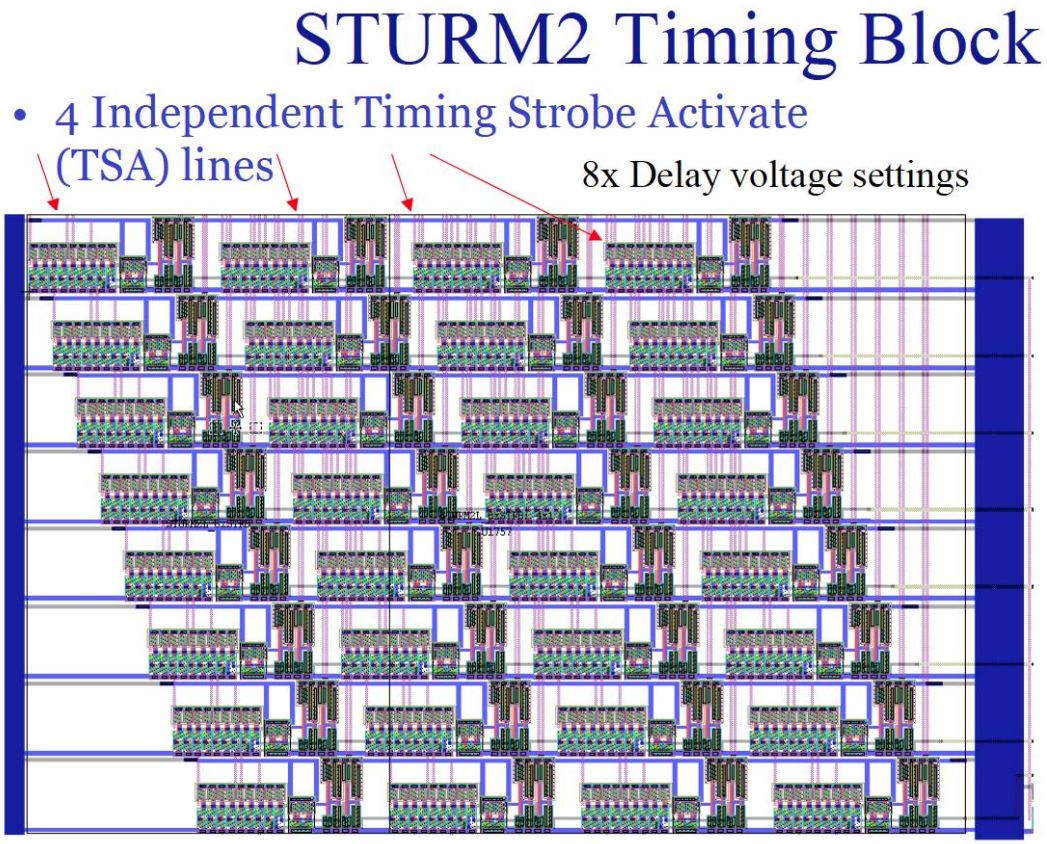

FIGURE 5. Timing Block of STURM2

3 Fermionics sensor

The fermionics sensor is placed in the middle of the motherboard and it sits on in a GPA socket. Bending the electron beam it emits an X-ray. The X-ray is focused to the X-ray detector (Figure 6). X-ray detector in this case is a fermionics sensor.

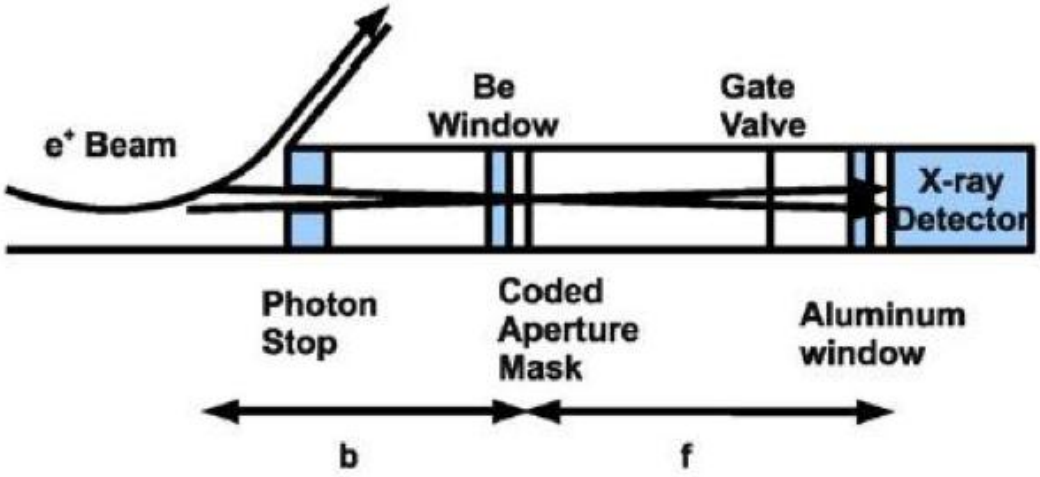

FIGURE 6. Bending the electron beam it emits X-ray

3.6 eV is needed to release one electron-hole pair from the silicon material, so the X-ray with a 3.6 keV magnitude will produce 1,000 electron-hole pairs. 1,000 electron-hole pairs is equivalent to 0.16 fC charge. (Dr. Gary S. Varner, 2009)

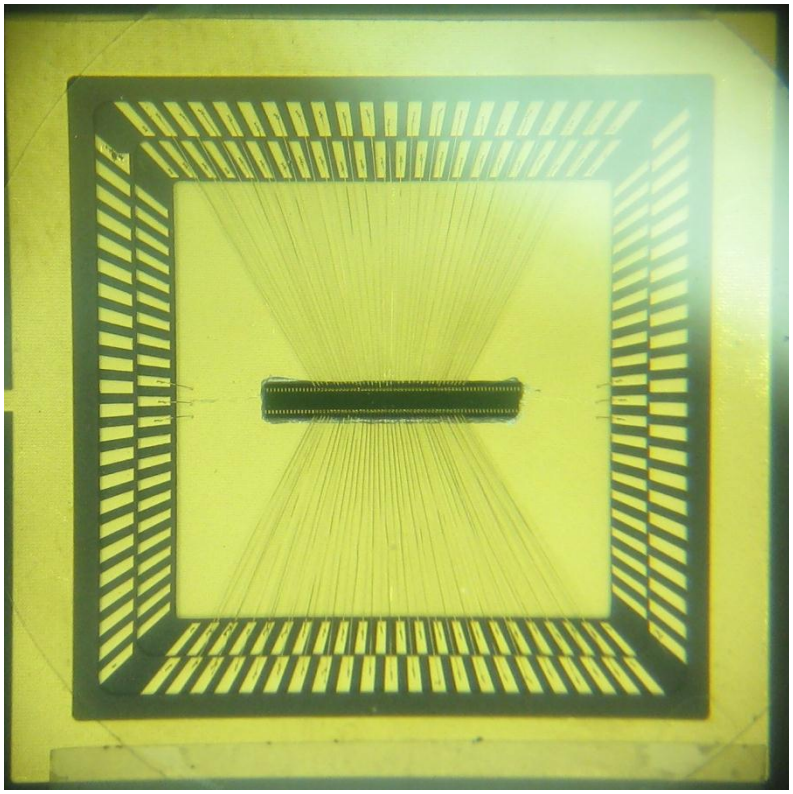

IMAGE 1. Fermionics sensor

X-ray gives 0.16 fC charges and fermionics sensors (Image 1) low-high change time is 0.25 nS. The current produced from the sensor with this charge is

$$\Delta I = \frac{\Delta q}{\Delta t} = \frac{1.6*10^{-16}C}{2.5*10^{-10}s} = 0.7\mu A \qquad [1.1]$$

Sensor's output voltage, with 50Ω transfer line, is

$$\Delta \mathrm{V} = \Delta \mathrm{I} * R = 0.7\mu A * 50\Omega = 35\mu V \qquad [1.2]$$

The ASIC needs at least 10 mV in order to receive the signal in a reasonable resolution. To 10 mV from 35 µV the gain needed is 50 dB.

$$G = 20 * log_{10}\frac{U_{OUT}}{U_{IN}} = 20 * log_{10}\frac{10mV}{0.035mV} = 49.11dB \approx 50dB \qquad [1.3]$$

(Dr. Gary S. Varner, 2009)

4 X-ray monitoring device

To monitor X-rays a device must be designed. The device has the fermionics sensor and the STURM2 chip. Amplification is needed because the fermionics sensor gives out only 35 µV and the ASIC card needs at least 10 mV. The device became eventually a motherboard that holds the sensor, all the amplifier cards, all the ASIC cards and the SCROD. Image 2 presents the monitoring device with assembled ASIC card, eight channels of amplifiers and the SCROD. The GPA socket holding the fermionics sensor is in the middle of the motherboard.

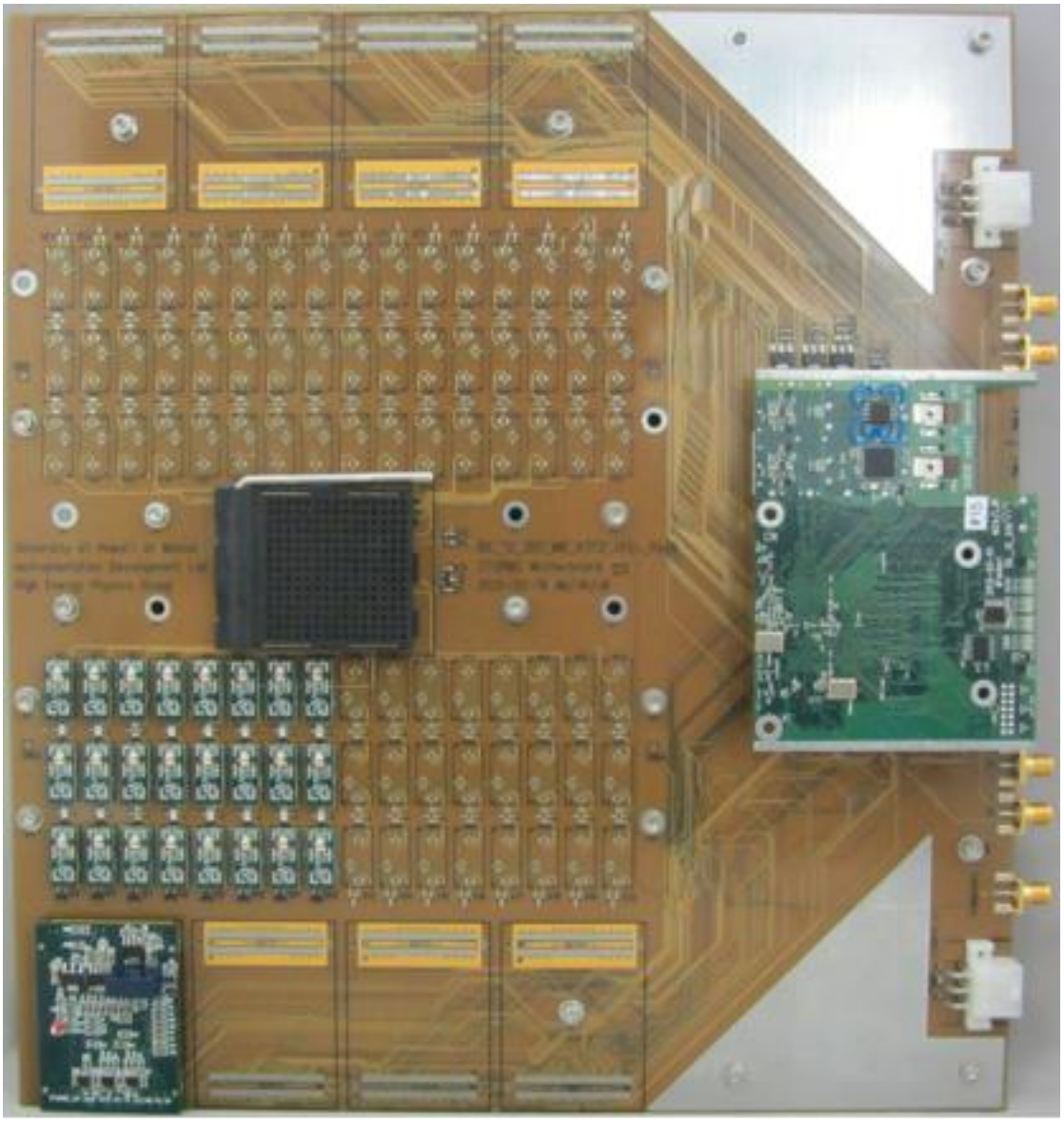

IMAGE 2. X-ray monitoring device with STURM2 chips

4.1 Motherboard

The motherboard design started in 2011 and was completed in 2012 as revision B. The motherboard revision A was well maid and only few changes were needed. The motherboard has 96 amplifier cards on both sides. In total there are 192 amplifier cards, eight ASIC cards and the SCROD. The fermionics sensor is also placed on the motherboard. The motherboard has two power connectors, one for the amplifier cards and the other for everything else. In the bottom side of the motherboard there is nothing but half of the amplifier cards.

The motherboard has eight layers. Two are grounds and three are powers. One of the power layers is just for the amplifiers. The motherboard has seven different operating voltages. SCROD operates 1.2, 1.8, 2.5 and 3.3 voltages. For the amplifier cards are four volts and five volts for the ASIC cards.

4.2 Amplifier cards

Referring to the formulas on a page 16, the ASIC needs 10 mV while sensor's output voltage is only 35 µV. The needed amplification is at least 50 dB. Gain was raised to 60 dB to be more reliable and easier to design. The rule of thumb is not to go over the 40 dB inside of a box, because of that the amplification has been made with three stages. The final design was three amplifiers in a row with each 20 dB and total 60 dB, which gives the wanted 10mV to the ASIC.

The PCB-design of the amplifier card consists of four layers and a number of components. The layers are top, bottom, ground, and power. Soldering components to the amplifier card is easy except RF-connectors. Those tiny connectors needs to be soldered to their proper place where they meet a similar connectors on the motherboard

4.3 Daughter cards

The daughter cards, also known as the ASIC carrier card, main purpose are to collect samples from the sensor and to make 12-bit analog to digital conversion. The ASIC card has had a few revisions and the latest revision was finished in 2012. The differences between the two newest revisions are not that major but yet necessary. Image 3 shows the top and the bottom of the assembled ASIC card.

IMAGE 3. Daughter card with STURM2 chip

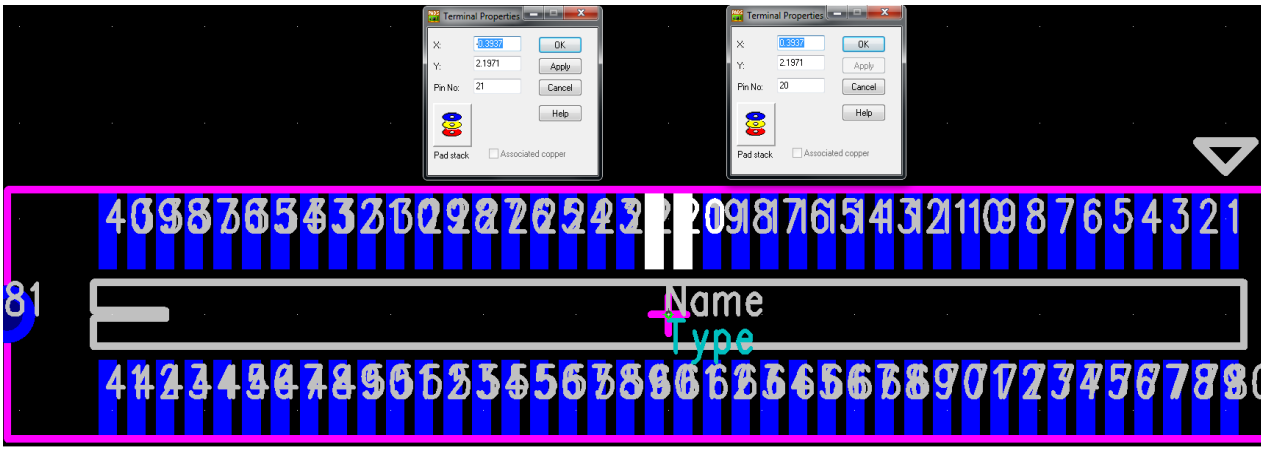

FIGURE 7. Connectors footprint was wrong

As seen in Figure 7, the footprint of the gaps between connector's legs was too small. The footprint was made in mils and when converted to the metric units, the gap was wrong size. It should have been 0.8 mm when it was 0.7874-mm. It does not seem a lot but when mistake multiplies the pads do not meet the connectors in rear. That could have made soldering unwanted. When soldering connectors to the pads, with wrong size of the gap, the legs need to be spread and could accidently get cut off. In the whole device there are 16 connectors in the motherboard and two connectors on each ASIC card. On the motherboard there are eight ASIC cards. This little mistake could have caused lot of extra work.

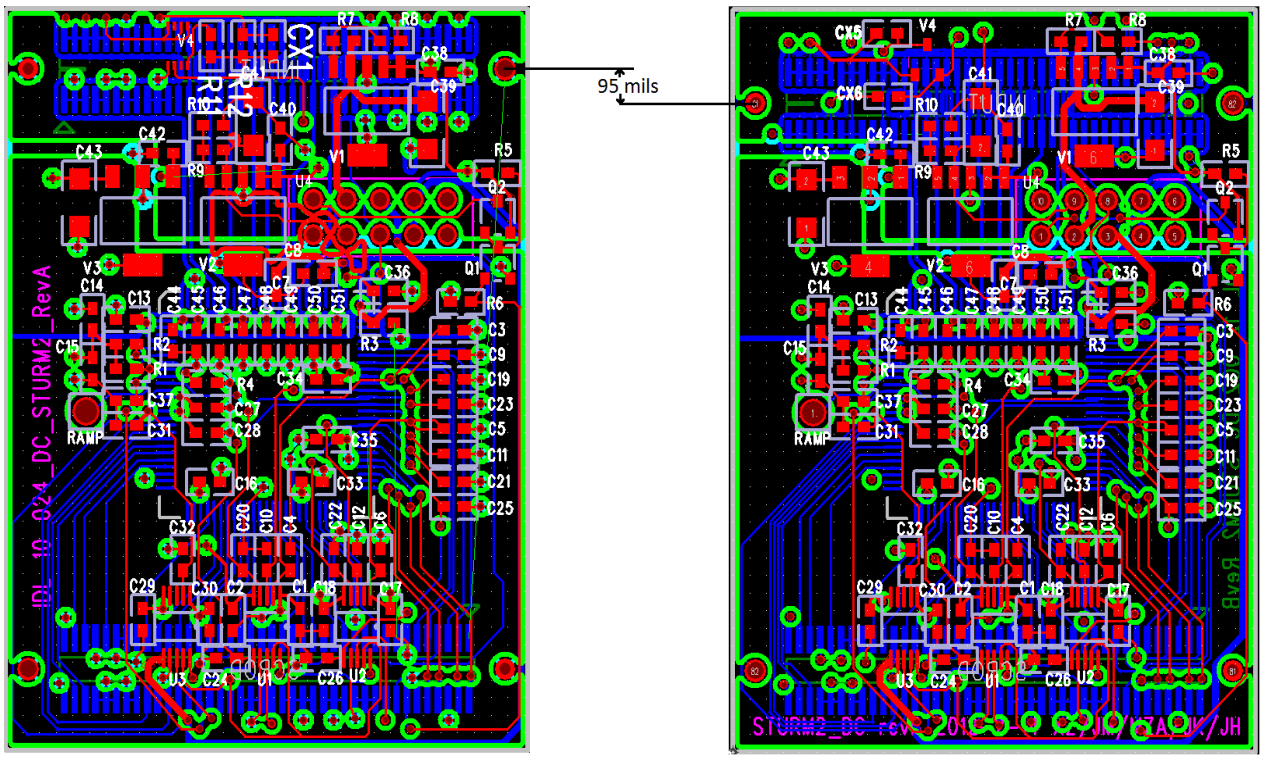

FIGURE 8. Connectors legs needed to move 95 mils down

In the ASIC card the connectors were not in their right position. The upper connector needed to be moved 95 mils down to its proper place, as shown in Figure 8. Otherwise it would not have met the connector in the motherboard as wanted. Image 4 shows a new revision of the ASIC card where the connector has been moved and it meets the connector in the motherboard.

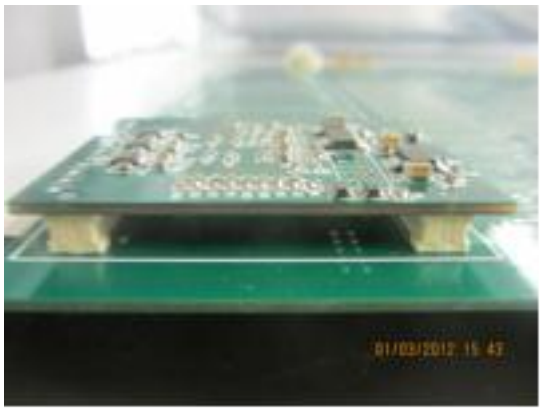

IMAGE 4. ASIC card connected to the motherboard

When the DPED net from the relay to the regulator V1 was made it was not yet connected. To solve this, the DPED net needed to be redone. Figure 9 shows the DPED net with black colour.

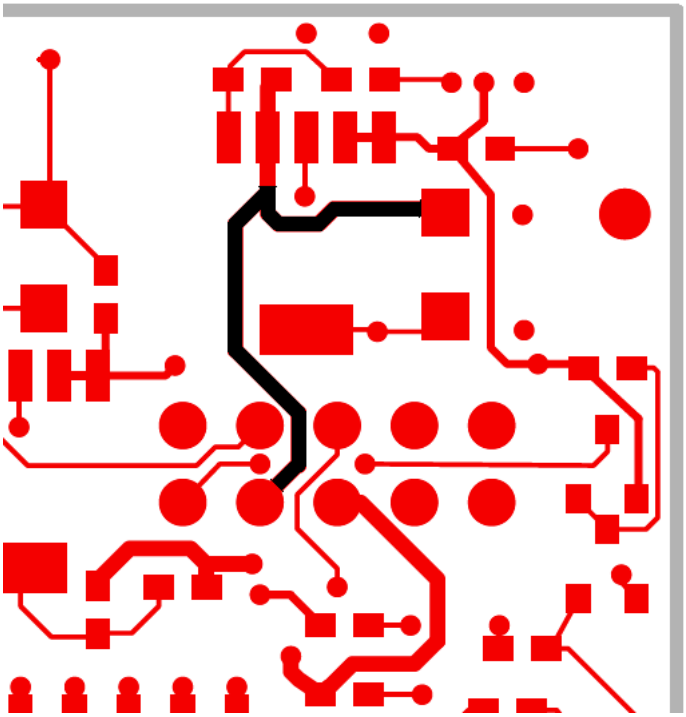

FIGURE 9. PCB file. Relays redone line in black

The last change between revision A and B is the regulator V4 that was changed from LD39015 to AP7333. AP7333 is simpler than LD39015. The circuit diagrams of the components are the same. AP7333 regulators did not need to be ordered and therefore time was saved. Figure 10 shows a footprint of the previous regulator and the new one. The left regulator is a LD39015 and the right one is a AP7333.

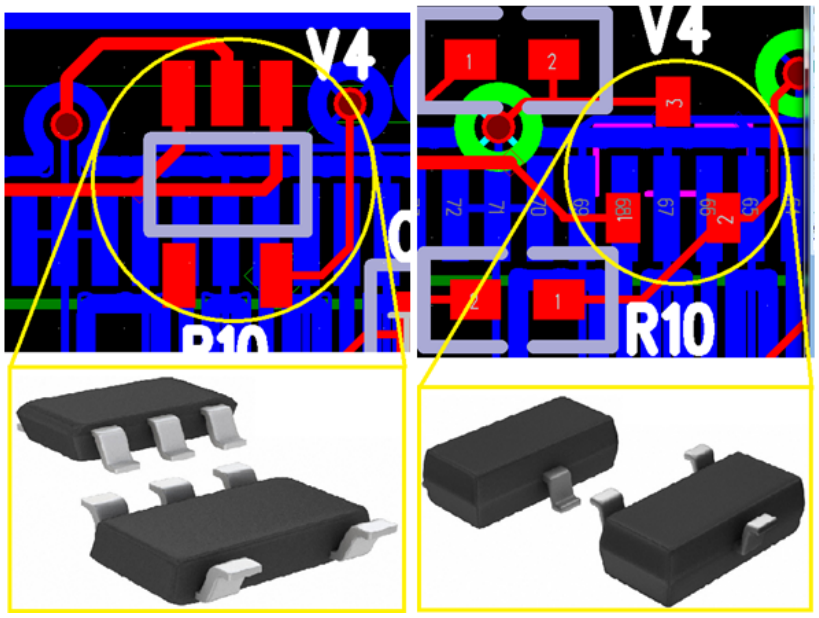

FIGURE 10. Regulator V4 in ASIC card

4.4 SCROD

SCROD is an interface between the monitoring device and the computer. It is designed in the IDLab earlier and it is used in many projects for the same purpose. The SCROD holds a Spartan 6 FPGA and it has a lot of connection points as USB, JTAG, Optical cable, RJ45 etc. In this project SCROD's main job is to retrieve the samples from STURM2 chip and share them to the computer for analyzing. A STURM2 firmware is in the SCROD. Image 5 shows revisionA2 of the SCROD. This is from batch 3. This SCROD was used in this thesis.

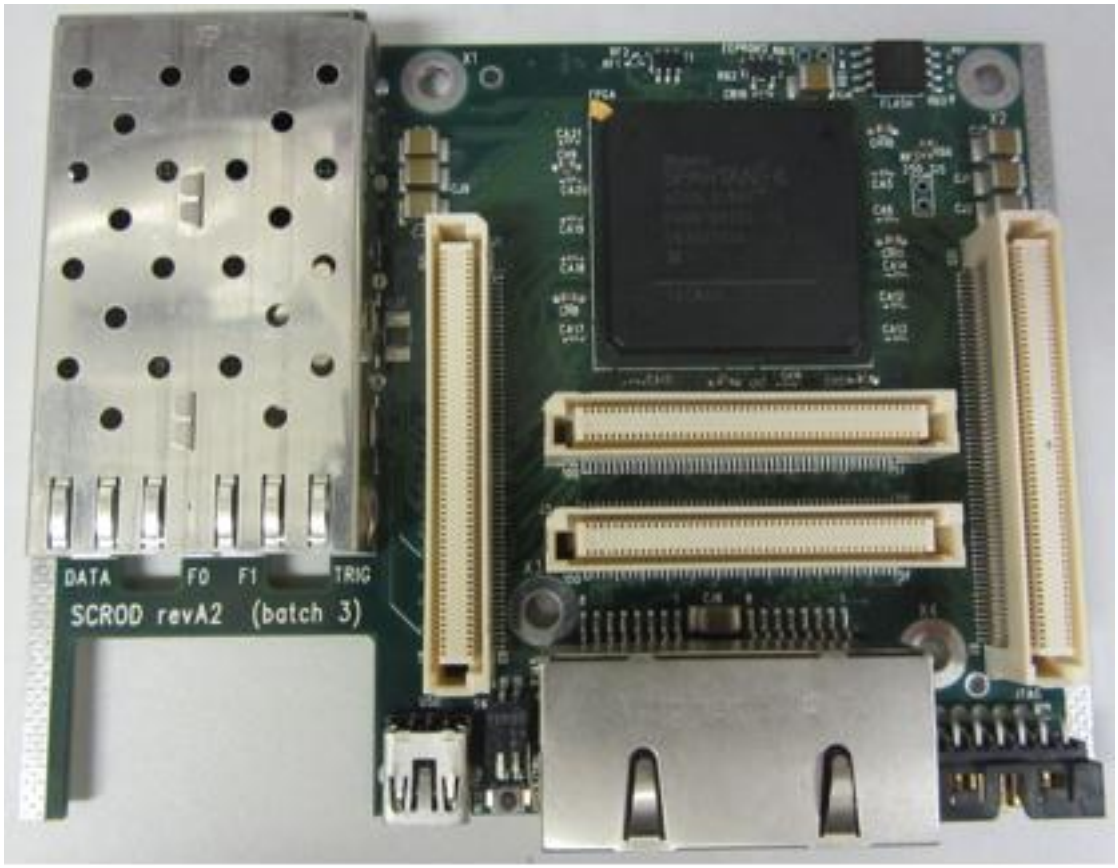

IMAGE 5. SCROD rev A2 with Spartan 6 FPGA

5 Firmware architecture

The STURM2 firmware is playing significant role in this project. Its major mission is to collect all the samples from the ASIC and deliver them to the computer. All this needs to be done in a minor time with a major speed. All the samples from every ASIC card need to be collected separately, which can be done with a delay. The STURM2 firmware consists of TOP, CLK_MAIN, DAC_MAIN, STURM2_MAIN, USB_MAIN and UCF. The coding language in this firmware is VHDL, which is originally made for the US military defense. VHDL is the most popular language in the firmware developing. The present code needed to be changed from the STURM2 evaluation board to the SCROD. The evaluation board has Spartan 3 FPGA and SCROD has Spartan 6 FPGA. In firmware designing this means that not only the UCF needs to be changed but much more. Figure 11 shows the hierarchy of the STURM2 firmware in the ISE Xilinx software.

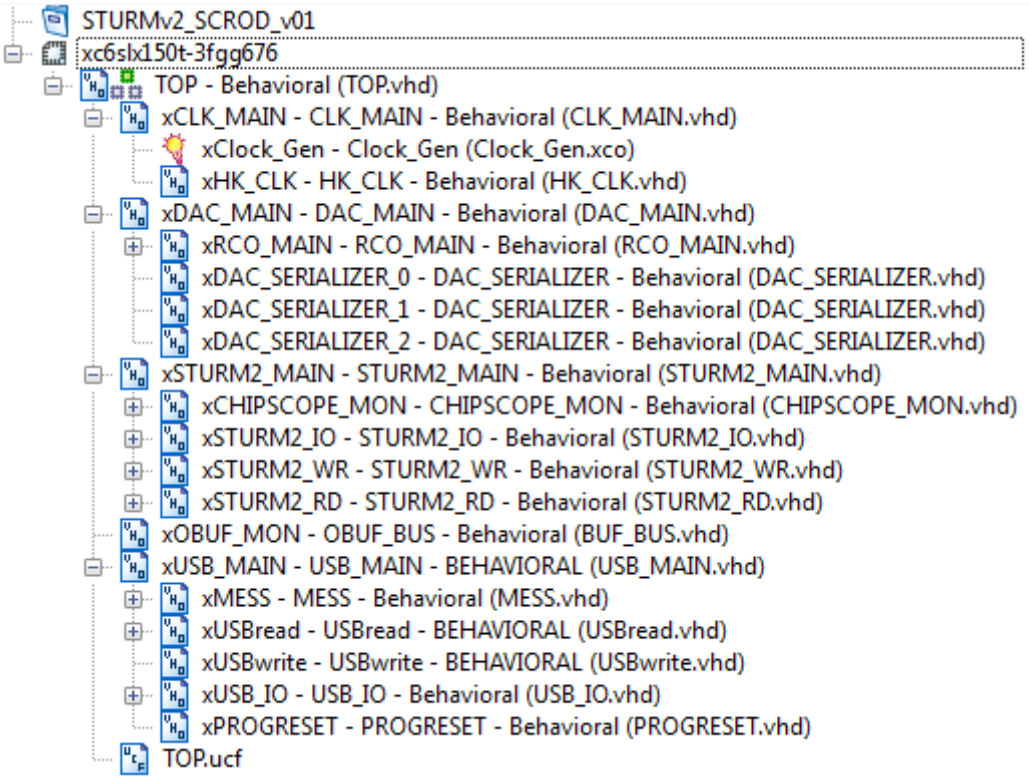

FIGURE 11. Hierarchy of the STURM2 firmware

UCF file reflects the pins of the FPGA. The code and the FPGA are connected via UCF file. Here all the pins from each block are showing simply. For example a board clock is taken to the code via FPGA and UCF file.

TOP block is the highest block of the code. The TOP block combines all the other blocks in the firmware. If the signal is needed in some other block than the one it has been made in it goes to the block it is needed via a TOP block. The TOP block combines not just the other blocks but also the UCF file.

CLK block is about the clocks. Every clock needed in this firmware are made there. So-called board clock, which comes from SCROD, is transferred to 150MHz when by itself it is 250 MHz. The RAM block needs a 10MHz clock, which is made in the clock generator under the CLK block.

DAC block's main purpose is to make a delay between the samples and to give an address for the sample. Adding time to the latest delay makes the delays.

STURM2 block's main purpose is to receive those samples from right place. There are eight ASIC cards, which each have the STURM2 chip, which all acquires 256 samples. The firmware needs to receive those samples from the chip separately. Obtaining the sample from the right place is taken care of in this block.

USB block's main purpose is to carry the samples to the computer for analyzing. In the USB block the data can be posted to the computer but also information can be read from the computer. In the future the optical cable will transfer the information.

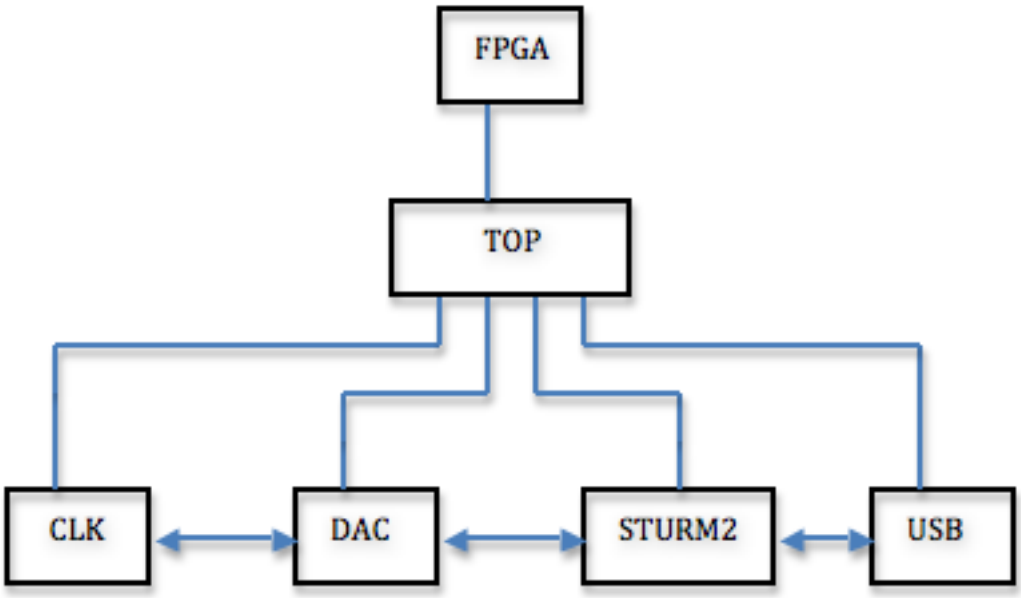

FIGURE 12. Firmware architecture

The firmware architecture is shown in Figure 12. Blocks CLK, DAC, STURM2 and USB works parallel below the TOP block. The signals which are needed in many blocks, need to be transferred via TOP. For example the clock signal comes from the

FPGA through the TOP to the CLK block and all the way to the DCM. The DCM generates a new virtual clock signal, which is needed in the DAC block. The new clock signal goes from the CLK block to the DAC via TOP block. The signal needs to be transferred via TOP if needed in another block than the one they are generated in.

5.1 Requirements and Objectives

At first the firmware was on the STURM2 evaluation board for developing the code. The code needed to be transferred to the SCROD. Technically the code needed to be transferred from Spartan 3 FPGA to Spartan 6 FPGA. The very first step was to check the UCF file and redo it. There are different pin numbers in Spartan 3 and Spartan 6 and that is why this needs to be the first thing to do.

The DCM, also known as Digital Clock Manager, component under the CLK_MAIN needs to be redone, which in Spartan 3 and Spartan 6 FPGAs are different. With a Spartan 3 the DCM can be made strictly inside the code unlike with Spartan 6. The DCM for Spartan 6 can be done with a separate component inside the code (Figure 13). The DCM is a component that creates all the virtual clocks. The STURM2 firmware was made with the 150 MHz board clock but in SCROD the board clock is 250 MHz, therefore the DCM needed to be redone.

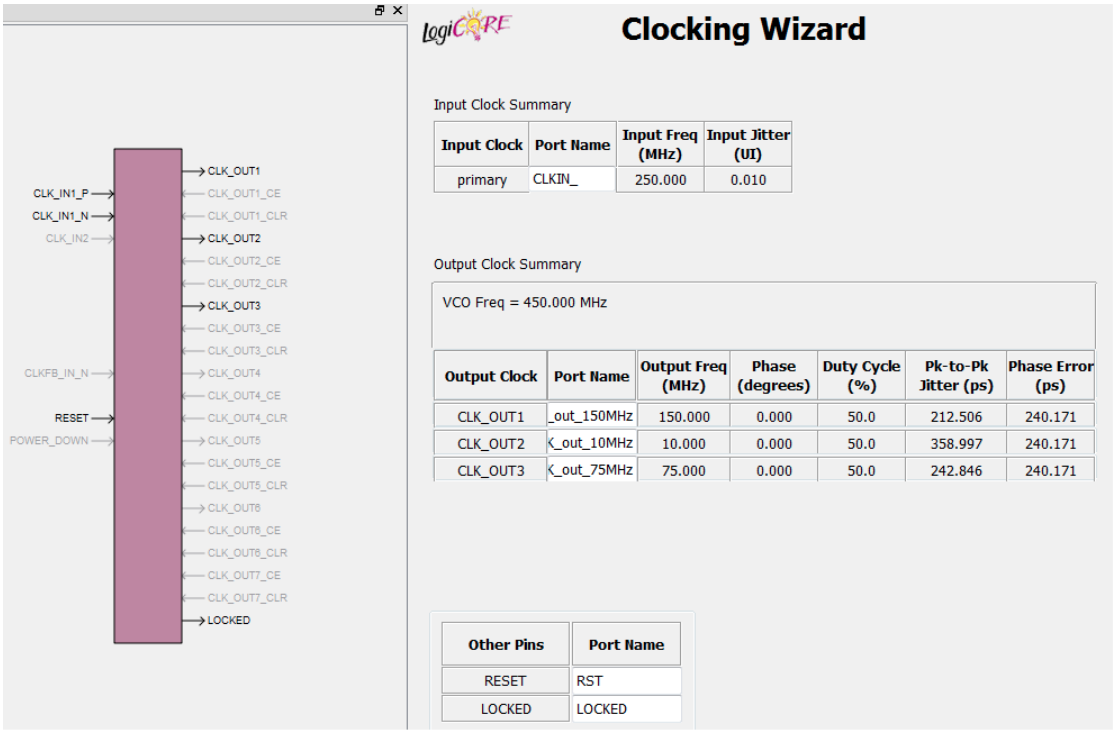

FIGURE 13. Clocking Wizard. New DCM in progress

```
component Clock_Gen
   port(
      CLKIN_P         : in     std_logic;
      CLKIN_N         : in     std_logic;

      CLK_out_150MHz : out    std_logic;
      CLK_out_10MHz  : out    std_logic;
      CLK_out_75MHz  : out    std_logic;

      RST            : in std_logic;
      LOCKED         : out std_logic
         );
end component;
-------------------------------------------------------------------------------
   xClock_Gen  : Clock_Gen
   PORT MAP(
      CLKIN_P        =>    BCLKp,
      CLKIN_N        =>    BCLKn,
      CLK_out_150MHz =>    CLK,--_150MHz,
      CLK_out_10MHz  =>    xCLK_10MHz,
      CLK_out_75MHz  =>    CLK_75MHz,
      RST            =>    not (xWAKEUP), --'0',    --not (xCLR_ALL),
      LOCKED         =>    LOCKED
            );
```

FIGURE 14. New DCM taking in to the firmware in CLK_MAIN block

Figure 14 shows how the component is taken to the actual code. One needs to define a component and later call it. In the UCF file the board clock is named as BCLKp and BCLKn. Board clock in SCROD is differential, therefore two signals must be used. The pin can be named as wanted but the same name must be used everywhere where the board clock is used. The port map in the code shows how the component is called. In this case the board clock in the DCM is CLKIN_P and CLKIN_N and in the UCF file the pins are BCLKp and BCLKn. The board clock from the UCF comes to the DCM and gives the clock frequency. The DCM's output clocks in this firmware are 150MHz, 75MHz and 10MHz. To work the DCM needs a real clock.

Another huge difference is that a double buffer cannot be used for shifting a virtual clock to the board. Spartan 6 FPGA does not support a double buffer and the ODDR2 component has to be used instead. With Spartan 3 FPGA there is no such a problem. Figure 15 shows how the ODDR2 component replaces the buffer used in the original code with Spartan 3 FPGA.

```
--------------------------------------------------------------------------------
-- xOBUF_SCLK : OBUF
-- port map (
--    I  => xCLK_10MHz,
--    O  => SCLK);
--------------------------------------------------------------------------------
   xODDR2_SCLK : ODDR2
   generic map (
        DDR_ALIGNMENT => "NONE", -- Sets output alignment to "NONE", "C0", "C1"
        INIT          => 0,    -- Sets initial state of the Q output to '0' or '1'
        SRTYPE        => "SYNC"  -- Specifies "SYNC" or "ASYNC" set/reset
              )
   port map (
        Q  => SCLK,         -- 1-bit output data
        C0 => xCLK_10MHz, -- 1-bit clock input
        C1 => not (xCLK_10MHz),   -- 1-bit clock input
        CE => '1',          -- 1-bit clock enable input
        D0 => '1',          -- 1-bit data input (associated with C0)
        D1 => '1',          -- 1-bit data input (associated with C1)
        R  => '0',          -- 1-bit reset input
        S  => '1'           -- 1-bit set input
            );
--------------------------------------------------------------------------------
```

FIGURE 15. Output buffer need to be change to ODDR2 block

5.2 Future

The firmware design continues and the STURM2 firmware will provide samples from the fermionics sensor to the computer to be analysed in the future. The firmware is not finished yet but it is in progress. The firmware is not the only unfinished thing in this project. The oscillation problems with the amplifier cards also have to be solved before they can be used in the real particle accelerator.

6 Testing

In this thesis the amplifier cards and the STURM2 firmware were tested. The amplifier cards were tested with a network analyzer and the firmware with an USB-tester and a ChipScope.

6.1 Amplifier cards

The amplifier cards needed to be tested in two parts. The first part was to test the amplifier cards by themselves, as shown in the Image 6, and the second part with all the three cards in a row, as shown in the Image 7. The measurements were made with N9923A FieldFox Handheld RF Vector Network Analyzer. Image 8 shows how the amplifiers are connected to the Network Analyzer. The power for the amplifier cards is from the power supply.

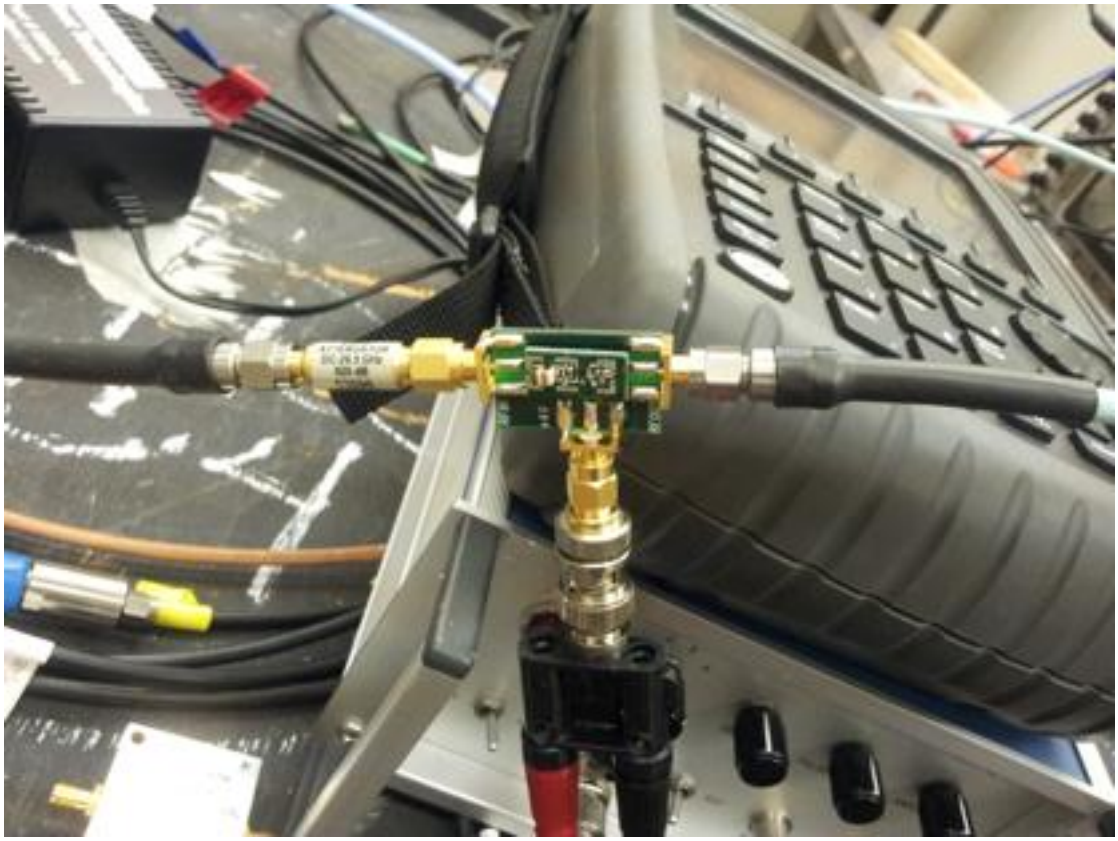

IMAGE 6. One Amplifier with 20 dB attenuator

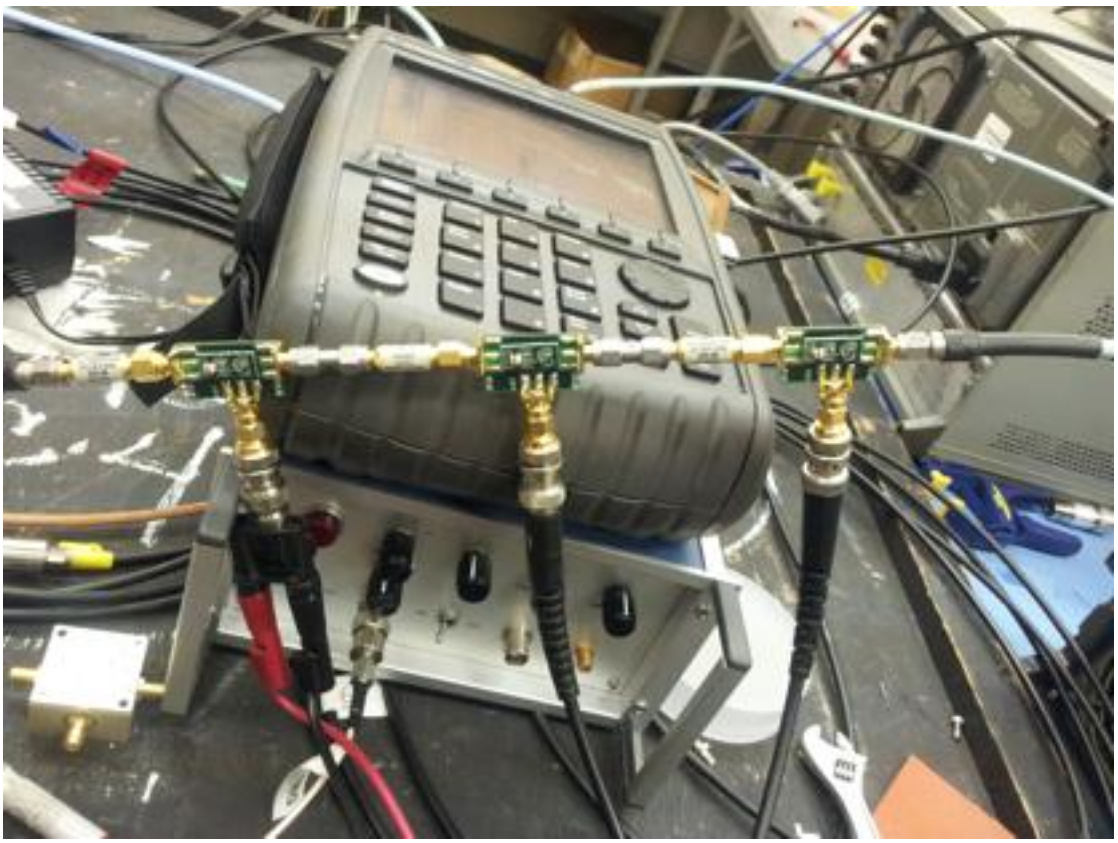

IMAGE 7. Three amplifiers with three 20 dB attenuators

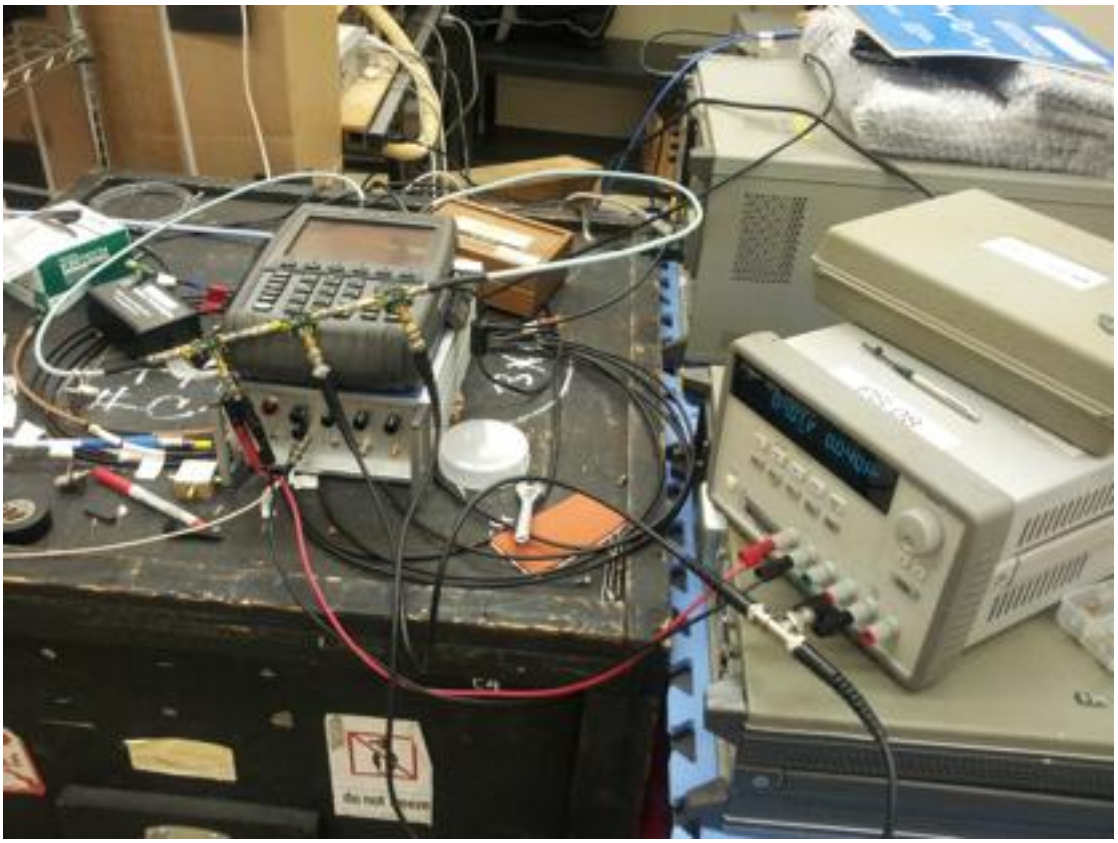

IMAGE 8. Measuring three amplifiers in a row with network analyzer

Measuring with the network analyzer is quite simple because it is a signal generator and a measurement device at the same time. The network analyzer gives the results in xlsx –format that can be used for variable applications. For testing the amplifier cards the carrier boards were made. Image 9 presents the amplifier cards standing on the carrier boards. These carrier boards had the same RF connectors as the motherboard, as seen in Image 10.

IMAGE 9. Amplifier card's carrier board for testing

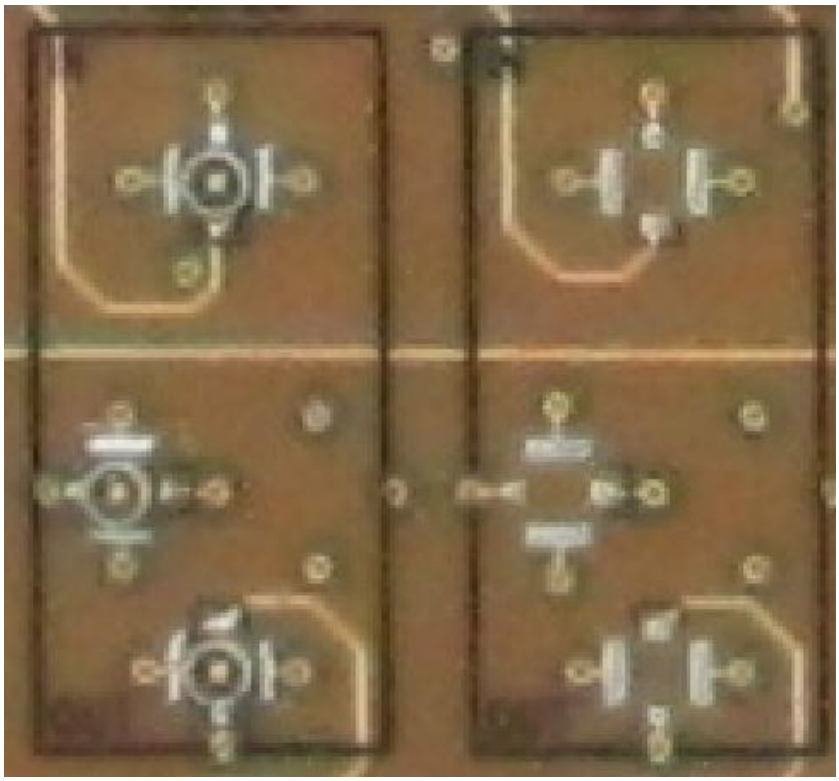

IMAGE 10. RF-connectors in motherboard for amplifier cards

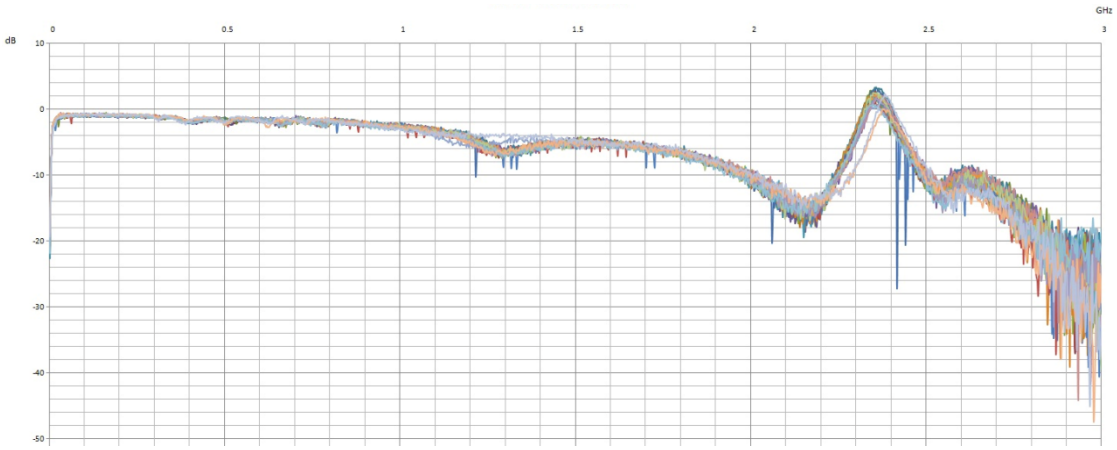

Chart 1. Test result. One amplifier with 20dB attenuator

The frequency that one is interested in is around 1 GHz. These test results shows that the amplifiers works as required. (Charts 1 and 2)

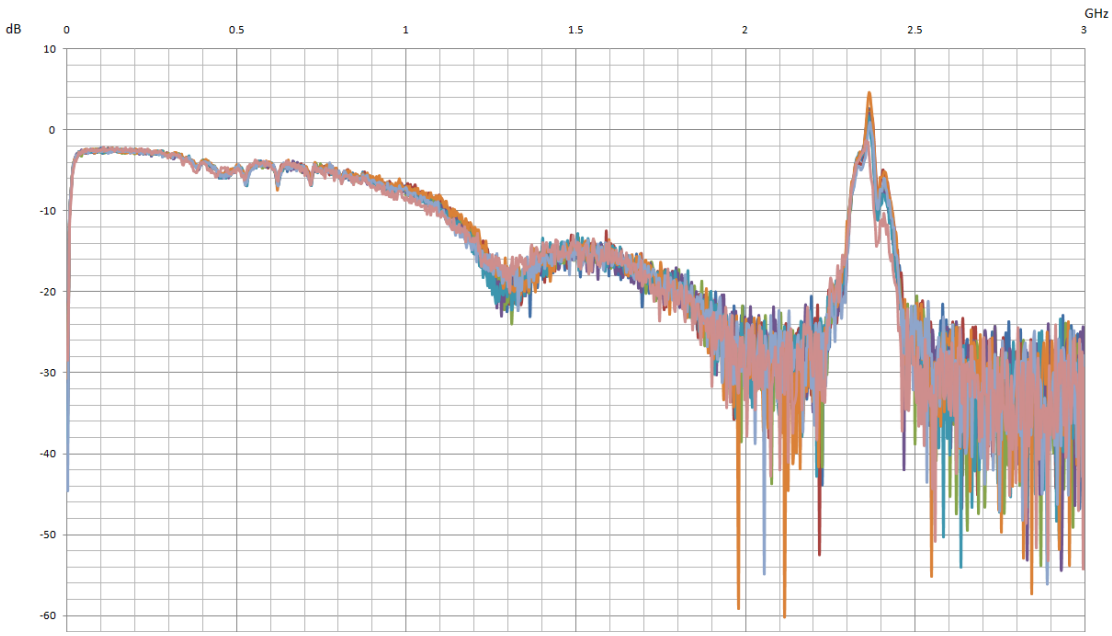

Chart 2. Test result. Three amplifiers in a row with three 20dB attenuators

Amplification with three amplifiers drops somewhat but not too much. There is a point where amplification rises signicantly. Filters between every amplifier stage are supposed to prevent that.

These tests were made with the carrier boards. When the amplifier cards were put on the motherboard to their right places, the results were not like expected. The amplifiers started to oscillate right away when the power was turned on. Apparently the amplifier stages were too close to each other and should have been placed further away.

There are a couple of possible solutions for that problem. Removing the filters is one possibility, because those filters are reflective and causes oscillation. Removing the filters helped a bit but it did not solve the problem. The oscillation was still occuring. Changing the attenuator element in the amplifier card to a bigger one worked but the oscillation was still too great. Making a shield to the amplifier card might be solution. Image 11 shows the oscillation when there was no signal coming in.

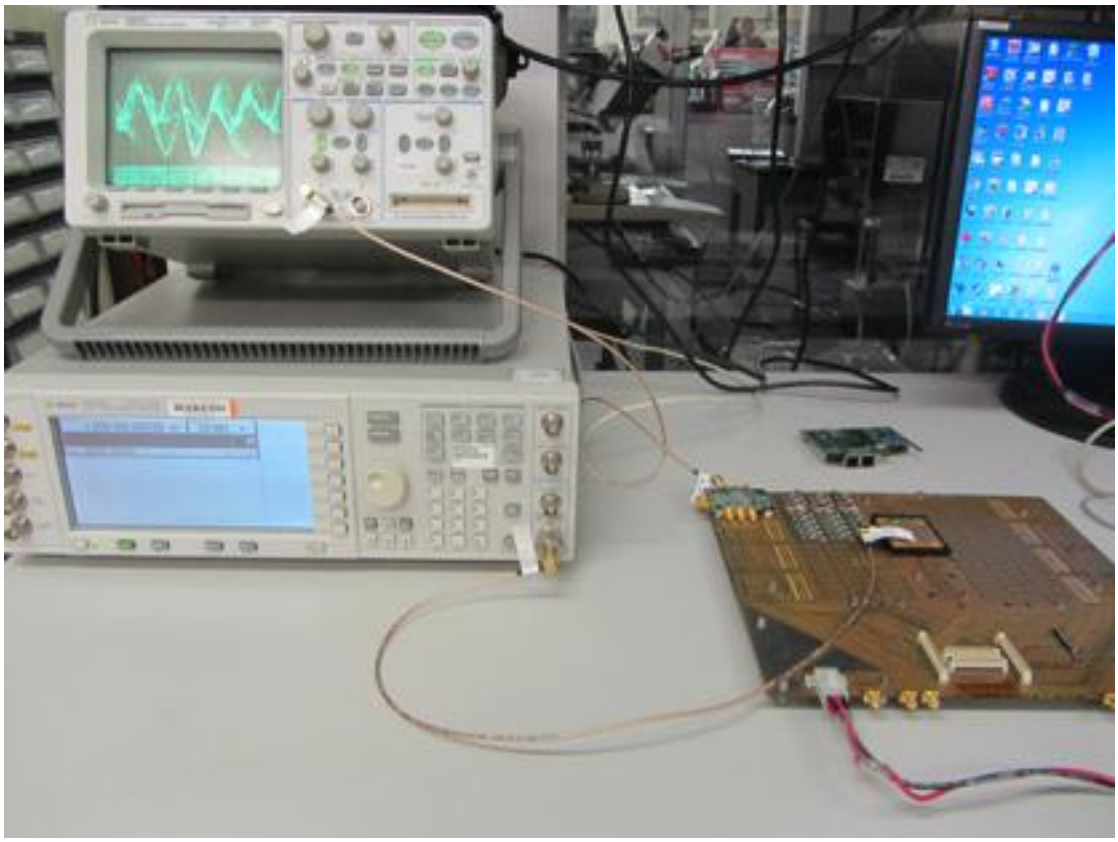

IMAGE 11. Amplifier testing when cards in motherboard

Removing one amplifier stage to the daughter card could be one option, but that means the motherboard and the daughter card needs to be redesigned and that will take time. With the carrier boards the amplifier cards were further away from each other than they are on the motherboard. By bringing the amplifier cards close enough to each other they started to oscillate. That is why with by putting one amplifier stage to daughter card the oscillation problem could be solved. The amplifier cards would be further away from each other.

6.2 Firmware

When the firmware was on the evaluation board, it was possible to do the testing with a software called the USB-tester. Image 12 presents the STURM2 evaluation board, which was used to develop the STURM2 firmware

IMAGE 12. STURM2 Evaluation board

The USB-tester is software made to Linux operating system. It has been made for testing the STURM2 firmware with the evaluation board. Figure 16 shows the USB-tester in progress.

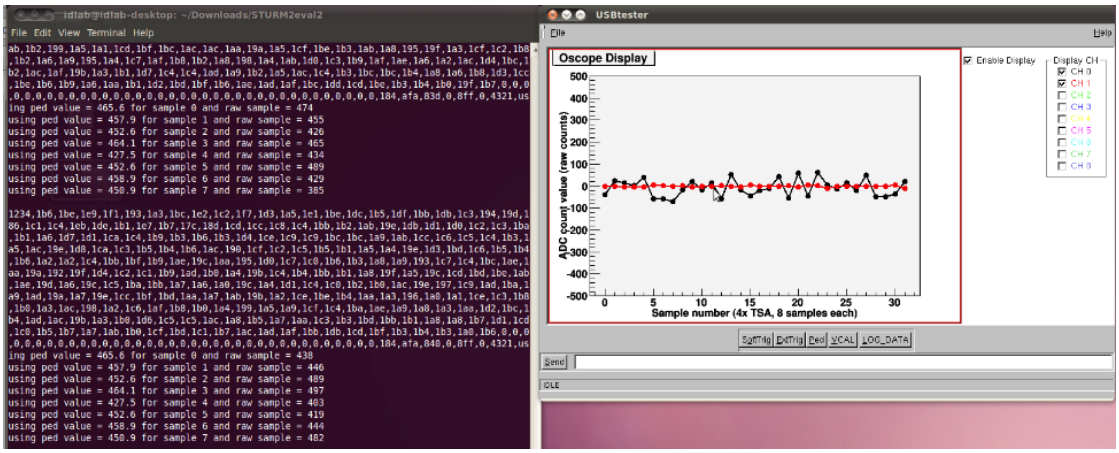

FIGURE 16. USB-tester software on Linux Ubuntu

With the USB-tester it was easy to get to known with the firmware by changing something in the code and analyzing the change. The main problem with the USB-tester is that it does not recognize the SCROD. The firmware can be tested with the USB tester, when the code is in the Evaluation board. When moving the code to the SCROD, the USB tester is not helpful anymore. After moving the existing firmware from the STURM2 evaluation board to the SCROD, testing needed to be done in some other way. Since the USB tester did not support the Spartan 6 FPGA, testing was made with ChipScope.

ChipScope is a testing tool under the ISE Xilinx designing program. ChipScope lets user to test one's works in little steps. With ChipScope it is easy to follow every signal or signals. In this thesis using ChipScope was minimum.

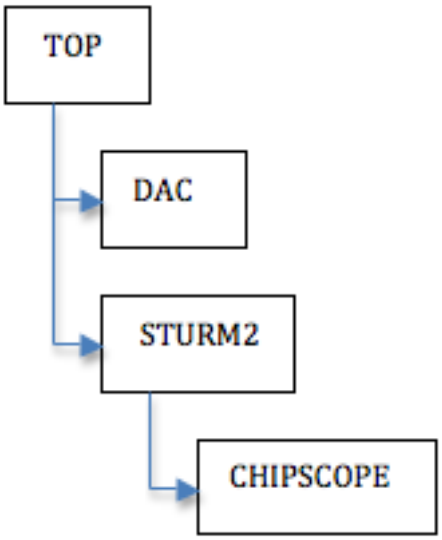

FIGURE 17. Part of the STURM2 Firmware Hiearchy.

The User can locate ChipScope anywhere. As shown in Figure 17, in this thesis the ChipScope is located under the STURM2_MAIN. Figure 18 presents the entity of the ChipScope.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity CHIPSCOPE_MON is
   generic(
      xUSE_CHIPSCOPE      : integer := 1);  -- Set to 1 to use Chipscope
   port(
      xCLK        : in  std_logic;
   -- ILA
      xMON        : in  std_logic_vector(31 downto 0);
   --ILA_DAC
      xDAC_MON    : in std_logic_vector (5 downto 0);
   --ILA_VDLY
      xVDLY_MON   : in std_logic_vector(96 downto 0);
   --VIO_TRIG
      xSOFT_TRIG  : out std_logic_vector (0 downto 0)
         );
end CHIPSCOPE_MON;

architecture Behavioral of CHIPSCOPE_MON is
   attribute BOX_TYPE   : string ;
```

FIGURE 18. ChipScope entity

Using the ChipScope requires a core in the code, which works as a component. The core can be done with the core generator just like the DCM. Used cores in the ChipScope can be either ILA or VIO. In this thesis the ILA is used. Neither of these cores can be used without ICON (Integrated CONtrol) core.
The VIO is virtual input/output, which lets user to control the part of the code when it is under testing. The ILA is Integrated Logic Analyzer that can be used for monitoring the code. When using only the ILA user cannot control testing. For example if monitoring the part of the code with the ChipScope where state does not change unless some signal changes, the user can use the VIO with that signal and see if the state changes. If not, user can analyse why and that is how it helps testing the firmware in pieces.

ChipScope's signals xMON are under STURM2_MAIN, xDAC_MON and xVDLY_MON are both under DAC_MAIN. Because the ChipScope is under STURM2_MAIN, the signals xDAC_MON and xVDLY_MON needs to go from STURM2 to DAC via TOP. Figure 19 presents the component of the ChipScope under STURM2_MAIN

```
component CHIPSCOPE_MON
generic(
   xUSE_CHIPSCOPE : integer := 1);  -- Set to 1 to use Chipscope
port(
   xCLK        : in  std_logic;
-- ILA
   xMON        : in  std_logic_vector(31 downto 0);
--ILA_DAC
   xDAC_MON    : in std_logic_vector (5 downto 0);
--ILA_VDLY
   xVDLY_MON   : in std_logic_vector(96 downto 0);
--VIO_TRIG
   xSOFT_TRIG  : out std_logic_vector (0 downto 0)
      );
end component;
```

FIGURE 19. The ChipScope in STURM2_MAIN needed to take as a component

```
xMON_HDR <= xMON(15 downto 0);
xMON(0)  <= xCH_SEL(0);
xMON(1)  <= xCH_SEL(1);
xMON(2)  <= xCH_SEL(2);
xMON(3)  <= xCH_SEL(3); --xPHASE_CNT(0);
xMON(4)  <= xSMPL_SEL(0);  --xPHASE_CNT(1);
xMON(5)  <= xSMPL_SEL(1);--xPHASE_CNT(2);
xMON(6)  <= xSMPL_SEL(2);
xMON(7)  <= xSMPL_SEL(3);
xMON(8)  <= xSMPL_SEL(4);
xMON(9)  <= xNRUN; --xsoft_TRIG; -- xEXT_TRIG;
xMON(10) <= START;
xMON(11) <= xTDC_START; --WILK
xMON(12) <= xTDC_STOP;
xMON(13) <= xTDC_CLR;
xMON(14) <= RAMP_DONE;
xMON(15) <= xCLK_10MHz; --xCLK;
xMON(16) <= xW_EN;
xMON(17) <= xCLR_ALL;
xMON(18) <= xDONE;
xMON(19) <= RAMPING;
xMON(31 downto 20) <= DATA;
xMON(31 downto 20) <= x"99" & xSTATUS;
xMON(31 downto 20) <= x"000";
```

FIGURE 20. This picture shows how the user can decide which signals one wants to monitor

Figure 20 shows which signals are followed in the xMON. The user can follow almost every signal in the code. Figure 21 shows which signals are followed in the xDAC_MON and xVDLY_MON.

```
xDAC_MON(0)           <= xCLK_10MHz;
xDAC_MON(1)           <= NSYNC;
xDAC_MON(2)           <= D_IN_0;
xDAC_MON(3)           <= D_IN_1;
xDAC_MON(4)           <= D_IN_2;
xDAC_MON(5)           <= UPDATE; --xMRCO;

xVDLY_MON(0)                <= xTST_OUT;
xVDLY_MON(12 downto 1)      <= VDLY0;
xVDLY_MON(24 downto 13)     <= VDLY1;
xVDLY_MON(36 downto 25)     <= VDLY2;
xVDLY_MON(48 downto 37)     <= VDLY3;
xVDLY_MON(60 downto 49)     <= VDLY4;
xVDLY_MON(72 downto 61)     <= VDLY5;
xVDLY_MON(84 downto 73)     <= VDLY6;
xVDLY_MON(96 downto 85)     <= VDLY7;
```

FIGURE 21. xDAC_MON and xVDLY_MON are both under the DAC_MAIN

The lack of time made ChipScope using minimum. With the ChipScope the whole firmware can be checked. In this thesis the ChipScope was used only for practising, for the digital analog conversion and checking the clock. It is easy to check with the ChipCope if the clock work as wanted. The ChipScope gives out an actual clock signal with the right frequency. With the digital analog conversion testing reliable results were not got because of the lack of time.

7 Conclusions

KEK organization works very hard to increase our knowledge of the birth of the universe. KEK will have the most powerful collider there has ever been, Super KEKB. The people at KEK are exploring deeper and deeper the questions of birth of earth with Super KEKB. Super KEKB will have 40 times greater luminosity than the earlier collider KEKB.

The monitoring device consists of the fermionics sensor, the ASIC cards, the amplifier cards, the SCROD and all these stand on the motherboard and the STURM2 chip is located on the bottom of the ASIC card. The motherboard, the ASIC card, the Amplifier cards and the SCROD are designed in the IDLab. First three are designed mostly by the foreign students, which give the students a special opportunity to travel abroad to study and to be a part of an international project.

The main principle of the device is that the X-ray is focused to the fermionics sensor, which after that gives out 35 µV. To gain 10 mV from 35 µV an 60 dB amplification is needed. To make this 60 dB amplification it was decided to use three 20 dB amplifiers and all on their own board.

The STURM2 chip is the core of the device and it is located in the bottom of the ASIC card. This chip takes the samples of the X-ray that is focused to the fermionics sensor. The sampling speed of the device is 10 giga samples per second. The STURM2 chip has 8+1 channels, which each have four storages and each of them holds eight samples. One STURM2 chip can hold 256 samples. The ASIC card also makes a 12-bit analog to digital conversion. The SCROD takes samples from the STURM2 chip and gives them to the computer. The actual firmware is on the SCROD.

Updates for the ASIC card and the firmware were necessary for many reasons. The firmware needed to be transferred from the STURM2 evaluation board to the SCROD. Because these two do not have the same FPGAs, transferring the code was rather complicated.

Some of the goals were reached in this thesis. The first thing to do was to make a new revision of the daughter card. The second goal was to transfer the firmware from the STURM2 evaluation board to the SCROD. The last goal was to test the device with the Free Electron Laser (FEL).

At the moment all the parts of the device have been manufactured and it is almost ready for FEL testing. Only a couple of things need to be finished. First, the amplification oscillation needs to be fixed. With amplification the rule of thumb is 40 dB inside of a box. When putting too much amplification inside of a box it starts to oscillate. Second, the firmware needs to be finished. The firmware is transferred from the STURM2 evaluation board to the SCROD and there are a couple of things that need to be fixed before it is ready for testing.

8 Further development

When the firmware works as wanted and the amplifiers do not cause oscillation the device is ready for the final hardware testing. The final hardware testing will be made in one of the laboratories in University of Hawaii at Manoa. The device is going to be tested with the FEL. The principle of this laser test is quite similar to how the device is going to be used in its final destination.

When a microwave beam is bent it emits X-rays and these X-rays are focused to the fermionics sensor. The main thing in this laser experiment is to see if the hardware works as wanted before it is used in a real collider.

9 REFERENCES

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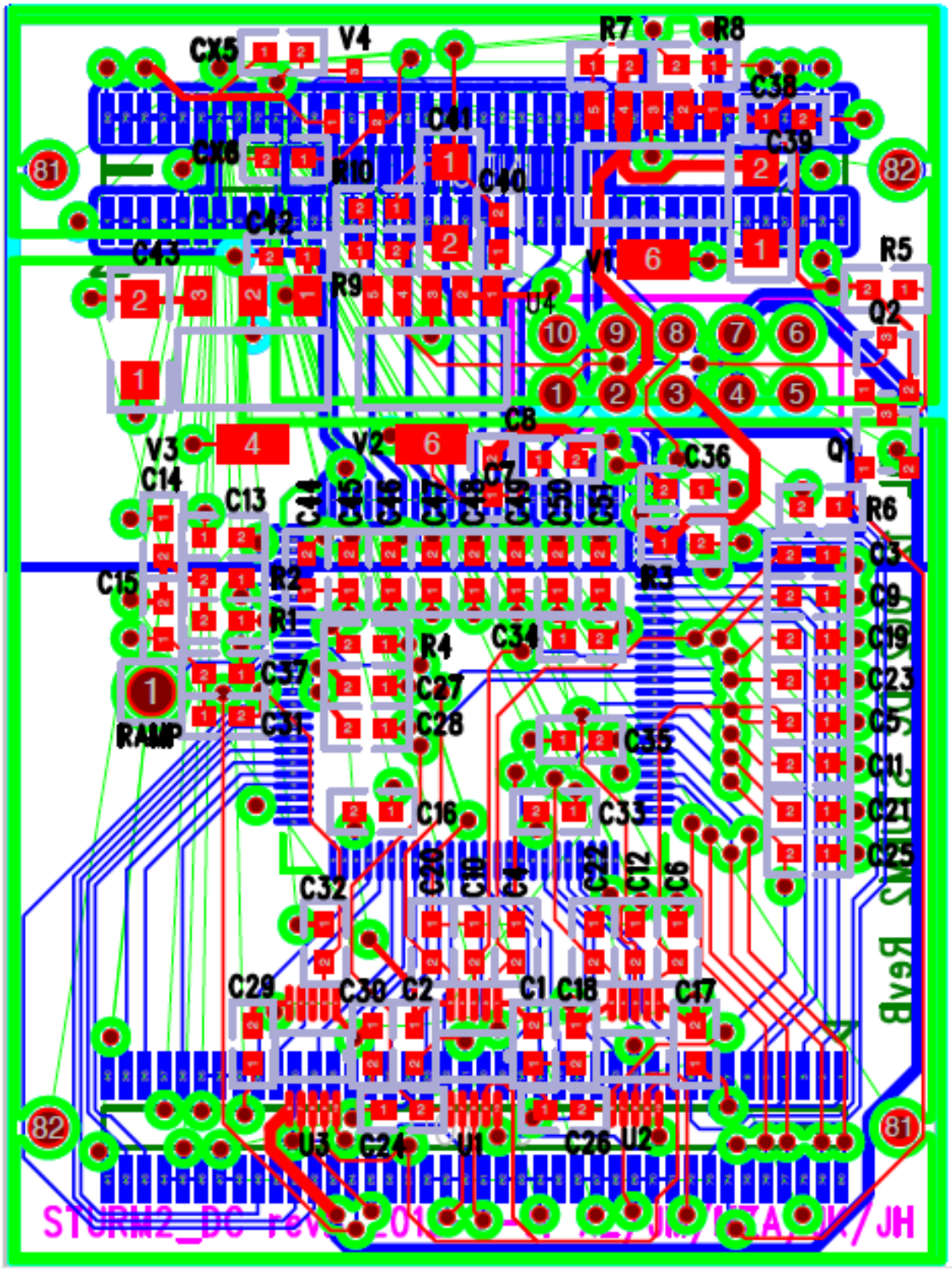
Varner, G. 2012. About my thesis and pictures
[email]. Recipients: Ari Parviainen, Janne J Himanen; Jussi J Kangaskoski; Lauri Karppinen; Vihtori L Virta. Sent 30 May 2012 [accessed 30 May 2012].

Appendix 1.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C39
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V3
V2
C8
C36
Q1
C14
C13
C7
R6
C15
R2
R3
C3
R1
R4
C34
C9
C19
C37
C27
C23
RAMP
C31
C28
C35
C5
C11
C16
C33
C21
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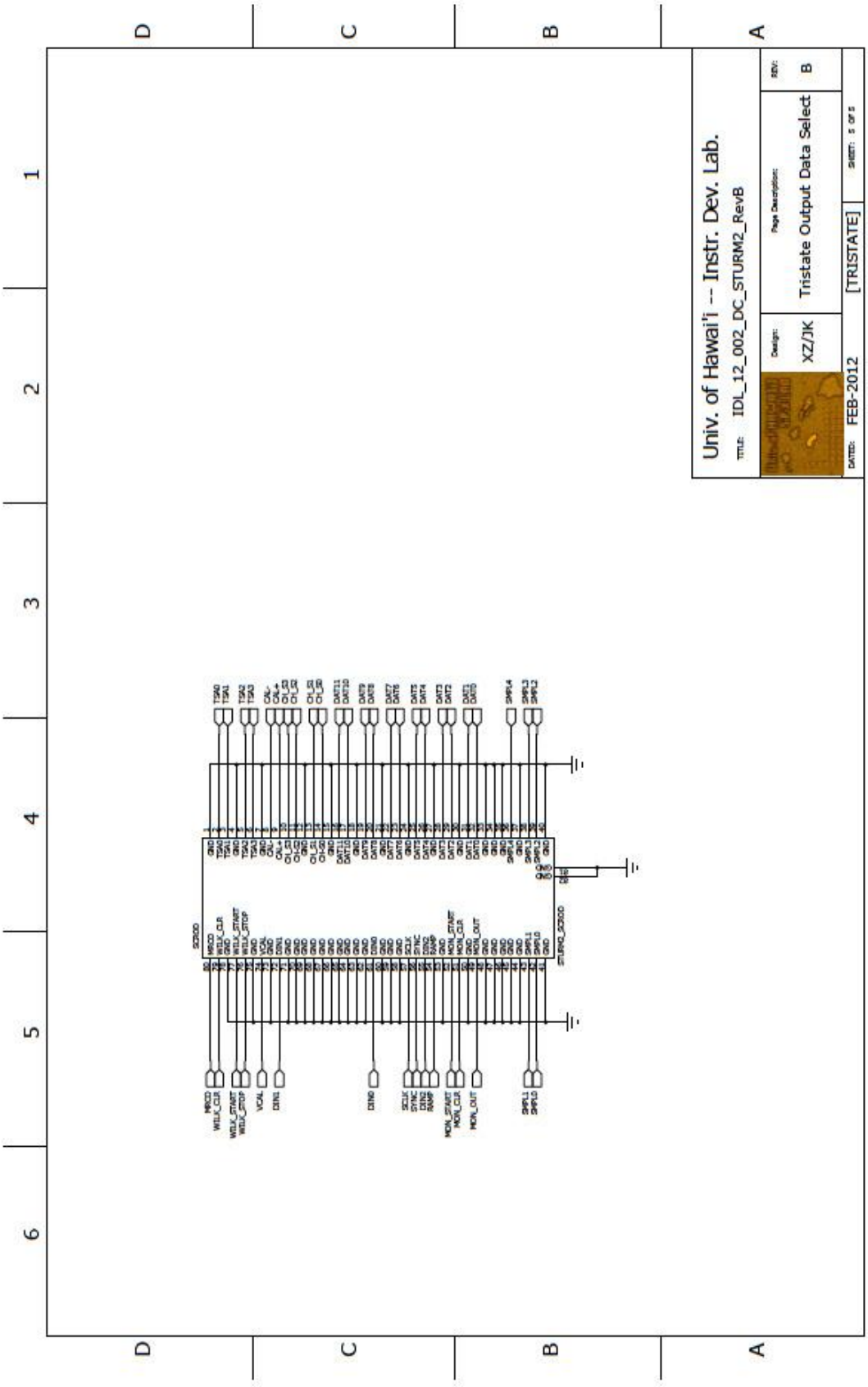
U2
Rev B

Appendix 2.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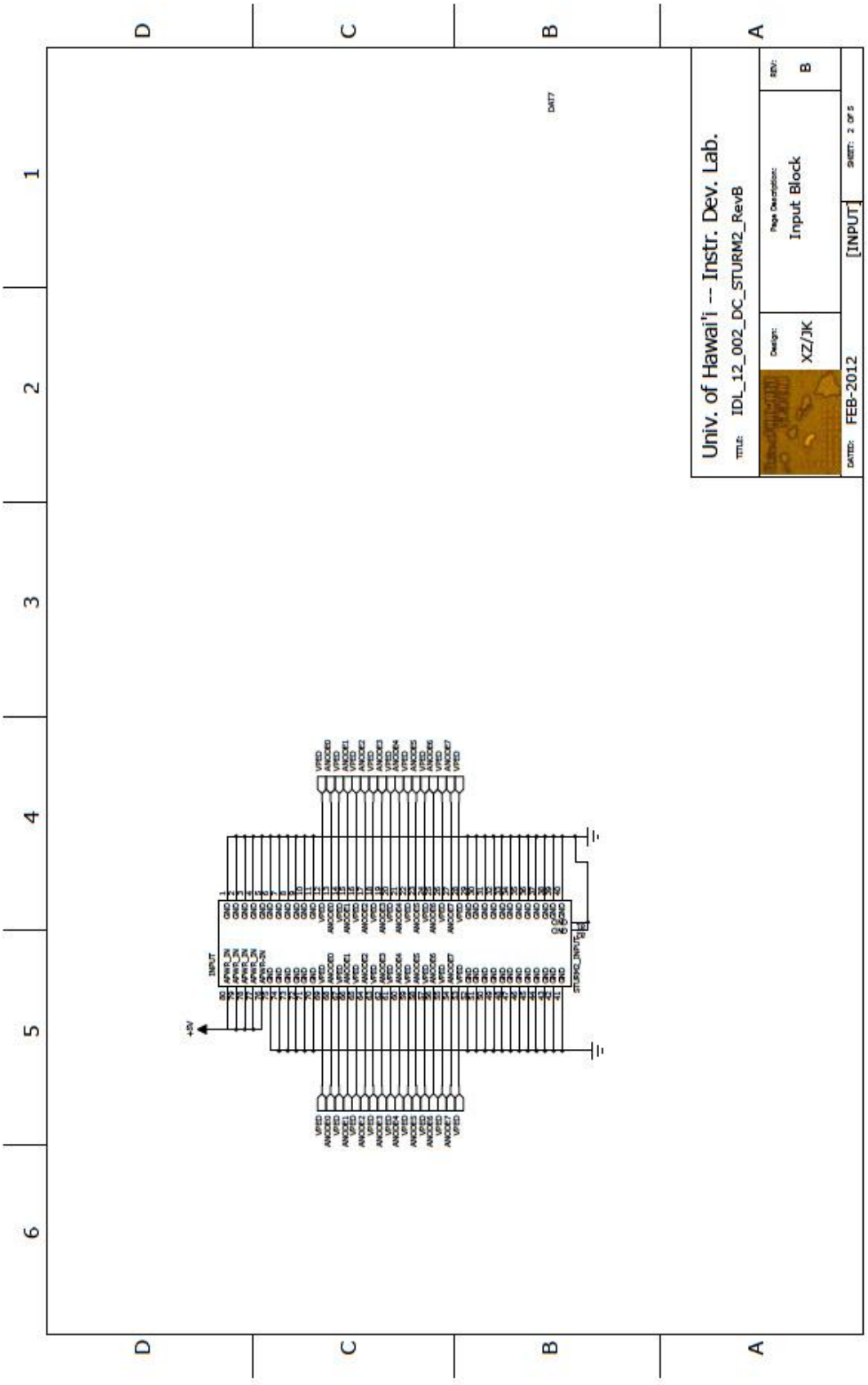
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STURM2_INPUTS
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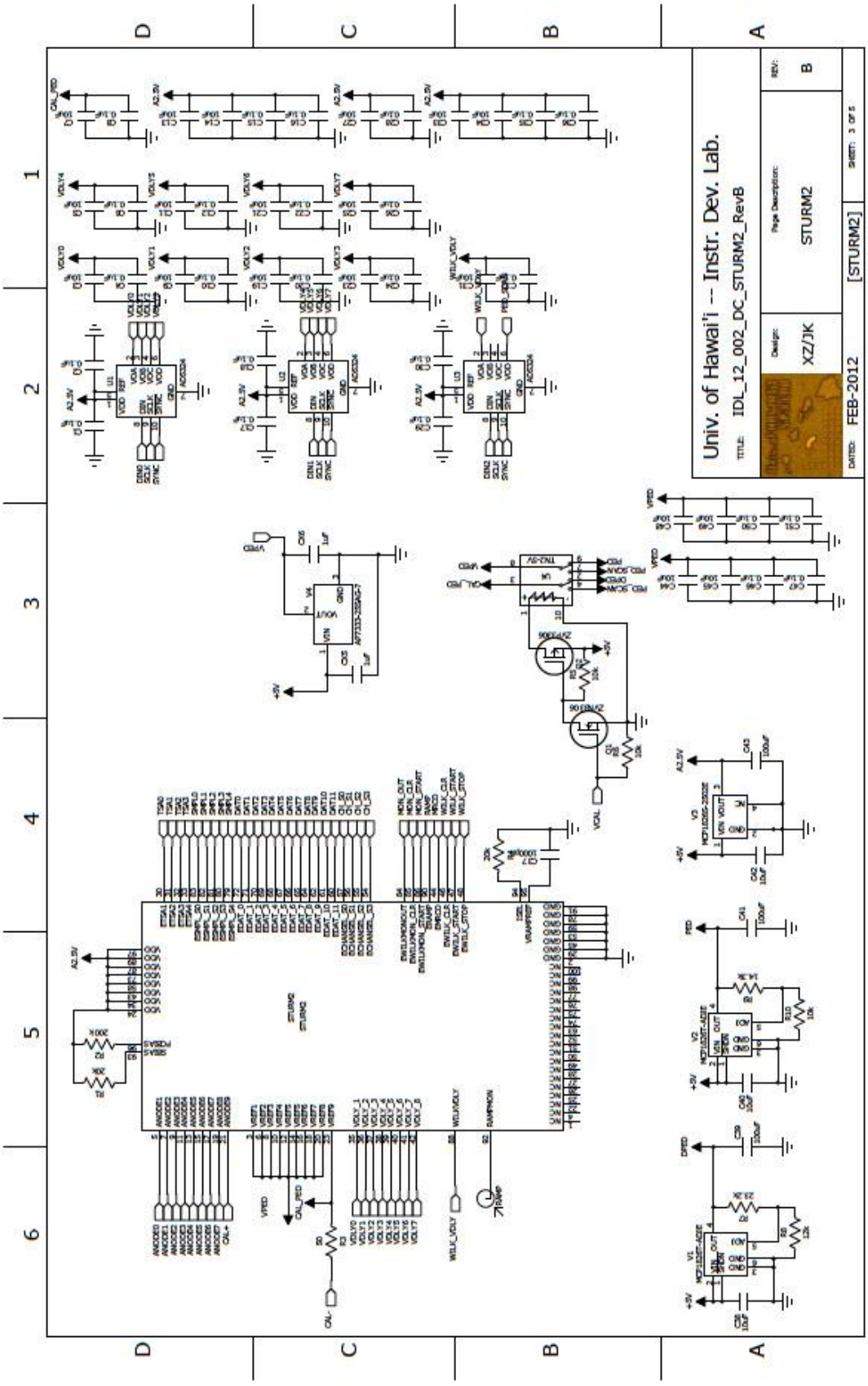
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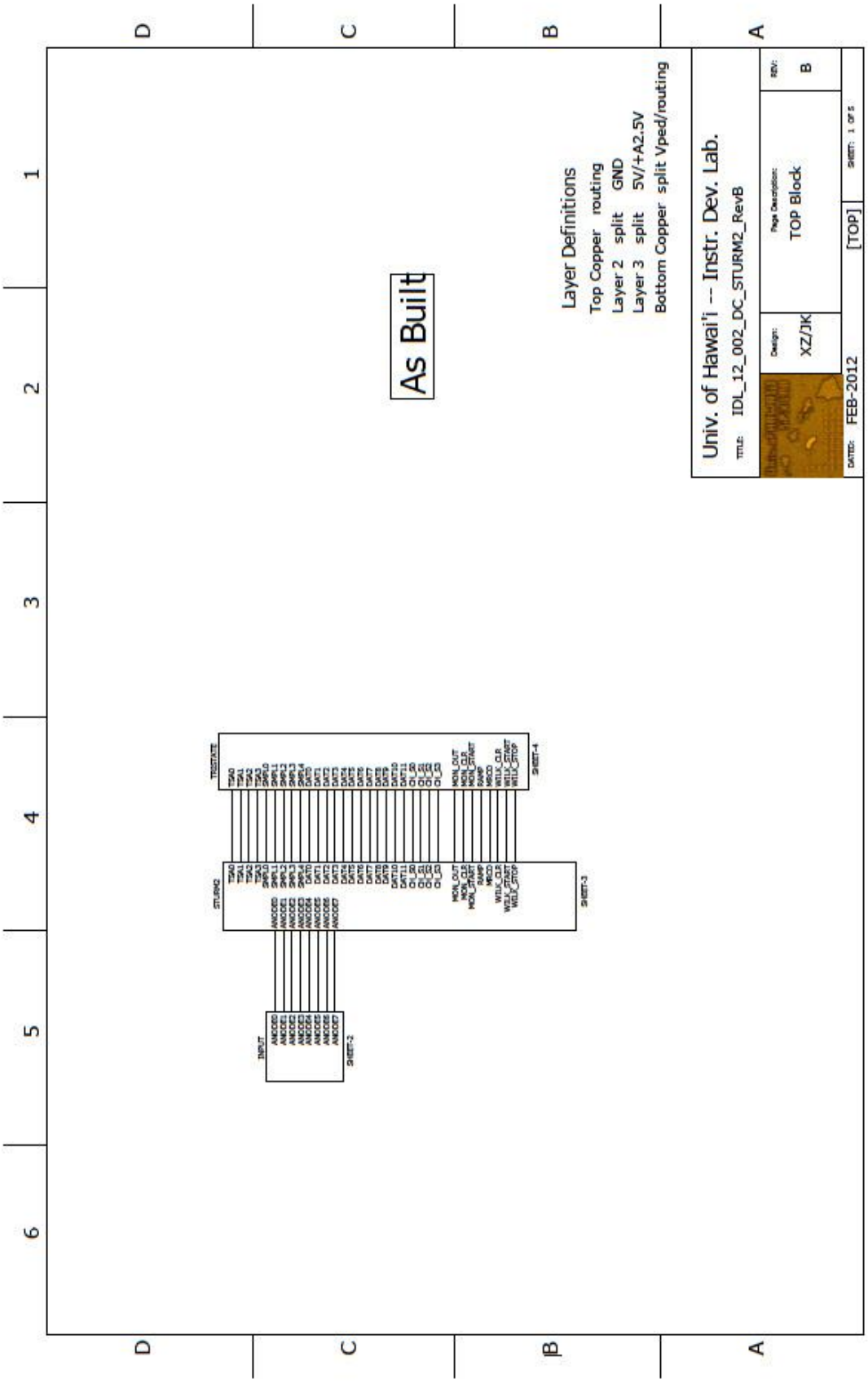
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Layer Definitions
Top Copper routing
Layer 2 split GND
Layer 3 split 5V/+A2.5V
Bottom Copper split Vped/routing
Univ. of Hawai'i -- Instr. Dev. Lab.
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DATED: FEB-2012
[TOP]
SHEET: 1 OF 5
INPUT
SHEET-2
STURM2
SHEET-3
TRISTATE
SHEET-4

Appendix 3.

QTY	Ref Res	Part Name	Manuf.	Descr.	Value
3	U1-3	AD5324			
1	V4	AP7333-25SAG-7			
25	C1-2 C4 C6 C8 C10 C12 C15-18 C20 C22 C24 C26 C28-30 C32 C35-36 C46-47 C50-51	CAP0603,0.1uF	IPC SM-782 STD.	0.031 X 0.061 INCHES	0.1uF
1	C37	CAP0603,1000pF	IPC SM-782 STD.	0.031 X 0.061 INCHES	1000pF
22	C3 C5 C7 C9 C11 C13-14 C19 C21 C23 C25 C27 C31 C33-34 C38 C40 C42 C44-45 C48-49	CAP0603,10uF	IPC SM-782 STD.	0.031 X 0.061 INCHES	10uF
2	CX5-6	CAP0603,1uF	IPC SM-782 STD.	0.031 X 0.061 INCHES	1uF
3	C39 C41 C43	CAP1206,100uF	IPC SM-782 STD.	0.062 X 0.126 INCHES	100uF
1	V3	MCP1826S-2502E			
2	V1-2	MCP1826T-ADJE			
3	R5-6 R10	RES0603,10k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	10k
1	R8	RES0603,12k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	12k
1	R9	RES0603,14.3k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	14.3k
1	R2	RES0603,200k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	200k
2	R1 R4	RES0603,20k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	20k
1	R7	RES0603,23.2k	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	23.2k
1	R3	RES0603,50	IPC SM-782 STD.	0.031 X 0.061 INCHES, 1/10W	50
1	STURM2	STURM2			
1	INPUT	STURM2_INPUT			
1	SCROD	STURM2_SCROD			
1	RAMP	TH_TESTPT			
1	U4	TN2-5V			
1	Q1	ZVN3306		ZVN3306	
1	Q2	ZVP3306F		ZVP3306	