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Integrated Circuit Testing Using Automatic Test Equipment

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Abstract

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Prompted by faulty devices in a small batch of PCM1808 analog-to-digital converters, the aim of this project was to develop a test setup and test program to perform incoming acceptance tests for the devices using automatic test equipment. The tests were to be able to establish the functionality and sufficient dynamic performance of the devices. The project was carried out for VLSI Solution Oy.

The basics of integrated circuit testing and the equipment used were explored. Analog-to-digital conversion and some analog-to-digital converter architectures were studied. Digital signal processing-based testing was researched. A device interface board was designed to allow the testing of the PCM1808 on automatic test equipment, and a test program for the tester was developed.

Devices from the batch with faulty devices and from another batch were tested. More faulty devices from the former batch were found, while the devices from the latter batch were all functional and performing to specification.

As a result of this project, incoming acceptance tests can be performed for future batches. As a future development, the testing should be automated by building a setup for a handler. Adding a wider range of tests to the test program should be considered.

Keywords: IC testing, ATE, Analog-to-Digital Converter, Digital Signal Processing

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Projektin tavoitteena oli kehittää testausjärjestely ja testiohjelma PCM1808-analogia-digitaalimuuntimien testaukseen automaattisella testauslaitteistolla vastaanottotestien suorittamiseksi. Tarve projektille syntyi viallisten komponenttien löydyttyä pienestä PCM1808-tuote-erästä. Testien tuli kyetä varmistamaan muuntimien toiminta ja riittävä dynaaminen suorituskyky. Projekti toteutettiin VLSI Solution Oy:lle.

Mikropiiritestauksen ja testauksessa käytettyjen laitteistojen perusteet selvitettiin. Analogia-digitaalimuunnokseen, analogia-digitaalimuunninarkkitehtuureihin ja digitaaliseen signaalinkäsittelyyn perustuvaan testaukseen perehdyttiin. Projektissa suunniteltiin ja valmistettiin piirilevy muuntimien liittämiseksi testauslaitteistoon testauksen ajaksi ja testauslaitteistolle luotiin testiohjelma testien suorittamiseksi.

Muuntimia testattiin viallisia komponentteja sisältäneestä erästä sekä uudemmasta erästä. Ensin mainitusta löytyi lisää viallisia komponentteja, mutta uudemmasta erästä kaikki testatut muuntimet läpäisivät testit.

Projektin tuloksena syntynyttä testausjärjestelyä ja testiohjelmaa voidaan jatkossa käyttää vastaanottotestien suorittamiseen. Testaus tulee vielä automatisoida suurempien määrien testaamisen mahdollistamiseksi. Laajempien testien lisäämistä testiohjelmaan tulee harkita.

Avainsanat:	Mikropiiritestaus, automaattinen testauslaitteisto, analogia-digitaalimuunnin, digitaalinen signaalinkäsittely

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List of Abbreviations

ADC: Analog-to-digital converter. A device that converts an analog signal to a digital representation.

ATE: Automatic/automated test equipment. A system that automatically performs tests on a device.

AWG: Arbitrary waveform generator. A device that can generate any electrical signal within its frequency and amplitude range.

DAC: Digital-to-analog converter. A device that converts a digital signal to an analog signal.

DIB: Device interface board. A circuit board that interfaces a device under test to the tester.

DUT: Device under test. An integrated circuit device on which tests are performed.

FFT: Fast Fourier transform. An efficient algorithm for computing the discrete Fourier transform of sampled data.

I2S: Inter-IC sound. A digital interface standard used for connecting audio devices together.

LSB: Least significant bit. The lowest-value bit of a binary number.

SNR: Signal-to-noise ratio. The ratio of the power of a test signal and the mean power of all other frequencies within the measured frequency band.

THD: Total harmonic distortion. The ratio of the combined power of all harmonic components to that of the fundamental frequency.

THD+N: Total harmonic distortion + noise. The ratio of the power of a test signal and the mean noise power plus the total power of the harmonic components of the test signal.

1 Introduction

In the electronics industry, it is often stated that the cost of finding a faulty circuit grows tenfold at every stage of product manufacture, from individual integrated circuit, to populated circuit board and so on. This is known as the Rule of Ten [1 pp. 44]. Indeed, diagnosing and changing a faulty or underperforming component in a completed product is time-consuming and expensive, so it is important to prevent them from entering the production line to begin with.

This project was carried out for VLSI Solution, an integrated circuit design and manufacturing company. After having issues with a small batch of PCM1808 analog-to-digital converters used in a DSPeaker product, it was decided that an incoming acceptance test would be implemented for the component to ensure its functionality and performance before printed circuit board assembly.

This thesis first introduces, in Section 2, some basic concepts in integrated circuit testing and the equipment used. Section 3 focuses on analog-to-digital converters. Analog-to-digital conversion and sampling theory are explained in brief. Common types of analog-to-digital converters are described, along with their typical uses and important performance characteristics. The section then covers how digital signal processing can be utilized in testing some of these characteristics. The implementations of a test setup and a test program for testing the PCM1808 analog-to-digital converter with automatic test equipment are then described, and results from testing the devices are presented. Finally, Section 4 provides conclusions and future development suggestions.

2 Integrated Circuit Testing

This section briefly explains some of the tests performed on integrated circuits (ICs) and introduces different types of integrated circuit testing. It then describes some of the common test equipment used in different phases of IC production.

2.1 Testing

Testing of integrated circuits is done to make sure that no faulty devices are shipped to customers. Every test follows this basic idea: apply stimulus, observe response. The stimulus can be something like a forced current through a diode, and the response would be its forward voltage.

There are wide varieties of DC and parametric tests, analog and sampled channel tests, and digital tests that can be performed on a device under test (DUT). DC and parametric tests include continuity, leakage and power supply currents, and tests for digital circuits such as input leakage currents and output voltages, to name a few. Analog and sampled channel tests are largely similar, with DSP-based testing being done using sampled channels in the source and capture instruments. Among these are gain, noise and distortion tests. Memory tests such as checkerboard and walking ones and zeros RAM tests, and scan tests such as partial or full scan, or JTAG 1149.1 boundary scan, though the latter is usually more geared towards board-level testing. A single DUT may go through thousands of these tests before being accepted for shipping. The final metric on which a production lot is assessed is lot yield, the percentage of good devices out of the total number tested.

The following chapters describe some of the contexts in which these tests are performed, and common equipment used.

2.1.1 Characterization

Characterization testing is done during prototyping and initial production runs to determine the conditions under which final production testing is to be performed. The tests are extensive, and the tests may be performed over a wide range of supply voltages, clock frequencies, loading conditions, temperatures and so on. These extensive tests are lengthy, making running full characterization tests in production economically unviable. From these tests, a subset is selected to make production testing as fast as possible while still catching all defective devices.

2.1.2 Production Testing

Once a product enters full production, every device will undergo production testing. Tests will be performed on each die on a wafer before packaging to avoid packaging defective dies, and again on packaged devices to make sure no defective devices are shipped.

Production testing may include grading of devices. A percentage of the passing devices may be particularly performant, allowing selling them at a premium, whereas the other devices, while fully functional, have lower performance and therefore lower value.

To make production testing as economical as possible, the test program is highly optimized for test time while maintaining as high a coverage as possible. An obvious way is to stop the test program at the first failed test. To further reduce test time, the test program is profiled to determine the time each individual test takes, and the tests are ordered based on the typical failure rate of each test in a way that minimizes the average time it takes to detect a defective device. Some ways to optimize the individual tests include minimizing required settling times, preparing subsequent tests while the tester’s array processor is processing captured data, and finding the right balance between test accuracy and test time, e.g. using a faster but less accurate instrument for a particular measurement if higher accuracy is unnecessary.

2.1.3 Incoming Acceptance Testing

A PCB manufacturer may perform incoming acceptance tests for components procured from a supplier prior to using them in a product. It can be done simply to verify that the component is functional, or compliant to the most important parts of its specification, as is the case in this project. Grading may be done to find particularly high-performing components to be used in devices with more stringent requirements than the minimum performance specified for the component. Another reason might be to select well-matched components for use in individual PCBs.

As test development by the IC manufacturer is a collaborative effort of both design and test engineers, comprehensive incoming acceptance testing of more complex IC devices such as microcontroller units may not be possible due to insufficient knowledge of the design.

2.2 Test Equipment

A variety of equipment is used in the testing of IC devices during different stages of manufacture. These range from bench equipment used in a laboratory during prototyping to ATE testers used with wafer probers after wafer fabrication and with handlers after individual dies have been packaged. The following chapters give an overview of some of the equipment used.

2.2.1 Bench Equipment

Bench equipment is used to measure some specific parameters in the lab. An evaluation card is often built to allow testing and debugging the device using bench equipment. An evaluation card may allow connecting the device to a variety of instruments, e.g. variable DC power supplies, oscilloscopes, spectrum analyzers, audio analyzers, or logic analyzers. It may also provide digital interfaces such as USB or UART for communication.

It is useful to verify ATE measurements using bench equipment. A discrepancy between bench measurements and measurements done on an ATE tester is often indicative of bugs in the ATE test program, or problems in the device interface board.

2.2.2 Automatic Test Equipment

There are different kinds of ATE testers optimized for testing the various types of integrated circuits: testers with limited analog measurement capabilities for digital devices, memory testers for memory devices, e.g. DRAM or non-volatile memories such as FLASH, for analog devices with high performance digitizers and waveform generators but limited digital capabilities, and mixed-signal testers with good capabilities for both digital and analog testing. [1 pp. 260]

A typical mixed-signal ATE tester, such as the one used in this project, comprises a workstation, a mainframe, and a test head. The workstation is the user interface used to debug test programs, and to operate production testing. The mainframe houses power supplies, calibration sources, measurement instruments, and a computer that runs the test program controlling the instruments. The test head contains instruments that need to be close to the DUT, such as high-speed digital channel cards. A device interface board (DIB), designed for a specific device or family of devices, is attached to the test head to interface the DUT with the tester. A manipulator, either separate or built into the mainframe, is used to position and dock the test head and DIB to a wafer prober or a handler unless a manual test socket is used e.g. for debugging the test program.

A wide variety of instruments are commonly found in a mixed-signal tester. These include programmable DC sources for forcing voltage or current, DC meters for voltage and current measurements, relay matrices for flexible connections of the various instruments to the DIB, relay control lines for controlling relays placed on the DIB, low and high frequency arbitrary waveform generators for stimulating the DUT with e.g. sine waves, multitone signals or ramps, waveform digitizers for capturing analog waveforms from the DUT, a

time measurement system for measuring parameters such as frequency, jitter and rise and fall times, a digital subsystem for testing digital logic by driving or comparing the DUT's input and output pins and for capturing their output, and calibration sources used to calibrate the various instruments to ensure the measurements stay within specifications. It is also possible to connect external bench instruments to the tester and control them through a General Purpose Interface Bus (GPIB) or universal asynchronous receiver-transmitter (UART).

2.2.3 Wafer Probers

Once a wafer has been fabricated, it is tested before dicing and packaging to avoid the cost of packaging faulty devices. This is done with a wafer prober connected to an ATE tester. The prober steps through the wafer, bringing each die in contact with the needles or spring contactors of the probe card for testing. To reduce total test time, the probe card may contact multiple dies per touchdown for parallel testing, and even full wafer contact is possible [3]. Wafer probers may have temperature forcing capability to allow testing in low or high temperatures, e.g. −40 °C or +85 °C, a common temperature range for industrial applications.

After touchdown, the prober signals the tester that it is ready to test, and the tester runs the test program. The prober then receives binning from the tester, and defective dies may be marked with ink to be discarded, but a more modern approach is to create a wafer map with full binning information of each die.

Wafer maps are also used for analysing the distribution of different defects over the area of the wafer, which may reveal problems in the fabrication process. It may be possible to improve yield by test program debugging or process adjustments or reveal a need for design changes to make the design less sensitive to process variations. [2 pp. 82]

2.2.4 Handlers

After packaging, the devices go through final test. It is done to verify that all bond pads are connected, the devices were not damaged in the packaging process, and their performance did not shift.

A handler picks untested devices from trays or tubes and places them into the contactor. After running the test program, the ATE tester sends binning to the handler, and the handler sorts the devices back to trays or tubes accordingly. Some handlers are capable of placing multiple devices to contactors of a multi-site device interface board at the same time, allowing parallel testing of devices. Like wafer probers, handlers may be capable of temperature forcing.

After final test the devices are baked in accordance with the standard IPC/JEDEC J-STD-033 before dry packing to drive out any moisture they have absorbed from the ambient environment. This is done to prevent popcorning, the rapid formation of steam within the package during the soldering process, possibly damaging the device [4].

3 Analog-to-Digital Converter Testing

This section starts by introducing the basics of analog-to-digital conversion and sampling theory and describes some ADC architectures, their common uses, and key parameters in the different use cases and how they are tested. The application of digital signal processing (DSP) in testing is then covered. Finally, the device interface board and test implementations for testing the PCM1808 ADC using an ATE tester are explored, and the results are presented.

3.1 Analog-to-Digital Conversion

Analog-to-digital conversion is the process of converting an analog signal into a digital representation. The analog signal can be something static like the voltage of a battery, or something that changes over time like the electrical signal from a microphone or the radio antenna of a WiFi access point.

Some of the countless applications include measuring instruments and data loggers where the analog signal from a sensor such as a temperature or a humidity sensor is converted for display and storage in digital form, digital cameras where the voltage of each pixel of an image sensor is converted to produce a digital image, and audio applications where a continuous-time, continuous-amplitude signal is converted to produce a digital audio recording, or for digital signal processing like the analog-to-digital converter (ADC) tested in this project.

The digitization of a continuous signal is called sampling. The level of the signal is sampled, or quantized, at a regular rate, known as the sampling rate or sampling frequency. The analog signal can be reconstructed from the samples.

According to the Nyquist–Shannon sampling theorem, the sampling frequency must be at least twice the highest frequency component, called the Nyquist frequency, of the signal to avoid aliasing. Aliasing is distortion caused by a frequency component being above the Nyquist frequency, appearing as if it were of lower frequency, as illustrated in Figure 1 below. In practice aliasing is

avoided by using a somewhat higher sampling frequency than twice the highest frequency of interest to allow effective low-pass filtering to eliminate aliasing.

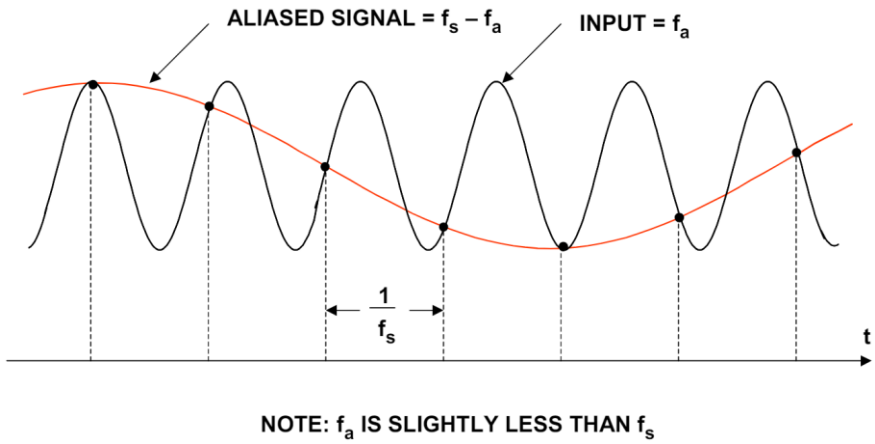

Figure 1. Aliased signal. [5 pp. 2.28].

Another key aspect of sampling is resolution, or bit depth. It is the number of bits a sample is quantized to. As the continuous-amplitude signal has infinite levels, but is quantized to a finite number of bits, it cannot be represented exactly, as shown in Figure 2 below.

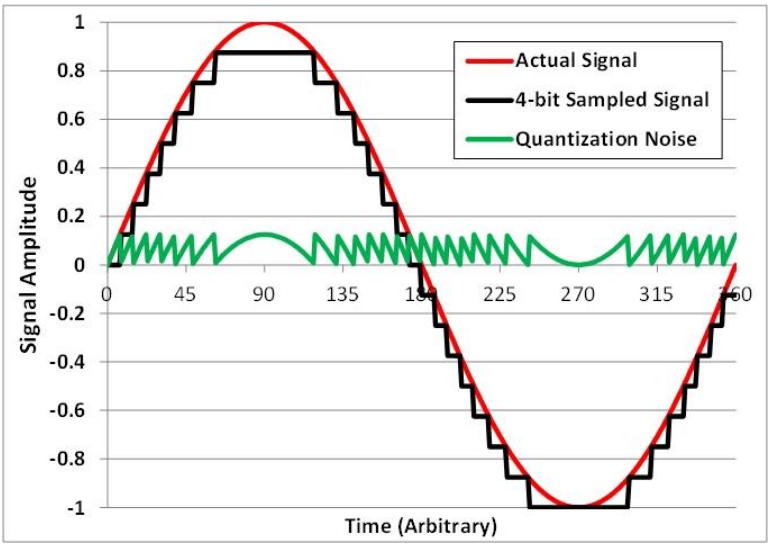

Figure 2. Quantization noise. [6].

As can be seen in Figure 2, the sampled signal differs from the original signal. This introduces what is known as quantization noise in the digital signal.

Jitter, the imprecision of the clock controlling the sampling, causes the signal to be sampled at irregular intervals. As the signal level is continuously changing, a sample taken at the wrong point in time may be quantized to a different level than it otherwise would have. This sampling jitter is another source of noise in the digital signal.

3.2 Analog-to-Digital Converters

There are numerous ADC architectures. Some are more well-suited to certain applications than others due to their inherent advantages and disadvantages. A few architectures will be described in this chapter.

A flash ADC, shown in Figure 3 below, consists of an array of comparators, a string of resistors and a combinational logic block. The string of resistors is connected to a reference voltage, and one of each comparator's inputs is connected to a point in the string to provide a different threshold for every comparator, and the other to the input signal. The outputs are connected to the logic block to convert the combined outputs to binary format. An n-bit flash ADC requires n^2-1 comparators, so the size and power consumption of the ADC will grow very fast as the resolution increases, limiting the resolution practically achievable with this architecture. Owing to its speed, it is often used in radar processing, oscilloscopes, and magnetic storage applications. [7]

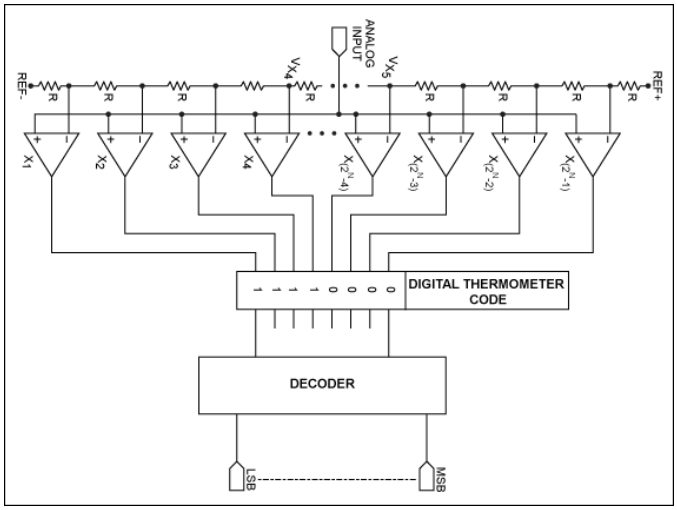

Figure 3. Flash ADC architecture. [7].

A successive-approximation ADC, in Figure 4 below, consists of a sample-and-hold (track/hold) circuit, a comparator, an internal n-bit digital-to-analog converter (DAC), and a register to store the approximation at each step of the conversion process. It performs a binary search by comparing the output of the internal DAC with the original input, changing the DAC output until a matching binary value is reached. At each step the value is stored in the register. Its resolution is determined by the resolution of the internal DAC. Unlike the flash ADC, its power consumption scales with the sampling rate. The need to perform multiple cycles of approximation and comparison limits its sampling rate. It is used in a wide variety of applications, such as data acquisition, test equipment and telecommunications. Its small size and low power consumption make it particularly suited for use in battery-powered equipment. [8]

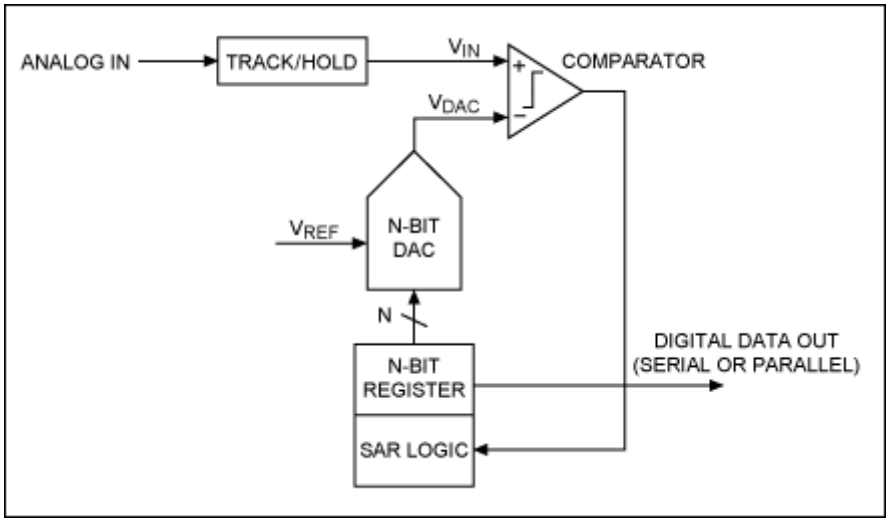

Figure 4. Successive-approximation ADC architecture. [8].

A pipelined ADC, a 12-bit example shown in Figure 5 below, consists of two or more quantization stages and time alignment and digital error correction logic. Each stage preceding the final stage comprises a sample-and-hold circuit, a low-resolution flash ADC and DAC, an analog subtractor circuit, and an amplifier. The input is quantized by the flash ADC, and the coarsely quantized signal is reconstructed by the DAC whose output is subtracted from the original input in the sample-and-hold circuit. The difference is then amplified and passed on to the next stage. The last stage simply resolves the remaining difference.

Each stage passes the bits from its flash ADC to the digital logic. After a stage has completed its operation, it is ready to process the next sample. This pipelined nature of the ADC gives it a high throughput, but causes a data latency of a few clock cycles, dependant on the number of stages. Pipelined ADCs can achieve higher resolutions at lower power consumption than flash ADCs, but at lower sampling rates. They are often used in digital imaging and video as well as networking applications. [9]

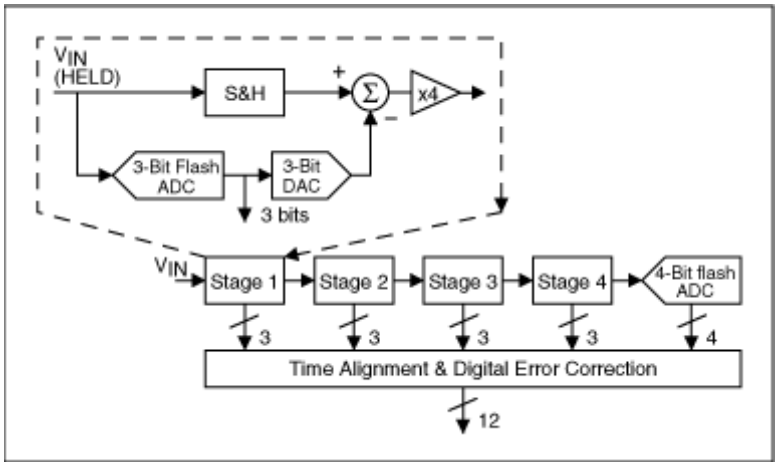

Figure 5. Pipelined ADC architecture. [9].

A sigma-delta (or delta-sigma) ADC, shown in Figure 6, is an oversampling ADC consisting of a sigma-delta modulator, a digital filter, and a decimation filter. The simplest sigma-delta modulator is a negative feedback loop comprising a difference amplifier (delta), an integrator (sigma), and 1-bit ADC and DAC. The difference amplifier subtracts the output of the feedback DAC from the input signal. Its output is then fed to the integrator whose output changes towards the positive or negative direction depending on the sign of its input at a rate dependant on the magnitude of its input. The integrator's output is then quantized by the 1-bit ADC and passed to both the feedback DAC as well as the digital and decimation filter. For each final output sample, the input signal is sampled multiple, often hundreds of times by the converter. This allows the use of a simple, low-order anti-aliasing filter. Sigma-delta ADCs with more difference amplifier and integrator stages and higher-resolution ADCs and

DACs exist. The architecture is used extensively in relatively low-frequency, high-resolution applications such as scientific instruments and audio. [10]

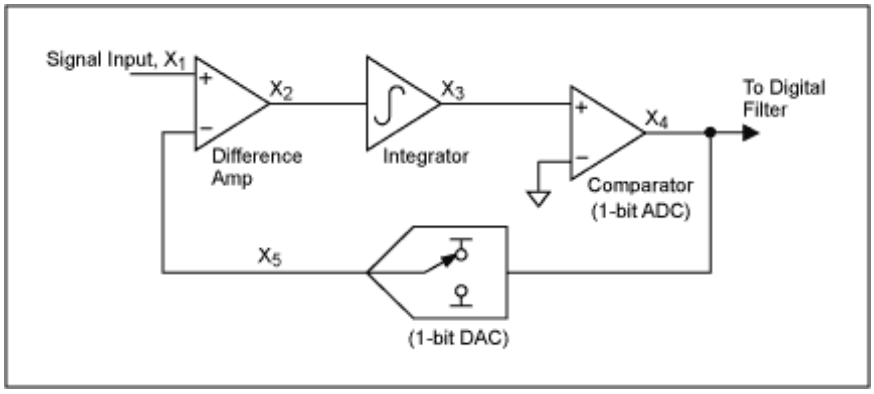

Figure 6. Sigma-delta ADC architecture. [11].

3.3 Digital Signal Processing-Based Testing

As both the AWGs and waveform digitizers found in mixed-signal ATE testers are sampled channels, digital signal processing (DSP) techniques are used extensively in mixed-signal IC testing. DSP allows the separation of signal components, filtering, and other signal manipulations. This makes it possible to perform multiple measurements in parallel. In this chapter, the coherent signals and repetitive sample sets, as well as some test techniques in the frequency domain will be introduced.

3.3.1 Coherent Signals

A coherent signal is a signal where an integer relationship exists between all its frequencies and the sampling rate. When a single period of the signal is repeated, the transition from the last sample to the first sample is seamless. In a non-coherent signal, there is a discontinuity between the last and the first sample when the signal is repeated, an example of which is shown in Figure 7.

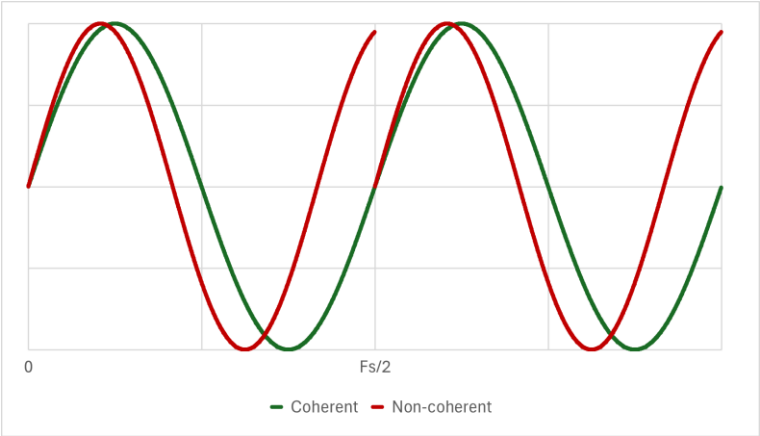

Figure 7. Coherent and non-coherent signals.

The Fast Fourier Transform (FFT) is often used to convert the signal to a representation in the frequency domain for analysis and frequency-domain filtering. The FFT operates on the assumption of a repeating signal. When FFT is performed on a non-coherent signal, a discontinuity will introduce spectral leakage, or aliased components whose energy will spread over the frequency spectrum, illustrated in Figure 8.

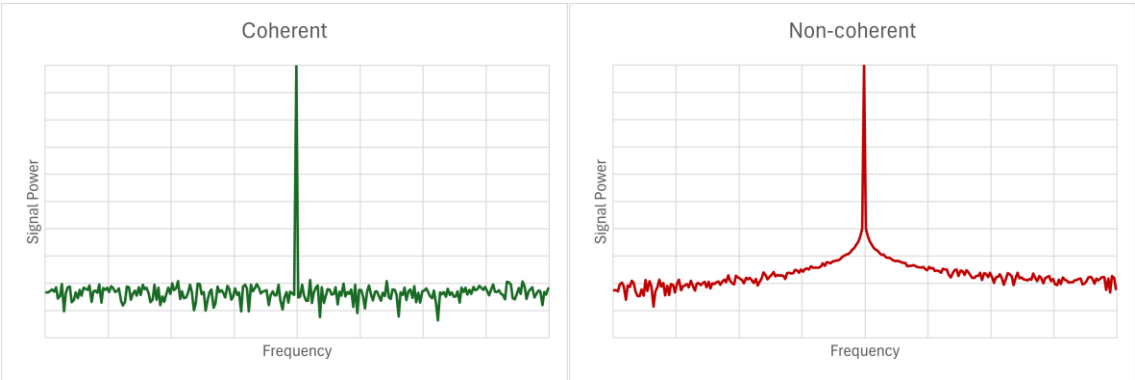

Figure 8. Frequency spectrum of a coherent (left) and a non-coherent signal (right).

As can be seen in Figure 8, the noise floor appears to have risen across the frequency spectrum of the non-coherent signal, especially near the sine wave's frequency bin. If coherent signals cannot be achieved, windowing can be used to reduce the effect of spectral leakage. In the example in Figure 9 below, the

commonly used Hann (often called Hanning) window is used to smooth a non-coherent signal.

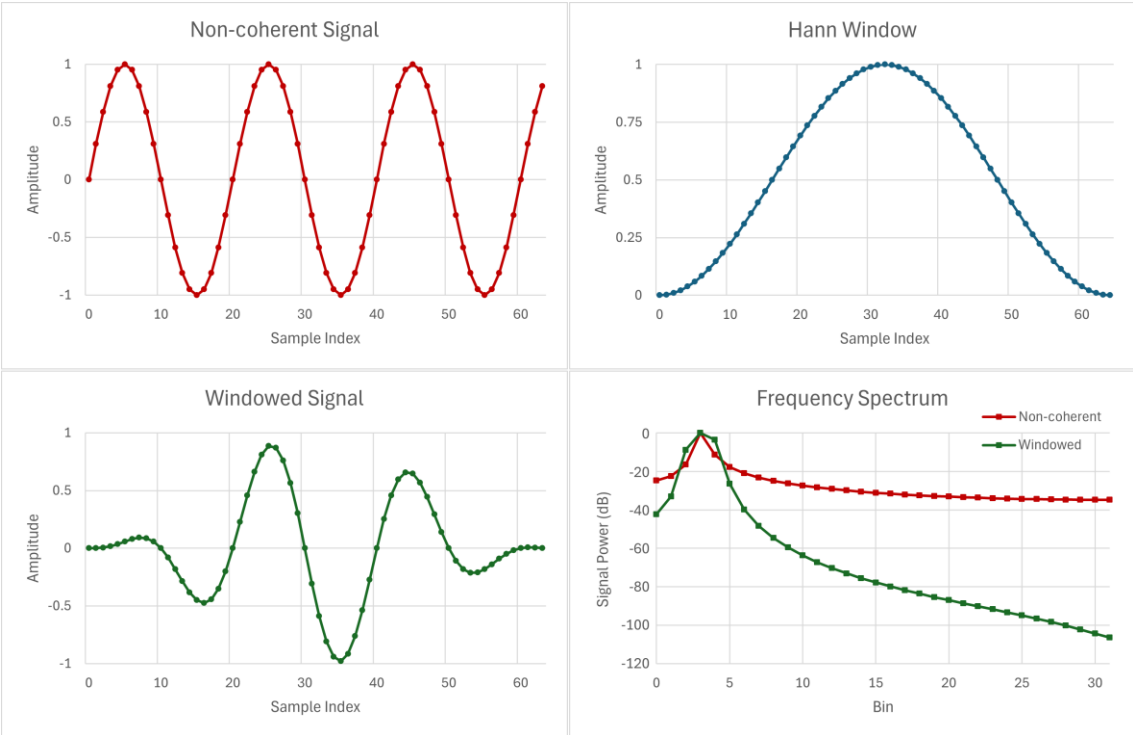

Figure 9. Applying the Hann window to a non-coherent signal.

As Figure 9 shows, the window function forces the signal towards zero at both ends to eliminate the discontinuity, mitigating the spectral leakage. However, it reduces frequency resolution, visible as a wider peak in the spectrum, so coherent signals should be used whenever possible.

The clocks of the analog and digital instruments of an ATE tester can be controlled extensively. By extension this allows controlling the sampling rate of an ADC (or DAC) under test, enabling coherent sampling from tester to DUT and back to tester, eliminating spectral leakage.

When N samples are collected at a sampling frequency F_s, the resulting period is called the unit test period. The frequency, F_s/N, is the fundamental frequency, also known as the frequency resolution. Only integer multiples M up to $N/2$ of

the fundamental frequency are coherent. These FFT is divided into these frequency bins.

When selecting frequency bins for test tones, the bin number *M* should be mutually prime with the number of samples *N*, i.e. they should not have common factors. A mutually prime bin may cause periodic errors in the quantization noise of the signal instead the errors being randomly distributed, or in the case of multitone signals, non-mutually prime bins are more likely to cause test tones and harmonic and intermodulation distortion components to overlap, leading to measurement errors [2 pp. 276].

3.3.2 Frequency Domain

As discussed in Chapter 3.3.1, the FFT is used to manipulate and analyze signals in the frequency spectrum. It allows performing various parametric tests and filtering operations on the signals.

Filtering is also possible in the time domain by convolving the filter's impulse response with the signal but is rarely done as the frequency spectrum will be already available for the various tests, and it is simpler and faster in the frequency domain, where it is performed by simply multiplying the signal's frequency spectrum with the filter's frequency response. If a filtered time-domain signal is needed, an inverse FFT can be performed on the frequency-domain filtered signal, though this is usually unnecessary. [2 pp. 337]

Signal-to-noise (SNR) is the ratio of the power of the test tone and the mean noise power, expressed in dB. In the frequency domain, it is calculated by dividing the power of the test tone bin with the mean power of all other bins excluding the harmonic (integer multiples of the test tone) bins and the DC bin.

Total harmonic distortion (THD) is the ratio of the power of the test tone and the total power of its harmonic components, or sometimes the reciprocal, expressed in dB. It is calculated by dividing the power of the test tone bin by the sum of the powers of the harmonic bins.

Before measurements, the signal may be filtered in some ways. For example, the test tone's harmonic components will be discarded for SNR calculation. This can be done by zeroing the harmonic bins of the power spectrum.

A-weight filtering is commonly used in audio applications where the SNR is often specified as an A-weighted measurement. The A-weighting curve approximates the human hearing's sensitivity at different frequencies, dropping when the frequency goes down from 1 kHz, being somewhat heightened from 1 kHz to 6 kHz, where it starts dropping again. The filter is applied by multiplying the magnitude of the spectrum by the magnitude of the filter. An example of this is shown in Chapter 3.6.3.

3.4 Device Under Test

The device for which a test setup and a test program for incoming acceptance test was implemented is the Texas Instruments PCM1808 24-bit analog-to-digital converter designed for use in audio applications. It is a single-ended stereo device that uses a sigma-delta modulator. The DUT can be configured to output 24-bit PCM data in two formats, I2S or left-justified, in either master or slave mode. It supports sampling rates from 8 kHz to 96 kHz, and system clock frequencies in three different multiples of the sampling rate. [12 pp. 1]

The DUT was to be tested to verify that it functions correctly, and that its dynamic performance was withing acceptable limits in a configuration similar to the end product. In the end product, the DSPeaker Anti-Mode X2 room correction device, it is used to convert an analog input signal to digital for real time processing.

The DUT has 14 pins, listed in Table 1, that need to be electrically connected to the ATE tester.

Table 1. DUT pins and their descriptions.

Pin number	Pin name	Description
1	VREF	Reference voltage decoupling
2	AGND	Analog ground
3	VCC	Analog power supply, 5 V
4	VDD	Digital power supply, 3.3 V
5	DGND	Digital ground
6	SCKI	System clock input
7	LRCK	Left-right clock input or output
8	BCK	Bit clock input or output
9	DOUT	Audio data output
10	MD0	Audio interface mode select 0
11	MD1	Audio interface mode select 1
12	FMT	Audio interface format select
13	VINL	Analog input, left channel
14	VINR	Analog input, right channel

As can be seen from Table 1, testing the device requires a few different kinds of instruments: power supplies, digital channels, and analog signal sources. These will be described in the following chapters.

3.5 Device Interface Board

As part of the project, a device interface board was designed and manufactured to interface the DUT with the ATE tester’s instruments, with additional circuitry. The DIB has a contactor that doubles as a manual socket when fitted with a knob that presses the DUT pins against the contactor. A number of relays controlled by the tester’s relay control lines are used to connect and disconnect large decoupling capacitors and tester instruments, as well as to change the circuitry in other ways during test program execution. The DIB’s design will be explored in the following chapters.

The DIB connects to the test head via a coaxial ribbon cable and a board that attaches to the test head. This is to make it easier to use with one of the company's prototyping handlers.

Finally, board check tests were developed to verify that the DIB is fully functional and will not cause good devices to fail tests. They are run once after loading the test program for the DUT, and any faults will be reported to the operator. The tests for each part of the DIB are explained in their respective chapters.

3.5.1 Power Supply Pins

To power the DUT, its two power supply pins, the 5-volt VCC and 3.3-volt VDD, must be connected to the tester's power sources. A diagram of the VDD pin's circuit is given as an example in Figure 10. The VCC pin's circuit is functionally identical.

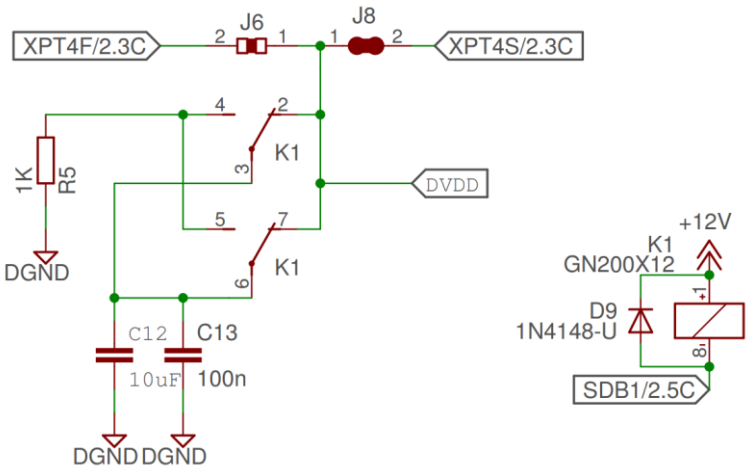

Figure 10. VDD pin's connections to a DC matrix line (XPT4) and to a capacitor via a relay (K1), and the relay's control line (SDB1).

As can be seen from Figure 10, the power supply pin is connected to the tester's DC matrix that will be used to connect a programmable DC power supply to the pin. These supplies can be programmed to force either current or voltage, and the tester's meter can be connected to them for voltage or current

measurements. Both power supply pins have a 100 nF decoupling capacitor placed very close to the pin, and two capacitors, 10 µF and 100 nF, that can be disconnected by a relay to speed up continuity testing. AGND and DGND pins are connected directly to analog ground and digital ground respectively.

The board's power supply circuitry is tested by first measuring the capacitance with the large capacitors disconnected, then closing the relay and measuring the capacitance again. Equation 1 below shows one way to determine capacitance.

$$C = \frac{\mathrm{I} \times \Delta \mathrm{t}}{\Delta \mathrm{V}} \tag{1}$$

Based on Equation 1, the capacitance can be measured by charging a capacitor to a known voltage, then discharging it for a set time, Δt, by forcing a constant current, I. A current proportional to the expected capacitance is used. The voltage after discharging the capacitor, ΔV, is measured, and the capacitance is calculated according to Equation 1.

3.5.2 Digital Pins

In total there are seven digital pins on the DUT: two mode pins, a data format select pin, three clock pins, and a data output pin. All digital pins are connected to the tester's digital channels. The digital channels are equipped with per-pin measurement instruments that can force voltage and measure current, or vice versa. They can be used for fast continuity and leakage testing.

The two mode pins, MD0 and MD1, are used to select between master mode with system clock operation at 256, 384 or 512 times the sampling rate, and slave mode with system clock rate autodetection [12 pp. 14]. Slave mode is used in the end product. There it is set by pulling the pins low with pulldown resistors, but the tester's digital channels allow selecting any mode by driving each pin high or low.

As with the mode pins, in the end product the data format select or FMT pin is pulled low with a pulldown resistor, selecting the I2S format, but the format can be freely selected when testing.

The three clock pins, SCKI, LRCK and BCK, are connected to digital channels through 0 ohm resistors that can be changed to some low-value resistors if required for impedance matching. This turned out to be unnecessary. The digital channels are used to drive all clock inputs when the DUT is in slave mode. In master mode, LRCK and BCK work as outputs, so the digital channels would be used in receiving mode. Clocking will be described in detail in Chapter 3.6.3.

The DOUT pin is also connected through a 0 ohm resistor. The pin outputs the digitized audio, and the data is captured by the tester's digital channel for processing and analysis.

After loading the test program, the digital channels are tested for shorts and leakage. Shorts are tested by forcing a small current and measuring voltage, expecting the voltage to rise to a programmed voltage limit. Leakage is tested by forcing a low voltage and measuring current.

3.5.3 Analog Pins

The three analog pins on the DUT are VREF, the analog-to-digital converter's reference voltage decoupling, and the two analog inputs, VINL and VINR. The reference voltage is 0.5 VCC, or 2.5 V nominal. VINL and VINR have a peak-to-peak input voltage equal to 0.6 VCC or 3 V nominal. [12 pp. 4]

Figure 11 shows how the VREF pin is connected on the DIB.

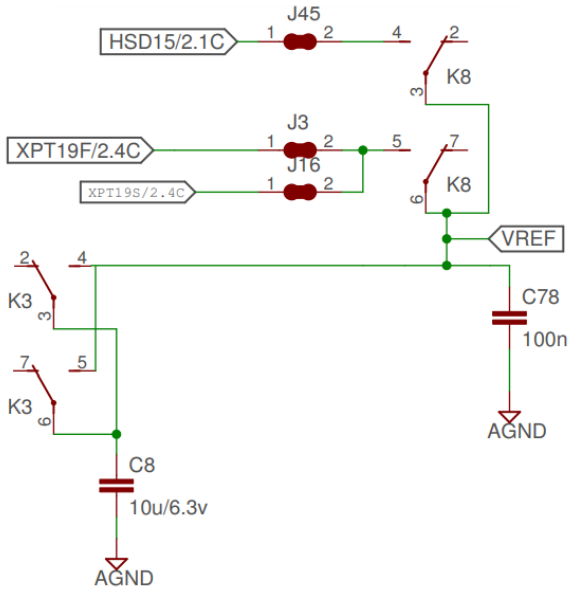

Figure 11. Diagram showing the circuit connected to the VREF pin.

As shown in Figure 11, the VREF pin has a 100 nF decoupling capacitor directly connected to the pin, and a 10 µF decoupling capacitor connected through a relay so it can be disconnected to speed up continuity testing. There is also a digital channel and a matrix line connected to the pin through a relay. The digital channel is used for continuity testing, and the matrix line for accurate measurement of the reference voltage, and during the board check for measuring first the small capacitor, then both. These can be disconnected by the relay to minimize any interference during dynamic performance measurements.

As an example of the circuitry for the analog input pins, Figure 12 shows the left channel.

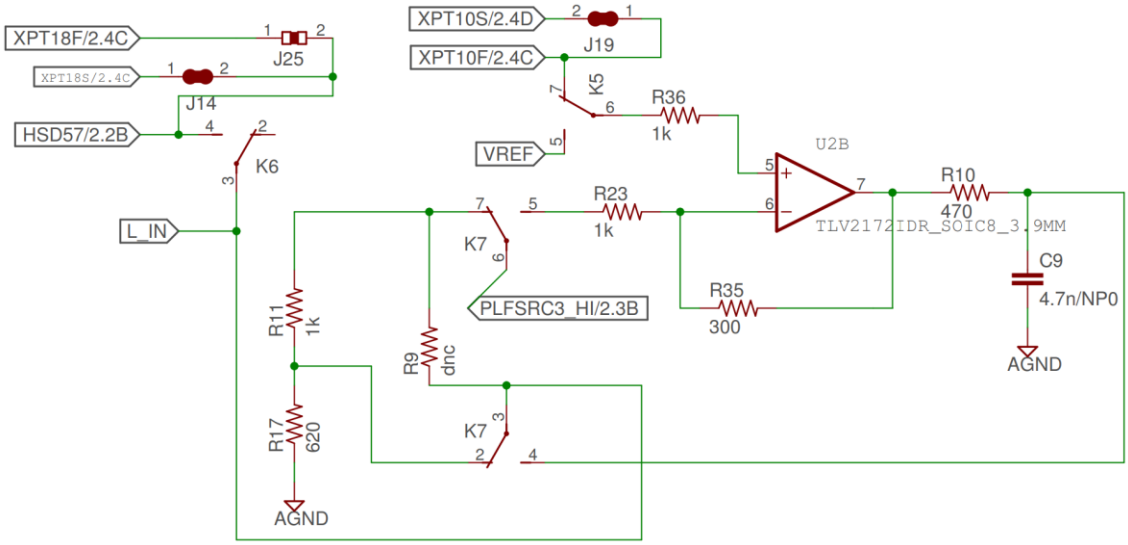

Figure 12. A diagram showing the circuit connected to the left analog input pin.

As can be seen from Figure 12, the VREF pin can be connected via a relay to the board's two op-amps' non-inverting inputs to bias them to the reference voltage. In its normally closed position, the relay connects those inputs to the DC matrix to facilitate testing of the op-amps. The analog inputs, VINL and VINR, are connected to the tester's low frequency AWG, through either a simple voltage divider, or an attenuating op-amp circuit and an anti-aliasing filter similar to those in the end product. Switching between these two is done with a relay. The pins are also connected to a digital channel and to the DC matrix through a relay for board check and continuity testing.

The voltage divider was added so that the device can also be tested without the additional circuitry, while being able to use the AWG in a more optimal amplitude range to maximize its performance. With regards to continuity testing, detailed in Chapter 3.6.2, a compromise was made in the board design. Continuity is typically tested by forcing a low current, between 100 µA and 1 mA, but in this design some of the current flows to ground through the ground-connected resistor of the voltage divider, so a higher, 2 mA current must be used to ensure a large enough voltage drop over the resistor in case of an open connection at the DUT. This was done to minimize the number of relay connections in the signal path, and the higher current was deemed acceptable. Solder pads were also added for a 0 ohm resistor, denoted by a resistor marked

as “dnc” or “do not connect” in the diagram, so the voltage divider can be bypassed, while also reducing the number of passes through a relay by one.

The voltage dividers are tested by first routing a DC source through the AWG’s channel card and forcing a small current through both resistors and measuring the voltage, from which the total resistance is calculated. Then the measurement is repeated from the DC matrix line, from where the current flows only through the ground-connected resistor, whose resistance is then calculated and subtracted from the total resistance, giving the resistance of the input resistor.

The op-amp circuits are tested by applying a few combinations of DC voltages from the matrix line to the non-inverting input, and through the AWG’s channel card to the inverting input. Their output voltages are measured, and attenuation is calculated from the difference between input and output voltages. No AC tests are performed.

3.6 Test Implementations

Initial development of the test program was done on tester simulator software. With the simulator the test program can be stepped through while monitoring the state of each tester instrument to make sure they are doing what the programmer had intended without risking damage resulting from programming errors to the DUT, the device interface board, or the tester’s instruments. After the basic structure of the test program and its test functions were completed, the program was developed further on the ATE tester’s workstation.

3.6.1 Test Program Initialization

After loading the test program, certain actions are performed to initialize the tester hardware and the test program. Instruments used in the program are powered on and calibrated. The digital channels’ configurations such as edge timings are loaded, digital test vectors are loaded into vector memory, the tester’s digital and analog clocks are configured, an A-weighting filter is created,

and a test tone is created and moved into the AWG's waveform memory. These will be described in detail in Chapter 3.6.3. The board check is then run, and if the board passes all tests, the program is ready for testing.

3.6.2 Continuity

Continuity is tested first after the DUT is inserted into the contactor to check that all pins on the device are in contact before continuing with other tests. It is done by detecting the ESD protection diodes, or silicon-controlled rectifiers that behave essentially like diodes, on the device's input and output pins. To detect the protection diode between a pin and a power supply pin, the power supply pin is forced to 0 V while a low positive current is forced into the pin being tested, and the voltage is measured. A positive voltage of one diode drop is expected. A negative current is forced to detect the diode between a pin and ground. A voltage reading of 0 V indicates a short, and an open causes the voltage to reach the source's programmed clamp voltage. To achieve a shorter test time, pins can be tested in parallel. However, if two adjacent pins are shorted, the combined current is forced through their two parallel diodes, resulting in the expected voltage drop. To avoid this adjacent fault masking, only every other pin is tested in parallel while the other pins are grounded. [2 pp. 40.]

Each pin's expected forward voltage in both directions is listed in Table 2. Loose test limits, −900 mV to −300 mV and 300 mV to 900 mV, are used in the tests.

Table 2. Approximate expected forward voltages of pins to be tested for continuity.

Pin	Pin to ground	Pin to power supply
1 VREF	−550 mV	700 mV
3 VCC	−500 mV	Not tested
4 VDD	−500 mV	Not tested

Pin	Pin to ground	Pin to power supply
6 SCKI	−450 mV	Not tested
7 LRCK	−450 mV	650 mV
8 BCK	−450 mV	650 mV
9 DOUT	−450 mV	650 mV
10 MD0	−450 mV	Not tested
11 MD1	−450 mV	Not tested
12 FMT	−450 mV	Not tested
13 VINL	−670 mV	770 mV
14 VINR	−670 mV	770 mV

As shown in Table 2, all pins are tested to ground, while only the analog pins and LRCK, BCK and DOUT are tested to power supply. The other pins lack ESD protection diodes to power supply, as can be deduced from the DUT's datasheet's Absolute Maximum Ratings. This was initially confirmed by measuring the forward voltages using a digital multimeter in diode test mode.

Before testing, the larger capacitor is disconnected from pin 1 (VREF), and the digital channel is connected to it by closing the relay. Pins 1 and 6 through 12 are tested by forcing a negative current of 100 µA with the per-pin measurement instruments of the tester's digital channels, first the odd-numbered pins in parallel, then the even-numbered pins. The measurement is then repeated with a positive current, excluding pins 6 and 10 through 12. All other pins are connected to ground during the measurement. Clamp voltages are programmed to −1.5 V and 1.5 V.

If the voltage dividers for the analog inputs, pins 13 and 14, are bypassed as described in Chapter 3.5.3, the pins can be tested together with VREF and the digital pins using the tester's digital channels connected to the pins through a relay. With the voltage dividers in use, the analog inputs must be tested using the tester's DC sources through the matrix lines that are connected via the same relay as the digital channels. This is due to the per-pin measurement

instruments' limited current capability, while a comparatively high current of 2 mA is needed as discussed in Chapter 3.5.3.

The power pins are tested one-by-one, with all other pins connected to ground and the large decoupling capacitors disconnected. The power supply pins only have a protection diode between the pin and ground, so a current of 100 µA is only forced in the negative direction. The sources' clamp voltage is programmed to −2 V.

3.6.3 Dynamic Performance

To test the dynamic performance, numerous things need to be set up: power for the DUT, its format and mode pins, relays on the DIB, power for the op-amps, the tester's clocks, digital channels' timings and levels, a test tone, and finally a digital test pattern for driving the device's clocks and capturing its output data.

The device is tested with nominal voltages: 5 V for VCC and 3.3 V for VDD. Both power supply pins have the large capacitor connected to it. The format and mode pins are pulled to ground using the per-pin measurement instrument to match the settings used in the final product, namely I2S format and slave mode. The large capacitor is initially disconnected from VREF, the matrix line and digital channel are connected to it, and VREF is connected to the op-amps' non-inverting inputs. The matrix line and digital channel are disconnected from the analog inputs, and the low frequency AWG is connected to them through the op-amp circuits. The op-amps are powered by one of the tester's DC sources, programmed to 9 V.

At test program initialization, the tester's digital and analog master clocks are both set to 196.608 MHz. Clocks for the digital and analog instruments are divided from these. The divider for the digital clock is 16, yielding a frequency of 12.288 MHz that will be used for the digital pattern, matching the SCKI frequency used in the end product. The analog master clock is divided by 512, yielding a 384 kHz clock to be used for the low frequency AWG.

For the test tone, an FFT frequency bin close to 1 kHz was to be selected. The DUT is tested at a sampling frequency F_s of 48 kHz, giving the ADC a Nyquist frequency of 24 kHz. 1024 samples are captured for SNR and THD measurements. Dividing F_s by the number of captured samples yields a frequency resolution of 46.875 Hz. Dividing the desired frequency of 1 kHz by the frequency resolution results in 21.333…, so finally bin 23, mutually prime with the number of samples, was chosen as the frequency bin, i.e. 1078.125 Hz.

The low frequency AWG is used to source the test tone. At test program initialization, the samples of the test tone are calculated and moved to the AWG's waveform memory. Listing 1 illustrates how the samples are calculated.

```
float tone_1khz[8192];
double Fbin = 23;
int samples = 8192; /* 1024*384000/48000 */
int i;

for (i = 0; i < samples; i++) {
    tone_1khz[i] = sin(2.0 * M_PI * Fbin/samples * i);
}
```

Listing 1. Calculating test tone samples for the low frequency AWG.

The `for` loop in Listing 1 calculates the samples for 23 periods of sine wave. The number of samples for the test tone is the number of captured samples times the ratio of the AWG's sampling rate to the DUT's sampling rate. The result is a coherent signal, as described in Chapter 3.3.1.

A setup was created for the digital channels. This includes drive and compare levels, drive formats, and drive and compare timings. The drive levels are the voltages applied when a channel is driving the pin to high or low logic level. Nominal voltages, 3.3 V and 0 V respectively, are used. The compare levels are the thresholds for valid DUT outputs. The minimum voltage for high level is set to 2.8 V, and the maximum for low level to 0.5 V, as specified in the DUT's datasheet. As the device is only tested in slave mode, the compare levels are only relevant to the DOUT pin. The formats used are return-to-zero for SCKI, and non-return-to-zero for LRCK and BCK.

As the SCKI frequency (F_{SCKI}) is the basis for the digital test pattern, the timing of each digital channel is defined in terms of its clock period. SCKI's drive edges are set to $0.5/F_{SCKI}$ and $1/F_{SCKI}$, meaning that a "1" in the test pattern will drive the channel high at the middle point of the clock period, and SCKI's format being return-to-zero, it will be driven back to low at the end of the clock period. This results in a 50 % duty cycle, within the required 40 % to 60 %. There is no phase relationship required between SCKI and LRCK. LRCK's drive edge is set to $0.5/F_{SCKI}$, in phase with SCKI. As its drive format is non-return-to-zero, it only has one drive edge that affects it when the test pattern changes its state from low to high and vice versa. LRCK requires a minimum setup time of 50 ns to BCK rising edge. To ensure this, BCK's drive edge is set to $0.5/F_{SCKI}$+55 ns, giving it some margin. DOUT's compare window is set from $0.5/F_{SCKI}$ +30 ns to $0.6/F_{SCKI}$+30ns, so DOUT output can be captured close to BCK's rising edge where the output is valid.

A digital test pattern was created to make the DUT operate and to capture its digital output data. The pattern first synchronises the tester's digital and analog clocks, then starts the AWG, drives the DUT's clocks and captures its digital output. As SCKI is configured as return-to-zero, each line of the pattern, called vector, drives SCKI high, completing a single SCKI clock cycle as it returns to zero. The other clocks, being non-return-to-zero, are driven low explicitly: BCK's state is changed every two SCKI cycles, LRCK's every 128 SCKI cycles. If the DUT were to be tested in its other modes, separate digital patterns would need to be created for each combination of data format and SCKI clock rate.

The pattern consists of two separate I2S frame loops with loops for left and right channel bits nested within them. The first frame loop drives the clocks without capturing the output while a low-amplitude test tone is fed into the analog inputs to wake up the DUT and to let the VREF voltage settle. The VREF voltage and power supply currents are then measured and compared to test limits. The test tone's amplitude is set to 3 V peak-to-peak, the full scale amplitude of the DUT, and the VREF voltage is again given time to settle. Then the pattern generator continues to the second frame loop. It compares the output level and captures

the I2S data from DOUT at every BCK rising edge until 1024 samples have been captured. An invalid output level at any point causes the test to fail.

After capturing the samples, the data is processed using the tester's array processor. First, as the captured data is 32 bits per sample, 24-bit signed sample plus eight trailing zeros, the 23 least significant bits of each sample are right shifted by 8. The samples are then converted to double precision floating-point format. Next, the interleaved samples of the left and right channel are separated, and an FFT is performed on the signals. They are then brick wall filtered by zeroing the frequency bins below 20 Hz, in this case only the DC bin, and above 20 kHz, the generally accepted limits of human hearing, by zeroing the elements that fall outside those limits in the resulting arrays. Figure 13 below shows the power spectrum before and after brick wall filtering.

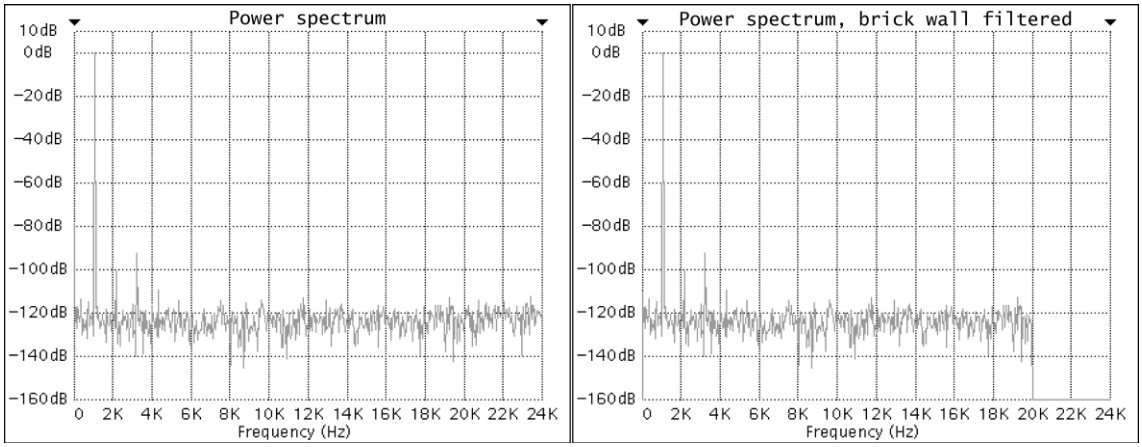

Figure 13. Full power spectrum (left) and brick wall filtered power spectrum.

As can be seen from the full power spectrum in Figure 13, the DC bin is just above −80 dB, while most of the noise is below −120 dB. Harmonic distortion can be seen as peaks at the harmonic frequencies of the test tone, 1078.125 Hz at 0 dB, the highest, third harmonic, reaching close to −90 dB. The removal of the DC bin and noise above 20 kHz is visible in the filtered spectrum. After this filtering, THD and SNR are calculated.

Before calculating the A-weighted SNR, the A-weighting filter is first applied by multiplying the FFTs by the magnitude of the filter, shown in Figure 14 below.

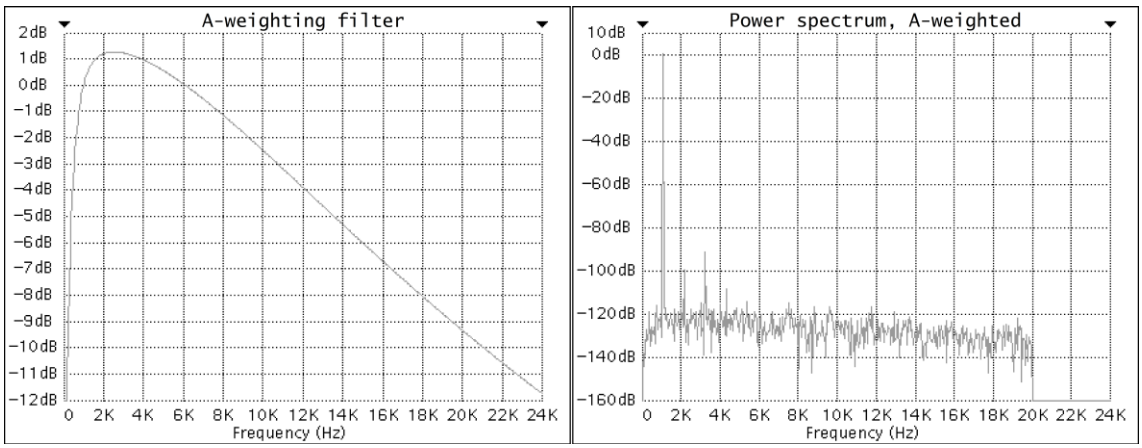

Figure 14. A-weighting filter (left) and the weighted power spectrum (right).

The A-weighting filter in Figure 14 shows how much it affects the spectrum. It attenuates frequencies below 1 kHz and above 6 kHz, and frequencies in between are slightly amplified. This effect is evident in the weighted spectrum when compared with the unweighted spectra in Figure 13. As the DUT's SNR specification is A-weighted, this measurement is more comparable to the specification than the first, unweighted measurement.

Finally, to test the total harmonic distortion + noise (THD+N), the digital test pattern is repeated, but this time the test tone's amplitude is set to −0.5 dB, or about 2.83 V peak-to-peak to match the test conditions in the specification.

3.7 Results

In total, 50 devices from the troublesome batch and 50 from a new batch were tested. As a test setup for the handler remains to be implemented, the devices were tested using a manual socket.

Of the 50 devices tested from the new batch, 49 passed on the first round. The failed device failed the left channel's unweighted SNR test marginally, measuring 92.9 dB on the first round, but didn't fail again when retested multiple times. Table 3 below shows each parameter's test limits, the mean, and three standard deviations below and above the mean. SNRA is the A-weighted SNR.

Table 3. Test results.

Parameter	**Low limit**	**High limit**	**Mean**	**−3σ**	**+3σ**
I VCC	0 mA	11 mA	8.80 mA	8.41 mA	9.20 mA
I VDD	0 mA	8 mA	5.17 mA	4.94 mA	5.41 mA
VREF	2.450 V	2.550 V	2.493 V	2.466 V	2.520 V
THD, left	−120 dB	−87 dB	−89.7 dB	−90.5 dB	−89.0 dB
SNR, left	93 dB	120 dB	94.3 dB	92.7 dB	95.8 dB
SNRA, left	95 dB	120 dB	96.7 dB	95.1 dB	98.3 dB
THD+N −0.5 dB, left	−120 dB	−87 dB	−88.7 dB	−89.4 dB	−88.0 dB
THD, right	−120 dB	−87 dB	−91.5 dB	−92.5 dB	−90.4 dB
SNR, right	93 dB	120 dB	94.3 dB	92.7 dB	96.0 dB
SNRA, right	95 dB	120 dB	96.8 dB	95.2 dB	98.4 dB
THD+N −0.5 dB, right	−120 dB	−87 dB	−89.8 dB	−90.7 dB	−88.9 dB

The devices were mostly well within the specified limits, with only the −3σ of the unweighted SNR reaching below the test limit. From these results it is evident that there is a noticeable difference between the two channels' THD performance. This warranted further investigation. By testing some devices using the voltage divider instead of the op-amp circuits, the difference in THD performance vanished, revealing that the likely culprit is the op-amp.

From the troublesome batch, only 33 devices passed. Surprisingly the devices that passed had somewhat better dynamic performance than the newer batch, with even the −3σ of the unweighted SNR being 0.3 dB above the test limit, though the sample size for both batches are quite small. The failed devices were retested, but none passed the retest. One device was otherwise functional, but its VCC current was 1.44 mA above the limit. Of the 17 failed devices, eight failed one or more continuity tests, two failed one of the supply current tests, and the remaining seven failed the left channel THD test. The

THD failures were catastrophic. Failure analysis showed that the analog channels were either completely dead, or the captured waveform was severely distorted.

4 Conclusions

The aim of this project was to develop a test setup and a test program for an ATE tester to perform incoming acceptance tests on PCM1808 analog-to-digital converters before using them in a product. The devices were to be tested for functionality and dynamic performance.

The project was successful in the development of the test setup and test program, and initial tests on the ADCs were performed with good results. The design of the device interface board allowed performing the essential tests and has flexibility for testing the devices without the additional circuitry if required in the future, with some possibilities for easy modifications.

The small troublesome batch of ADCs, procured from AliExpress during the global chip shortage, was tested, and 34 % of the devices were found to be faulty. Devices tested from a batch sourced from a reputable distributor were all found to be fully functional and performing to specification as expected. Based on these findings it is advisable to purchase components only from trusted sources. Sample-based testing of future batches may be sufficient.

To test larger quantities of the ADCs, a setup for a handler should be built to automate testing. This would make it possible to test thousands of devices in a day. Care should be taken with the setup to avoid damage to the ADC’s delicate leads.

The test program could be developed further by adding tests for DC gain mismatch and gain error, and more dynamic performance tests, including dynamic range and channel separation tests. The device could also be tested with higher system clock frequencies to judge whether the final product’s dynamic performance could be improved by changing the clock frequency used in it.

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